

Quad Power Management Switches

General Description

The AV9304/AV9504 Power Management Integrated Switch (PMIS) is designed for 3 and 5 Volt systems that need to switch steady state currents of up to 500mA. The PMIS is a self contained part requiring no external components. The AV9304 and AV9504 contain four power switches, in either the 16 pin PDIP or the 300 mil wide 16 pin SOIC package.

The N-Channel FET switches have a typical 0.3Ω on-resistance, with a maximum of 0.4Ω . For switching currents larger than 500mA, these transistors can be paralleled together. The +2.7V to +3.7V input supply range, the low quiescent current and the automatic power down features make the AV9304 ideal for battery-powered switching and control applications, such as notebook computers, portable medical analyzers and test equipment.

The "soft turn-on" feature of the 9304/9504 ensures that there will be no spikes on the switched power supply when the power turns on to the load.

The 9304 operates with a supply voltage of 2.7 to 3.6V while the 9504 operates with a supply voltage of 4.5 to 5.5V. Either part can switch loads from 2.7V to 5.5V.

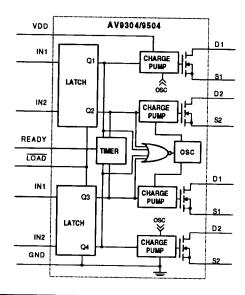
Features

- AV9304: 3.0 or 3.3V operating supply voltage
- AV9504: 5V operating supply voltage
- Switches loads from 2.7V to 5.5V
- 0.3Ω typical, 0.4Ω max switch resistance
- Steady state current of 500mA per switch
- Automatic Power Down
- 1 msec FET soft turn on
- No external components required
- Output Ready signal

Applications

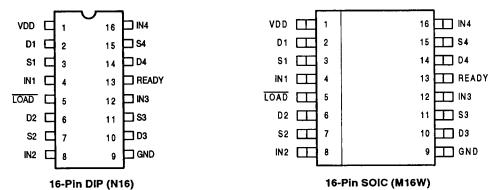
- Notebook PC Power Switching
- PCMCIA VCC Switching
- PDA's
- Palmtop Computers
- Hand-Held Medical Instruments

Block Diagram





Pin Configuration



Pin Descriptions

PIN#	PIN NAME	TYPE	DESCRIPTION
1	VDD		Positive supply voltage for the IC
2	D1	Out	FET 1 Drain
3	S1	Out	FET 1 Source
4	IN1	In	Logic input to FET 1 driver
5	LOAD	In	Transparent low latch. A logic "0" on this pin allows data to flow from IN to the FET driver. A logic "1" latches the outputs in their present state.
6	D2	Out	FET 2 Drain
7	S2	Out	FET 2 Source
8	IN2	In	Logic input to FET 2 driver
9	GND	_	Ground
10	D3	Out	FET 3 Drain
11	S3	Out	FET 3 Source
12	IN3	In	Logic input to FET 3 driver
13	READY	Out	Pulse indicating last input to change has its FET stable and fully turned on
14	D4	Out	FET 4 Drain
15	S4	Out	FET 4 Source
16	IN4	In	Logic input to FET 4 driver

Ordering Information:

Part Number	Temperature Range	Package Type
AV9304CN16	0°C to 70°C	16-lead plastic DIP (P16)
AV9304CW16	0°C to 70°C	16-lead Plastic SOIC (M16W)
AV9504CN16	0°C to 70°C	16-lead plastic DIP (P16)
AV9504CW16	0°C to 70°C	16-lead Plastic SOIC (M16W)

AV9304/AV9504



Absolute Maximum Ratings

Operating Conditions

VDD referenced to GND	7V
Storage temperature	
Voltage on I/O pins	05V to VDD +0.5V
Power dissipation	0.5 Watts

Drain Voltage:	
AV9304	2.7V to 5.5V
AV9504	2.7V to 5.5V
Operating temperature under bias	0°C to +70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

AV9304 (Operating V_{DD} =+2.7 to +3.7V, T_A =0°C to 70°C unless otherwise stated) AV9504 (Operating V_{DD} =+4.5 to +5.5V, T_A =0°C to 70°C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		DC Characteristics			1	
Chip supply	V_{DD}	AV9304	2.7	3.3	3.7	v
Chip supply	V_{DD}	AV9504	4.5	5	5.5	v
Switch Drain Voltage	V _{DF(} 1)		2.7		5.5	v
Switch Source Voltage	V _{SF}		V _{DF} -0.2		V _{DF}	v
Input Low Voltage	V _{IL}		V _{SS}		0.2V _{DD}	v
Input High Voltage	V _{IH}		0.7 V _{DD}		V _{DD}	v
Switch Current	I _{DF}		0		500	mA
Supply Current	I _{DD2} (2)	All switches active		100	200	μA
Standby Current	I _{DDSB}	All switches off		2	4	μA
Input Low Current	I _{IL}	$V_{IN} = 0V$			-2	μА
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			2	μA
Switch on Resistance	R _{ON}	All conditions		.3	.4	Ω
Switch on Resistance	R _{ON}	25°C,V _{DF} =3.3V		.25	 	Ω
		AC Characteristics			L I	
LOAD Pulse Width	t _W		50			ns
INX to LOAD Inactive Setup Time	t _{SU}		20		-	ns
LOAD inactive to INX Hold Time	t _{HD}		10			ns
Delay to Ready	t _D				6	ms

Note 1: In addition to the power dissipated by the oscillator and 4 charge pumps, the drop across the switches also contributes to the on chip power. This power per switches is given by: $I_{DF}(V_{DF}-V_{SF})$. The total on-chip power should be held below 0.5W.

Note 2: The current consumed by the IC is proportional to the number of switches on. If only 1 FET is on, I_{DD} will be 1/4 of specified value.



Device Description

Each of the channels consists of a transparent latch, charge pump, and N-Channel FET. Logic inputs to the drivers are latched when \overline{LOAD} goes high. The logic high signal from the latch activates the charge pump and, a few milliseconds later, the FET is fully turned on. On chip circuitry controls the FET turn on, which typically takes 1ms (fig 2.), to avoid the power supply current spikes (fig. 1) which would occur if the switch turned on fast into a fully discharged load capacitance. The chip has a common oscillator that drives the 4 charge pumps and runs at approximately 500KHz.

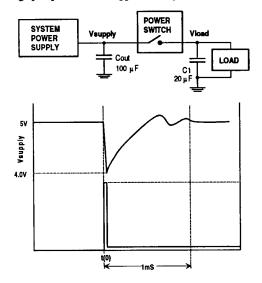


Figure 1. Power Supply glitch caused by fast ToN

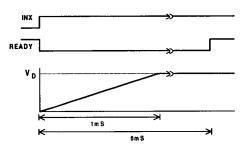


Figure 2. ICS9304/9504 controlled output rise-time and READY signal timing

An edge detector monitors the 4 latch outputs and activates the timer when any output goes high. The Ready signal, which comes from the timer, goes low immediately and then goes high again typically in 6ms, thus generating a negative going pulse (see Figure 1). Ready returns to the high state when output FET is stable and fully turned on.

The automatic power down feature works by monitoring the latch outputs. When all the latch outputs are at a logical zero, the output of the NOR gate is high and asserts the power down to the oscillator.

The AV9304/9504 FETs do not contain source to drain diodes, so when the part is used for switching inductive loads an external diode should be connected across the FET.