LSI LOGIC

RUPCIU and RUPCI 3.3V/5V PCI Universal Buffers

Preliminary

Description

LSI Logic Corporation has developed two versions of a mixed 3.3- and 5-V Peripheral Component Interconnect (PCI) Universal Buffer, the RUPCIU and the RUPCI. These buffers have been designed specifically to comply with both the 3.3-V and 5-V signaling environments of the *PCI Bus Specification Revision 2.0*.

The RUPCIU is a bidirectional 3.3V/5V I/O buffer. The RUPCI is a bidirectional 3.3V/5V I/O buffer with a latch in the output signal path. The RUPCI and RUPCIU buffers offer a TTL/LVTTL input receiver and output V/I characteristics that comply with the PCI electrical specification. Both buffers use only one I/O slot and one pad cell. The buffers are available in the LCA300K, LEA300K, and LCB300K libraries. Using these buffers reduces the time and effort needed to design an ASIC that connects to the PCI bus.

The *PCI Bus Specification Revision 2.0* provides a robust and well-defined bus standard. The bus has been optimized for direct interconnection and provides multiplexed data/address pins. In addition, the bus architecture accounts for future requirements of the market by offering microprocessor independence as well as a migration path from 5-V to 3.3-V signaling environments.

Figure 1 shows the logic diagram for the RUPCIU buffer, and Figure 2 shows the logic diagram for the RUPCI buffer.

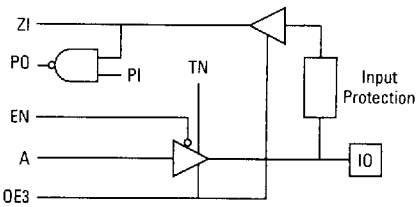

Figure 1. RUPCIU Logic Diagram

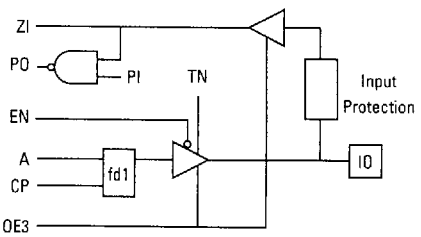

Figure 2. RUPCI Logic Diagram

Features and Benefits

- Compliant with *PCI Bus Specification Revision 2.0*
  - Eliminates engineering effort of designing an interconnect to PCI bus
- Meets both the 3.3-V and 5-V electrical specifications of the PCI bus
  - Provides for interconnect to either specified signaling environment allowing for system migration with the same I/O cell
  - Allows for universal interconnect to the PCI bus
- V/I characteristics that meet the PCI bus drive requirements
  - Provides for direct silicon interconnect to PCI transmission line
- Uses one I/O slot and one pad cell
  - Maximizes available I/O
- Two versions available
  - RUPCIU
    Bidirectional I/O buffer that provides maximum flexibility in I/O path design
  - RUPCI
    Bidirectional I/O buffer with registered output that assures clock-to-output timing for the I/O buffer stage
- Available in the LCA300K Compacted Array™, LEA300K Embedded Array®, and LCB300K cell-based product families
  - 0.6-micron drawn gate length (0.45-micron effective channel length)
  - Provides proven access to PCI technology

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RUPCIU

The RUPCIU is a bidirectional 3.3V/5V I/O buffer. The macrocell uses the 5-V core power source. The I/O ring can use either 3.3 or 5 V. OE3 selects the internal logic level to operate at either 3.3 V or 5 V. OE3 should match V_{DD4} as shown in Table 1. The OE3 signal is a DC state signal that the designer can use to introduce a latch in the core design with no performance penalty.

Cell delays are different depending on the value of V_{DD4}, thus there are two models for the cell. RUPCIU3V is the model for V_{DD4} = 3.3 V, and RUPCIU5V is the model for V_{DD4} = 5 V. Both models refer to the same layout cell.

Table 1. RUPCIU OE3

OE3	V_{DD4}
0	5 V
1	3.3 V

RUPCIU Specifications

This section provides the specifications for the RUPCIU bidirectional PCI 3.3V/5V I/O buffer.

Name: RUPCIU

Description: Bidirectional PCI 3.3V/5V I/O Buffer

Coding Syntax: (IO, ZI, PO) = RUPCIU3V (IO, A, EN, TN, OE3, PI);

(IO, ZI, PO) = RUPCIU5V (IO, A, EN, TN, OE3, PI);

Table 2 states loading values in standard loads, and Table 3 lists the operating conditions. Table 4 and Table 5 list DC characteristics for the commercial operating range.

Table 2. RUPCIU Loading Characteristics

Version	Technology	A	EN	TN	PI	OE3
RUPCIU	LCA/LEA300K	1.1	1.1	0.6	0.6	3.5
	LCB300K	1.4	1.4	0.8	0.8	4.8

Table 3. RUPCIU Operating Conditions

Parameter	5 V	3.3 V
V_{DD}	4.75 V–5.25 V	4.75 V–5.25 V
V_{DD4}	4.75 V–5.25 V	3 V–3.6 V
Junction Temperature	0–100 °C	0–100 °C

Table 4. RUPCIU DC Characteristics for 5-V Signaling

Symbol	Parameter	Condition	Min	Typ	Max
V_{IH} V_{IL}	Input Voltage High Level Input Voltage Low Level		2.0 V -0.5 V		V_{DD} + 0.5 V 0.8 V
I_{INH} I_{INL}	Input Leakage Current High Input Leakage Current Low	$V_{IO} = V_{DD}$ $V_{IO} = V_{SS}$	 -10 µA		+10 µA
I_{OL} I_{OH}	Output Current at Low State Output Current at High State	V_{OL} = 0.4 V[1] V_{OH} = 2.4 V[1]	12 mA		 -6 mA
C_{OUT}	Output Pin Capacitance[2]			3.5 pF	

Note:
1. Meets the V/I characteristics of the *PCI Bus Specification Revision 2.0.*
2. Does not include package capacitance.

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RUPCIU Specifications (Continued)

Table 5. RUPCIU DC Characteristics for 3.3-V Signaling

Symbol	Parameter	Condition	Min	Typ	Max
V_{IH} V_{IL}	Input Voltage High Level Input Voltage Low Level		0.475 x V_{DD4} -0.5 V		V_{DD} + 0.5 V 0.325 x V_{DD4}
I_{INH} I_{INL}	Input Leakage Current High Input Leakage Current Low	$V_{IO} = V_{DD}$ $V_{IO} = V_{SS}$	 -10 µA		+10 µA
I_{OL} I_{OH}	Output Current at Low State Output Current at High State	V_{OL} = 0.4 V[1] V_{OH} = 2.4 V[1]	6 mA		 -6 mA
C_{OUT}	Output Pin Capacitance[2]			3.5 pF	

Note:
1. Meets the V/I characteristics of the *PCI Bus Specification Revision 2.0.*
2. Does not include package capacitance.

Note that the RUPCIU buffer has features of both input and output buffers. The timing data in Table 6 and Table 7 show output delay times (A–IO) and input delay times (IO–ZI).

Table 6. RUPCIU AC Timing for 5-V Signaling

Version	I/O Slots	Pads	Propagation Delay[1] (ns)						
				Output Load (pF) for Delay Path A–IO				Input Fanout Loads for Delay Path IO–ZI		
RUPCIU	1	1	Transition	15	50	85	100	1	2	4
			t_{PLH}	2.21	3.15	3.85	4.13	1.04	1.13	1.29
			t_{PHL}	4.5	6.1	7.2	7.6	0.42	0.47	0.56

Note:
1. V_{DD} = 5 V and V_{DD4} = 5 V, junction temperature = 25 °C. Estimated wire length = 0, process = nominal.

Table 7. RUPCIU AC Timing for 3.3-V Signaling

Version	I/O Slots	Pads	Propagation Delay[1] (ns)						
				Output Load (pF) for Delay Path A–IO				Input Fanout Loads for Delay Path IO–ZI		
RUPCIU	1	1	Transition	15	50	85	100	1	2	4
			t_{PLH}	2.59	3.45	4.12	4.38	0.72	0.80	0.96
			t_{PHL}	4.48	6.29	7.53	7.99	0.51	0.56	0.66

Note:
1. V_{DD} = 5 V and V_{DD4} = 3.3 V, junction temperature = 25 °C. Estimated wire length = 0, process = nominal.

RUPCIU Specifications (Continued)

Table 8 and Table 9 list AC characteristics for the RUPCIU buffer. Power and ground rules are the same as the B6 (6 mA) output buffer.

For more information about power and ground rules, refer to Section 1.13 "Factors Affecting Power and Ground" in the *LCA300K Gate Array Series Product Databook, the LEA300K Embedded Array® ASICs Product Databook*, or the *LCB300K Cell-Based ASICs Product Databook.*

Table 8. RUPCIU AC Characteristics for 5-V Signaling

Symbol	Parameter	Condition	Min	Typ	Max
I_{OH}	Switch High Output Current	V_{OH} = 1.4 V V_{OH} = 2.4 V V_{OH} = 3.1 V	 -120 mA		-44 mA -20 mA
I_{OL}	Switch Low Output Current	V_{OL} = 2.2 V V_{OL} = 0.55 V V_{OL} = 0.71 V	95 mA 25 mA		 150 mA
t_R	Unloaded Output Rise Time	V_O = 0.4 V–2.4 V	1 V/ns		5 V/ns
t_F	Unloaded Output Fall Time	V_O = 2.4 V–0.4 V	1V/ns		5 V/ns

Table 9. RUPCIU AC Characteristics for 3.3-V Signaling

Symbol	Parameter	Condition	Min	Typ	Max
I_{OH}	Switch High Output Current	V_{OLH} = 0.3 x V_{DD4} V_{OH} = 2.17 V V_{OH} = 0.7 x V_{DD4}	 -30 x V_{DD4} mA		-12 x V_{DD4} mA -5.5 mA
I_{OL}	Switch Low Output Current	V_{OL} = 2.6 x V_{DD4} V_{OL} = 0.3 V V_{OL} = 0.18 x $V_{DD}4$	16 x V_{DD4} mA 8 mA		 35 x V_{DD4} mA
t_R	Unloaded Output Rise Time	V_O = (0.2–0.6) x V_{DD4}	1 V/ns		4 V/ns
t_F	Unloaded Output Fall Time	V_O = (0.6–0.2) x V_{DD4}	1 V/ns		4 V/ns

RUPCI

The RUPCI is a bidirectional 3.3V/5V I/O buffer with a latch in the output signal path. The signal is latched with a rising edge triggered flip-flop for synchronization.

The macrocell uses the 5-V core power source. The I/O ring can use either 3.3 or 5 V. OE3 selects the internal logic level to operate at either 3.3 V or 5 V. OE3 should match V_{DD4} as shown in Table 10. The OE3 signal is a DC state signal that the designer can use to introduce a latch in the core design with no performance penalty.

Cell delays are different depending on the value of V_{DD4}, thus there are two models for the cell.

RUPCI3V is the model for V_{DD4} = 3.3 V, and RUPCI5V is the model for V_{DD4} = 5 V. Both models refer to the same layout cell.

Table 10. RUPCI OE3

OE3	V_{DD4}
0	5 V
1	3.3 V

RUPCI Specifications (Continued)

This section provides the specifications for the RUPCI bidirectional PCI 3.3V/5V registered I/O buffer.

Name: RUPCI

Description: Bidirectional PCI 3.3V/5V Registered I/O Buffer

Coding Syntax: (IO, ZI, PO) = RUPCI3V (IO, A, EN, CP, TN, OE3, PI);

(IO, ZI, PO) = RUPCI5V (IO, A, EN, CP, TN, OE3, PI);

Table 11 states loading values in standards loads, and Table 12 lists the operating conditions. Table 13 and Table 14 list the DC characteristics for the commercial operating range.

Table 11. RUPCI Loading Characteristics

Version	Technology	A	EN	TN	PI	CP	OE3
RUPCIU	LCA/LEA300K	1.1	1.1	0.6	0.6	1.1	3.5
	LCB300K	1.4	1.4	0.8	0.8	1.4	4.8

Table 12. RUPCI Operating Conditions

Parameter	5 V	3.3 V
VDD	4.75 V–5.25 V	4.75 V–5.25 V
V_{DD4}	4.75 V–5.25 V	3 V–3.6 V
Junction Temp	0–100 °C	0–100 °C

Table 13. RUPCI DC Characteristics for 5-V Signaling

Symbol	Parameter	Condition	Min	Typ	Max
V_{IH} V_{IL}	Input Voltage High Level Input Voltage Low Level		2.0 V -0.5 V		V_{DD} + 0.5 V 0.8 V
I_{INH} I_{INL}	Input Leakage Current High Input Leakage Current Low	$V_{IO} = V_{DD}$ $V_{IO} = V_{SS}$	 -10 µA		+10 µA
I_{OL} I_{OH}	Output Current at Low State Output Current at High State	V_{OL} = 0.4 V[1] V_{OH} = 2.4 V[1]	12 mA		 -6 mA
C_{OUT}	Output Pin Capacitance[2]			3.5 pF	

Note:
1. Meets the V/I characteristics of the *PCI Bus Specification Revision 2.0.*
2. Does not include package capacitance.

Table 14. RUPCI DC Characteristics for 3.3-V Signaling

Symbol	Parameter	Condition	Min	Typ	Max
V_{IH} V_{IL}	Input Voltage High Level Input Voltage Low Level		0.475 x V_{DD4} -0.5 V		V_{DD} + 0.5 V 0.325 x V_{DD4}
I_{INH} I_{INL}	Input Leakage Current High Input Leakage Current Low	$V_{IO} = V_{DD}$ $V_{IO} = V_{SS}$	 -10 µA		+10 µA
I_{OL} I_{OH}	Output Current at Low State Output Current at High State	V_{OL} = 0.4 V[1] V_{OH} = 2.4 V[1]	6 mA		 -6 mA
C_{OUT}	Output Pin Capacitance[2]			3.5 pF	

Note:
1. Meets the V/I characteristics of the *PCI Bus Specification Revision 2.0.*
2. Does not include package capacitance.

RUPCI Specifications (Continued)

Note that the RUPCI buffer has some features of both input and output buffers. The timing data in Table 15 and Table 16 show output delay times (CP–IO) and input delay times (IO–ZI).

Table 17 and Table 18 list the AC characteristics for the RUPCI buffer. Power and ground rules are the same as the B6 (6 mA) output buffer.

For more information about power and ground rules, refer to Section 1.13 "Factors Affecting Power and Ground" in the *LCA300K Gate Array Series Product Databook*, the *LEA300K Embedded Array® ASICs Product Databook*, or the *LCB300K Cell-Based ASICs Product Databook*.

Table 15. RUPCI AC Timing for 5-V Signaling

Version	I/O Slots	Pads	Propagation Delay[1] (ns)						
RUPCI	1	1		Output Load (pF) for Delay Path CP–IO				Input Fanout Loads for Delay Path IO–ZI		
			Transition	15	50	85	100	1	2	4
			t_{PLH}	2.5		4.1	4.4	1.04	1.13	1.29
			t_{PHL}	4.2	5	6.9	7.3	0.42	0.47	0.56

Note:
1. V_{DD} = 5 V and V_{DD4} = 5 V, junction temperature = 25 °C. Estimated wire length = 0, process = nominal.

Table 16. RUPCI AC Timing for 3.3-V Signaling

Version	I/O Slots	Pads	Propagation Delay[1] (ns)						
RUPCI	1	1		Output Load (pF) for Delay Path CP–IO				Input Fanout Loads for Delay Path IO–ZI		
			Transition	15	50	85	100	1	2	4
			t_{PLH}	3.83	5.16	6.14	6.53	0.72	0.80	0.96
			t_{PHL}	3.89	5.69	6.93	7.39	0.51	0.56	0.66

Note:
1. V_{DD} = 5 V and V_{DD4} = 3.3 V, junction temperature = 25 °C. Estimated wire length = 0, process = nominal.

Table 17. RUPCI AC Characteristics for 5-V Signaling

Symbol	Parameter	Condition	Min	Typ	Max
I_{OH}	Switch High Output Current	V_{OH} = 1.4 V V_{OH} = 2.4 V V_{OH} = 3.1 V	 -120 mA		-44 mA -20 mA
I_{OL}	Switch Low Output Current	V_{OL} = 2.2 V V_{OL} = 0.55 V V_{OL} = 0.71V	95 mA 25 mA		 150 mA
t_R	Unloaded Output Rise Time	V_O = 0.4 V–2.4 V	1 V/ns		5 V/ns
t_R	Unloaded Output Fall Time	V_O = 2.4 V–0.4 V	1 V/ns		5 V/ns

RUPCI Specifications
(Continued)

Table 18. AC Characteristics for 3.3-V Signaling

Symbol	Parameter	Condition	Min	Typ	Max
I_{OH}	Switch High Output Current	$V_{OH} = 0.3 \times V_{DD4}$ $V_{OH} = 2.17$ V $V_{OH} = 0.7 \times V_{DD4}$	 $-30 \times V_{DD4}$ mA		$-12 \times V_{DD4}$ mA -5.5 mA
I_{OL}	Switch Low Output Current	$V_{OL} = 2.6 \times V_{DD4}$ $V_{OL} = 0.3$ V $V_{OL} = 0.18 \times V_{DD4}$	$16 \times V_{DD4}$ mA 8 mA		 $35 \times V_{DD4}$ mA
t_R	Unloaded Output Rise Time	$V_O = (0.2–0.6) \times V_{DD4}$	1 V/ns		4 V/ns
t_F	Unloaded Output Fall Time	$V_O = (0.6–0.2) \times V_{DD4}$	1 V/ns		4 V/ns