AVC16245

16 Bit Bus Transceiver with 3-State Outputs

Preliminary

Product Features

- Less than 2 nS maximum propagation delay at 2.5V and 3.3V V_{DD}
- Wide supply voltage range of 1.2V to 3.6 V
- Overvoltage-Tolerant Inputs/Outputs allow mixed-voltage-mode data communications
- Output circuitry with dynamic control minimizes over/undershoot and maximizes output drive
- Extended temp range of -40° to + 85° C
- 2KV ESD
- 48 pin TSSOP and TVSOP package availability

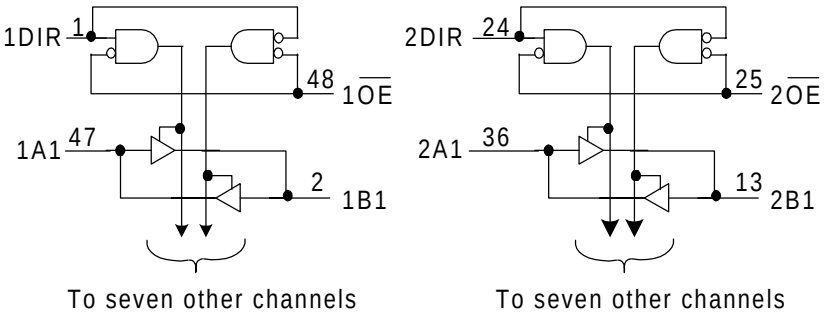
Product Description

The AVC16245 is a 16-bit transceiver featuring non-inverting buffer/line driver with 3-state bus compatible outputs in both send and receive directions.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) inputs. The output enable ($\overline{OE}$) inputs can be used to disable the device so that the buses are effectively isolated.

This product is designed to have an extremely low propagation delay and a minimum amount of power consumption.

Block Diagram

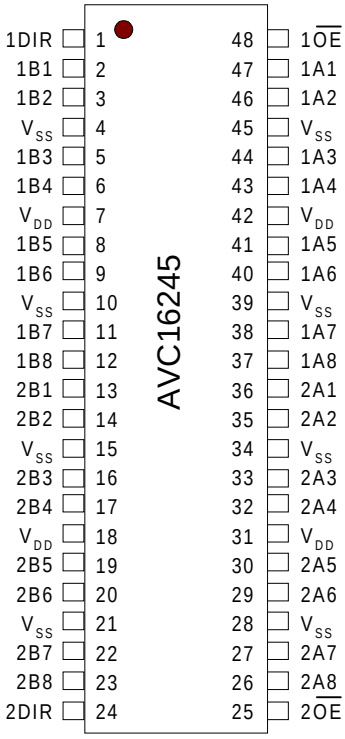


Product Description (Cont.)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied V_{DD} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the $\overline{OE}$ driving device.

Output circuitry is dynamically controlled, which, during output transitions, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical VOL vs. IOL and VOH vs IOH curves to illustrate the output impedance and drive capability of the circuit.

Pin Configuration



Preliminary

Pin Description

Pin Number	Pin Name	Description
48	$1\overline{OE}$	Output enable input (active LOW)
25	$2\overline{OE}$	Output enable input (active LOW)
1	1DIR	Direction Control
24	2DIR	Direction Control
4, 10, 15, 21, 28, 34, 39, 45	V_{SS}	Ground (0V)
7, 18, 31, 42	V_{DD}	Positive supply voltage
2, 3, 5, 6, 8, 9, 11, 12	1B(1:8)	Data inputs/outputs, Bank 1
13, 14, 16, 17, 19, 20, 22, 23	2B (1:8)	Data inputs/outputs, Bank 2
36, 35, 33, 32, 30, 29, 27, 26	2A (1:8)	Data inputs/outputs, Bank 2
47, 46, 44, 43, 41, 40, 38, 37	1A (1:8)	Data inputs/outputs, Bank 1

Function Table

Inputs		Inputs/Outputs	
$\overline{nOE}$	nDIR	nAm	nBm
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

Notes:

H = HIGH voltage level

L = LOW voltage level

X = Don't Care

Z = High impedance "off" state

Capacitance Table

Symbol	Parameter[1]	Cond.	Typ	Max	Unit
Cin	Input Cap.	Vin=0V	2.5	7	pF
Cout	Output Cap.	Vout=0V	6.5	9	pF
CI/O	I/O Port Cap	Vin=0V	6.5	9	pF

Note 1: As applicable to device type

Absolute Maximum Rating(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with respect to V_{SS}	-0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with respect to V_{SS}	- 0.5 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	- 65° to + 150° C	°C
I_{OUT}	DC Output Current	- 50 to + 50	mA
I_{IK}	Continuous Clamp Current, VI<0 or VI>V_{DD}	± 50	mA
I_{OK}	Continuous Clamp Current, Vo<0	-50	mA
I_{DD} I_{SS}	Continuous Current through each V_{DD} or V_{SS}	± 100	mA

Notes:
1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. V_{DD} terminals.
3. All terminals except V_{DD}.

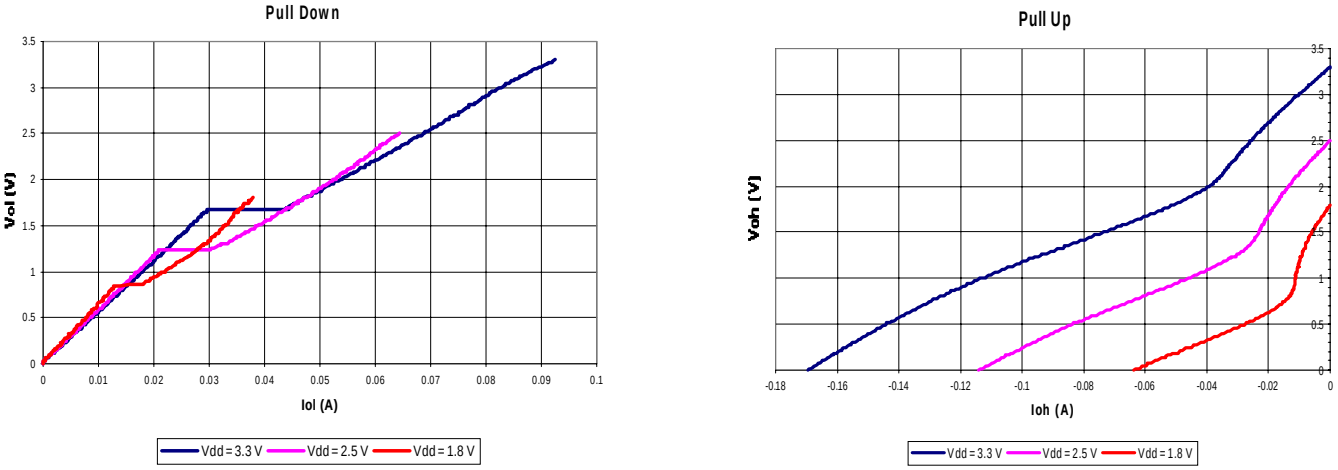


Figure 1. Output Voltage vs. Output Current (T_A = 25°C)

DC Parameters (T_{amb} = - 40° to + 85° C)

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max.	Unit
V_{IH}	HIGH level input voltage	V_{DD} = 1.2V		V_{DD}	-	-	V
		V_{DD} = 1.4V to 1.6V		0.65 x V_{DD}	-	-	V
		V_{DD} = 1.65V to 1.95V		0.65 x V_{DD}	-	-	V
		V_{DD} = 2.3V to 2.7V		1.7	-	-	V
		V_{DD} = 3.0V to 3.6V		2.0	-	-	V
V_{IL}	LOW level input voltage	V_{DD} = 1.2V		-	-	V_{SS}	V
		V_{DD} = 1.4V to 1.6V		-	-	0.35 x V_{DD}	V
		V_{DD} = 1.65V to 1.95V		-	-	0.35 x V_{DD}	V
		V_{DD} = 2.3V to 2.7V		-	-	0.7	V
		V_{DD} = 3.0V to 3.6V		-	-	0.8	V
		1.4V to 3.6V	I_o = -100µA	V_{DD} -0.20			V
V_{OH}[2]	HIGH level output voltage	V_{DD} = 1.4	I_o = -2mA	1.05	-	-	V
		V_{DD} = 1.65V	I_o = -4 mA	1.2	-	-	
		V_{DD} = 2.3V	I_o = -8 mA	1.75	-	-	V
		V_{DD} = 3.0V	I_o = -12 mA	2.3	-	-	V
		1.4V to 3.6V	I_o = 100µA	-	-	0.20	V
V_{OL}[2]	LOW level output voltage	V_{DD} = 1.4V	I_o = 2 mA	-	-	0.4	V
		V_{DD} = 1.65V	I_o = 4 mA	-	-	0.45	V
		V_{DD} = 2.3V	I_o = 8 mA	-	-	0.55	V
		V_{DD} = 3.0V	I_o = 12 mA	-	-	0.70	V
I_I	Input leakage current per pin	V_{DD} = 1.65V to 3.6V	Vin = V_{DD} or V_{SS}	-	-	± 2.5	µA
I_{OFF}	Power off leakage current	V_I or V_o = 3.6V	V_{DD} = 0V	-	-	± 10	µA
I_{DD}	Quiescent supply Current	V_{DD} =3.6V	Vi = V_{DD} or V_{SS} I_O = 0	-	-	40	µA
I_{OZ}	3-state output OFF-state current	V_{DD} = 3.6V	V_O = V_{DD} or V_{SS} V_I ($\overline{OE}$) = V_{DD}	-	0.1	± 12	µA

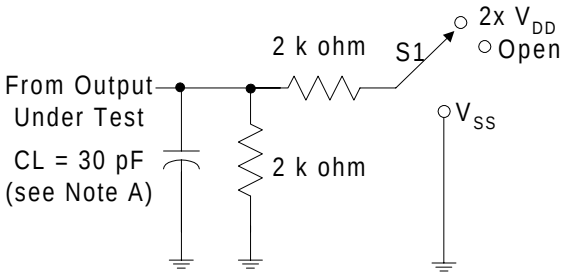
Notes:
1. All typical values are measured at T_{amb} = 25 ° C
2. V_{IN} = V_{IL} or V_{IH}

AC Parameters

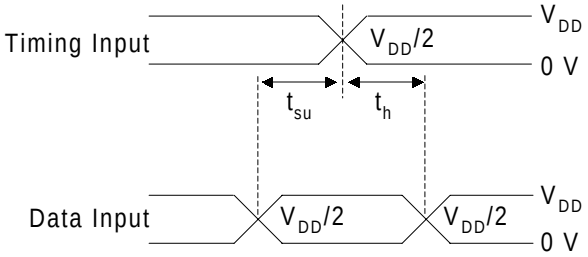
Symbol	Parameter	V_{DD} = 1.2V	V_{DD} =1.5V ± 0.1V		V_{DD} =1.8V ± 0.15V		V_{DD} =2.5V ± 0.2V		V_{DD} =3.3V ± 0.3V		Unit
		Typ[1]	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}/t_{PLH}	Propagation delay nAm to nBm (nBm to nAm)	3.9	0.8	4.0	0.7	3	0.6	1.9	0.5	1.7	ns
t_{PZH}/t_{PZL}	3-State output enable time nOE to nAm, nBm	8.4	1.5	9.2	1.4	7	1	4.3	0.7	3.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nAm, nBm	8.4	2.3	9.3	2.2	7	1.1	4	1.2	3.9	ns

Notes:
1. All typical values are measured at T_{amb} = 25 ° C
2. Typical value is measure at VDD = 1.8V, VDD = 2.5V, VDD = 3.3V.

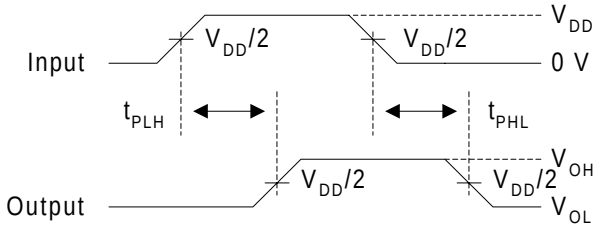
A. Parameter Measurement Information
V_{DD} = 1.2V and 1.5V ± 0.1 V



Load Circuit

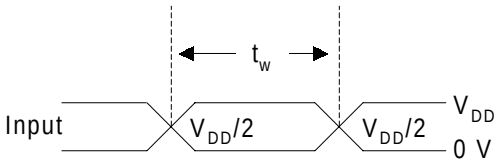


Voltage Waveforms
Setup and Hold Times

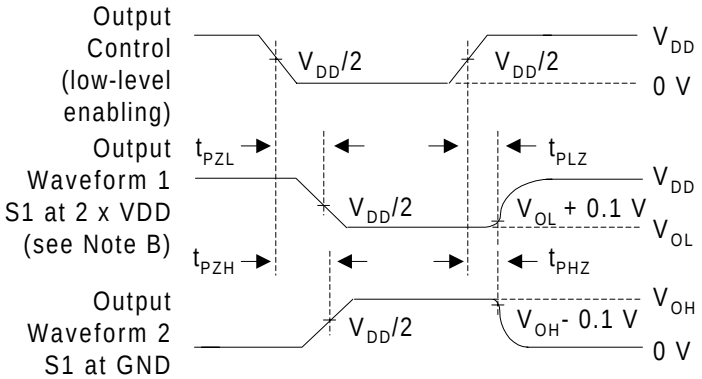


Voltage Waveforms
Propagation Delay Times

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}



Voltage Waveforms
Pulse Duration

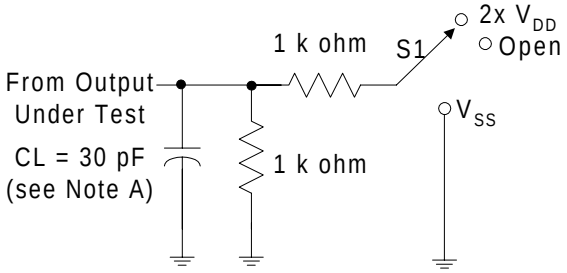


Voltage Waveforms
Enable and Disable Times

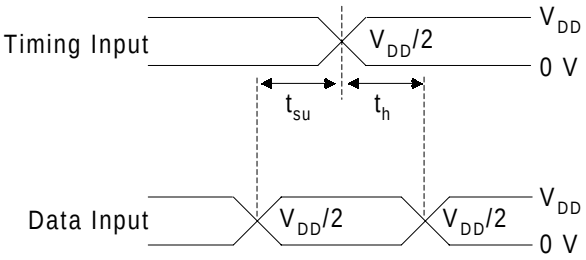
Notes:
A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 nS, t_f ≤ 2nS.
D. The outputs are measured one at a time with on transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

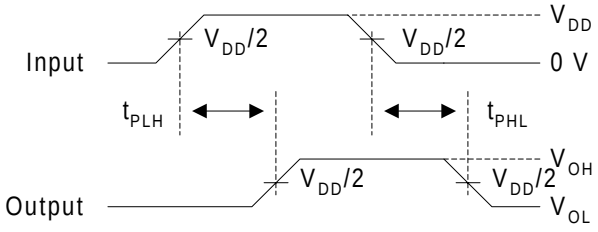
Parameter Measurement Information
V_{DD} = 1.8V ± 0.15 V



Load Circuit

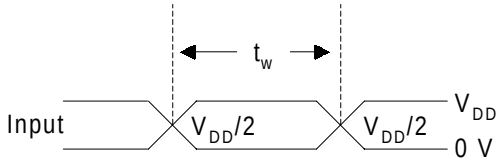


Voltage Waveforms
Setup and Hold Times

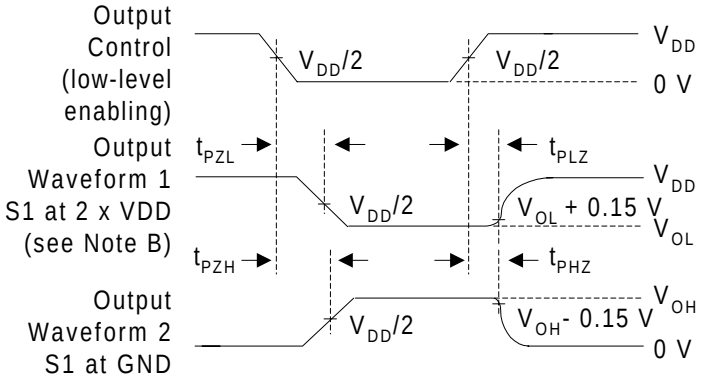


Voltage Waveforms
Propagation Delay Times

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}



Voltage Waveforms
Pulse Duration

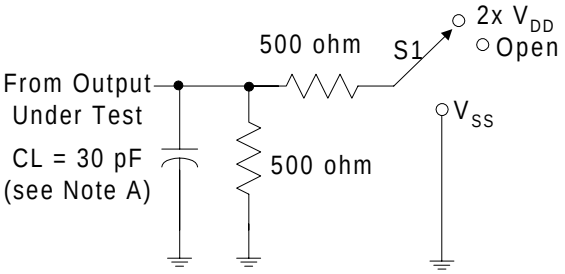


Voltage Waveforms
Enable and Disable Times

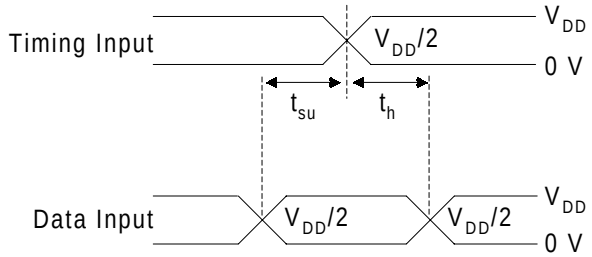
Notes:
A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 nS, t_f ≤ 2nS.
D. The outputs are measured one at a time with on transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

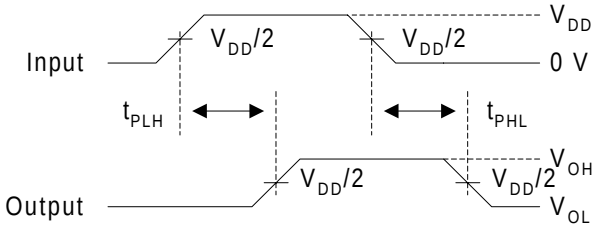
Parameter Measurement Information
V_{DD} = 2.5V ± 0.2 V



Load Circuit

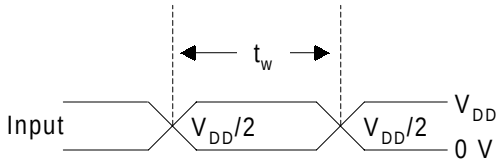


Voltage Waveforms
Setup and Hold Times

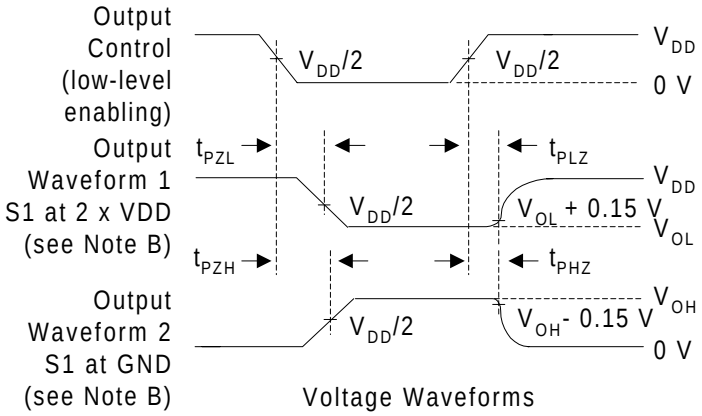


Voltage Waveforms
Propagation Delay Times

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}



Voltage Waveforms
Pulse Duration

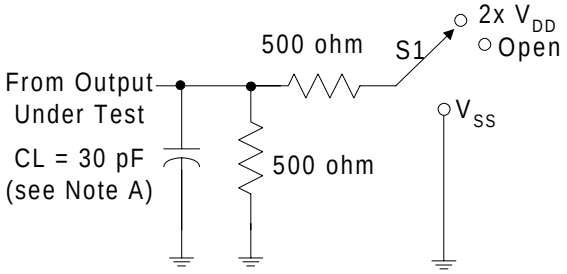


Voltage Waveforms
Enable and Disable Times

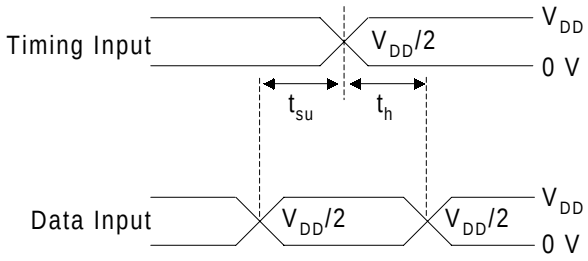
Notes:
A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 nS, t_f ≤ 2.5nS.
D. The outputs are measured one at a time with on transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 4. Load Circuit and Voltage Waveforms

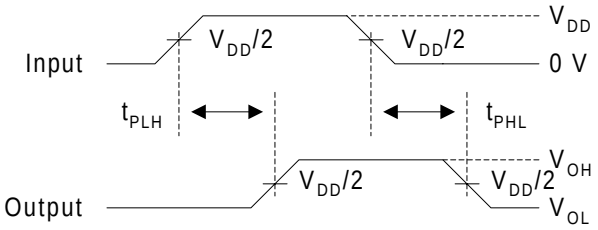
Parameter Measurement Information
V_{DD} = 3.3V ± 0.3 V



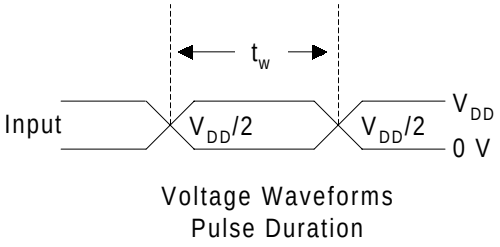
Load Circuit



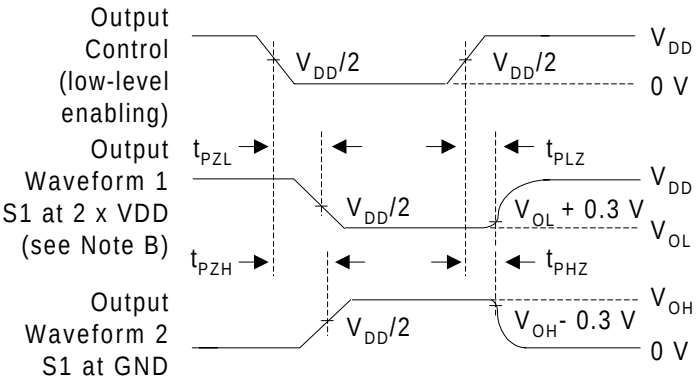
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Pulse Duration



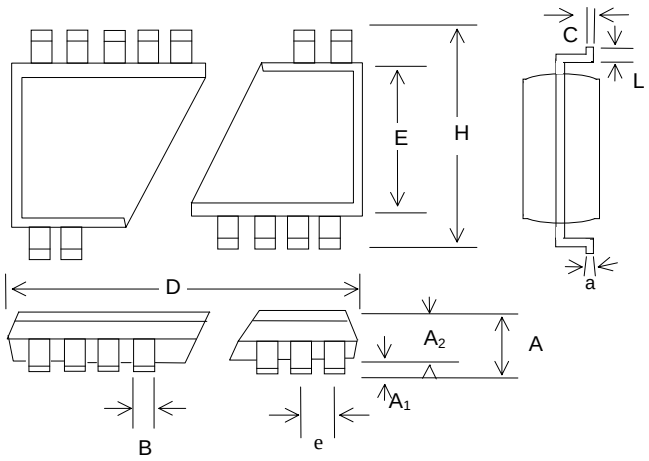
Voltage Waveforms
Enable and Disable Times

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}

Notes:
A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 nS, t_f ≤ 2.5nS.
D. The outputs are measured one at a time with on transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 5. Load Circuit and Voltage Waveforms

Package Drawing and Dimensions



48 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.011	0.17	-	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.488	0.492	0.496	12.40	12.50	12.60
E	0.236	0.240	0.244	6.00	6.10	6.20
e	0.02 BSC			0.50 BSC		
H	0.315	0.319	0.323	8.00	8.10	8.20
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

48 Pin TVSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.005	-	0.009	0.13	-	0.23
C	0.004	-	0.008	0.09	-	0.20
D	0.378	0.382	0.386	9.60	9.70	9.80
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.016 BSC			0.40 BSC		
H		0.252			6.40	
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

Preliminary

Ordering Information

Part Number	Package Type
AVC16245T	48 Pin TSSOP
AVC16245V	48 Pin TVSOP

Note: the ordering part number is formed by a combination of device number, package and screening as shown below.

Marking: Example:

IMI
AVC16245T
Date Code, Lot #

AVC16245T

Package
T = TSSOP
V = TVSOP

IMI Device Number

Notice