Digital satellite radio broadcasting tuner decoder

SAA7501

FEATURES

- Clock recovery
- Differential decoding
- Main frame synchronization
- Swapping half-frames in event of inversion
- Unscrambling
- Demultiplexing
- Subframe synchronization
- Error correction and concealment
- Scale factor decoding with error correction
- Shift into the original values using the scale factors
- Mute in event of synchronization loss.

GENERAL DESCRIPTION

The SAA7501 performs a decoder function for digital satellite sound broadcasting tuners. It is designed to decode one of 16 stereo channels broadcasting audio signals in accordance with the German standard – **Technische Richtlinie ARD/ZDF No. 3R1.**

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.5	V
P_{tot}	total power dissipation	–	500	mW
f_{T20N}	clock frequency	20.48	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7501WP	68	PLCC	plastic	SOT188

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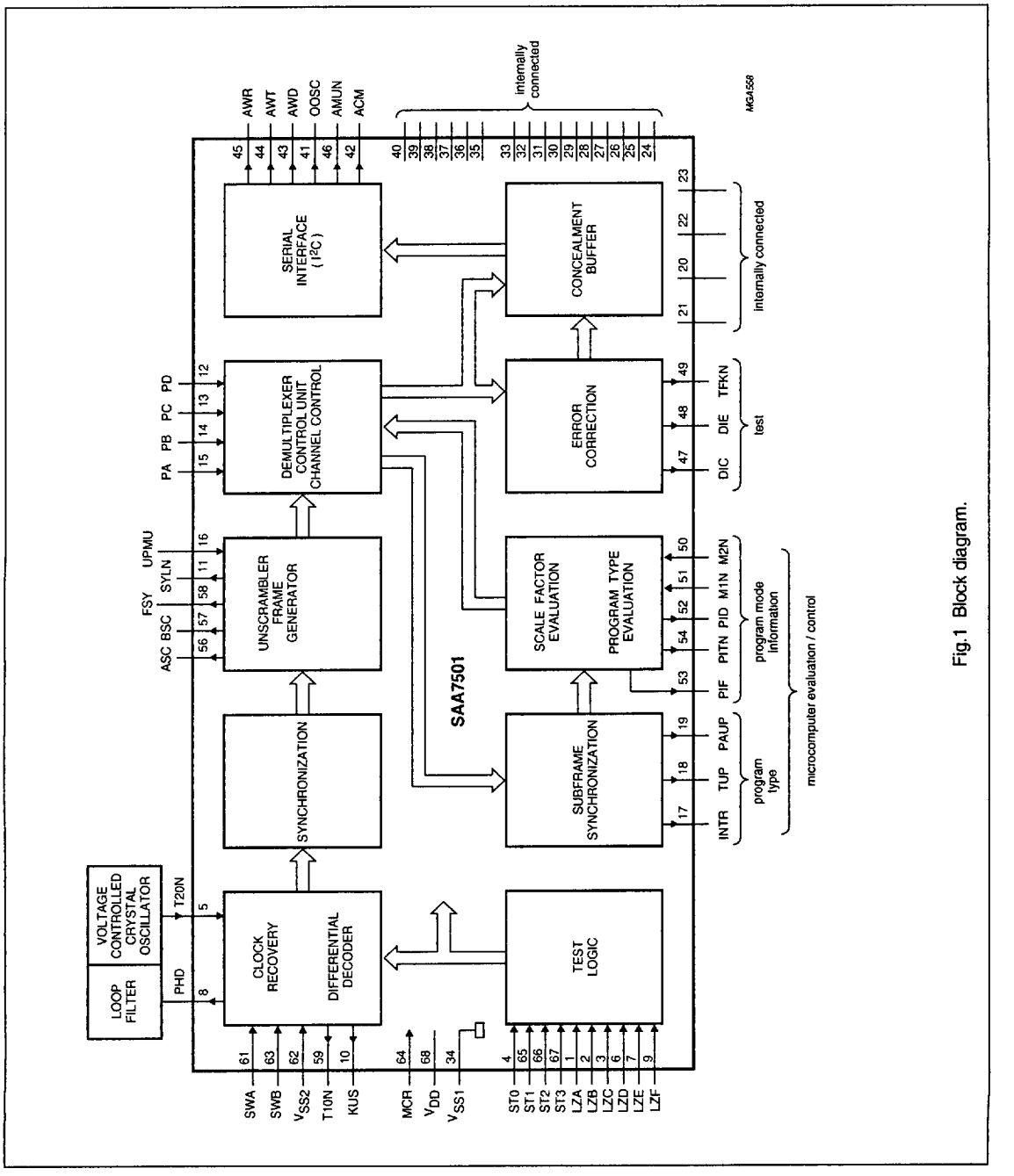

Fig.1 Block diagram.

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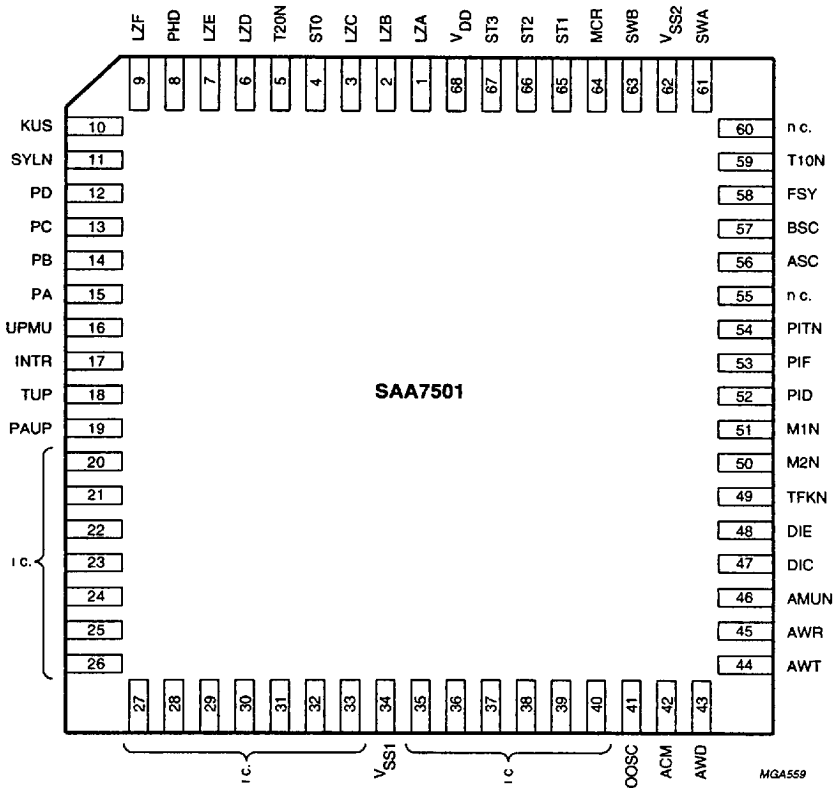

Fig.2 Pin configuration.

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PINNING

SYMBOL	PIN	DESCRIPTION
LZA	1	phase adjustment input for the internal clock (CMOS level with pull-down resistor)
LZB	2	phase adjustment input for the internal clock (CMOS level with pull-down resistor)
LZC	3	phase adjustment input for the internal clock (CMOS level with pull-down resistor)
ST0	4	control input for testing (CMOS level with pull-down resistor)
T20N	5	20.48 MHz clock input from voltage controlled oscillator (CMOS level)
LZD	6	control input for testing (CMOS level with pull-down resistor)
LZE	7	control input for testing (CMOS level with pull-down resistor)
PHD	8	phase control signal output for voltage controlled oscillator
LZF	9	control input for testing (CMOS level with pull-down resistor)
KUS	10	test output; A'B' swap
SYLN	11	synchronization indication flag output
PD	12	program number input selector; MSB (TTL level)
PC	13	program number input selector (TTL level)
PB	14	program number input selector (TTL level)
PA	15	program number input selector; LSB (TTL level)
UPMU	16	mute input; controlled by microcomputer (TTL level)
INTR	17	interrupt flag output for microcomputer
TUP	18	program type interface output for clock
PAUP	19	program type interface output for data
i.c.	20 to 33	internally connected
V_{SS1}	34	ground supply input
i.c.	35 to 40	internally connected
OOSC	41	4.096 MHz clock output
ACM	42	concealment flag output for SAA7220P/C
AWD	43	audio data output for SAA7220P/C
AWT	44	bit clock output for SAA7220P/C
AWR	45	word select signal output for SAA7220P/C
AMUN	46	mute signal output for SAA7220P/C
DIC	47	data output for testing
DIE	48	data output for testing
TFKN	49	burst clock output for test data
M2N	50	channel mode select input (TTL level)
M1N	51	channel mode select input (TTL level)
PID	52	program information (PI) interface output for data
PIF	53	program information (PI) interface output for window signal
PITN	54	program information (PI) interface output for clock
n.c.	55	not connected
ASC	56	data output for 10.24 Mbit/s interface
BSC	57	data output for 10.24 Mbit/s interface

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SYMBOL	PIN	DESCRIPTION
FSY	58	window signal output for 10.24 Mbit/s interface
T10N	59	10.24 MHz clock output
n.c.	60	not connected
SWA	61	10.24 Mbit/s data input (TTL level)
V_{SS2}	62	screen ground input
SWB	63	10.24 Mbit/s data input (TTL level)
MCR	64	master reset input (CMOS level)
ST1	65	control input for testing (CMOS level with pull-down resistor)
ST2	66	control input for testing (CMOS level with pull-down resistor)
ST3	67	control input for testing and mode select for 10.24 Mbit/s interface (CMOS level with pull-down resistor)
V_{DD}	68	power supply input

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FUNCTIONAL DESCRIPTION

General

The SAA7501 has been designed to decode 16 stereo channel sound broadcasting signals in accordance with the German standard – **Technische Richtlinie ARD/ZDF No. 3R1.** The channel carrying the sound broadcast program is selected and converted into an intermediate frequency by a front end. The signal is then amplified and demodulated {4 PSK (Phase Shift Keying) with carrier recovery}. The outputs from the demodulator are two differential coded signals that are input to the SAA7501. The SAA7501 decoder outputs the audio data, of the selected stereo or mono channel, as linear quantized 16-bit audio samples.

Selection of the desired audio channel, and stereo or mono mode, is controlled by inputs PA, PB, PC and PD. These inputs may be driven directly by switches or controlled by a microcomputer.

When under the control of a microcomputer, the SAA7501 transmits serial data to the microcomputer on the type of program (16 stereo or 32 mono). The corresponding synchronization of the subframe is partly performed by the SAA7501 (every 2 ms) and at a higher level by the microcomputer (every 16 ms). The SAA7501 also sends to the microcomputer, program information code data together with its clock and window signal.

The circuit automatically performs the system error correction and concealment. In the transmit error rate range of 0 to 3×10^{-3} a theoretical C/N (carrier-to-noise ratio) gain of approximately 6 dB is obtained. The residual error rate is almost zero for transmit error rates $\leq 3 \times 10^{-4}$.

The remaining functions, such as clock recovery, main and subframe synchronization and scale factor decoding, are protected in a similar manner so that they will not influence the residual error rate.

Clock recovery

The baseband signals A' and B' are connected to the SWA and SWB inputs of the SAA7501. For clock recovery, the phase of the incoming data streams is compared with T10N (half the oscillator frequency). The output of the phase comparator (PHD) controls, by means of the loop filter, the voltage controlled oscillator (both are external to the IC) and thus its output signal T20N.

For energy dispersal, for example, in modulation pauses or with constant signals, the data streams are scrambled during generation. The exceptions are the synchronization words and the special service bits. In order that the phase correspondence between the recovered system clock (T10N) and the input signals A' and B' can be adjusted to a minimum bit error rate (BER), a programmable phase shifter is provided (inputs LZA, LZB, LZC and ST3).

The differential decoder logic delivers the original data streams which may be exchanged depending on the number of mixer stages on the transmission channel. The polarity of the two synchronization words will indicate if this is necessary, if so the two data streams will be automatically switched over.

Synchronization

Using the synchronization circuit, the incoming data streams are first searched for 11-bit Barker code words. The synchronization circuit permits two errors for both synchronization words, which guards against failure of the synchronization word. If the synchronization word has been detected, the following data is examined at frame length intervals to see if the synchronization word is repeated. If it is repeated, it is acknowledged as a synchronization word (window check) and an internal frame pulse generator takes over further control. There is also a synchronization word failure control which initiates a renewed synchronization word search and mutes the AF output if four successive synchronization word failures occur.

To enhance the performance the result from the error correction circuit is used as an additional input to the synchronization circuit. This is to avoid extra errors through synchronization loss in the event of relative high, but for reception acceptable, bit error rates. This will not affect the rapid detection of a very high bit error rate or the non-synchronization of the data stream. The decoder will function correctly with a bit error rate up to 3×10^{-3}.

Demultiplexer

After synchronization, the beginning of a frame is marked and the digital signals are defined as to their assignment. First the non-scrambled special service bit from the half-frame A is taken out. The rest of both half-frames are unscrambled and demultiplexed so that each half-frame is split into two substreams with a rate of 5.12 Mbit/s (see Technische Richtlinie ARD/ZDF Nr. 3R1, main frame specification). Using the inputs from the synchronization circuit and the program selector (inputs

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PA, PB, PC and PD) the demultiplexer locks on to the selected program block and generates all the control signals required for further signal processing.

Error correction

The error correction circuit provides for exact identification of two errors in a 63/44 BCH block and correction of the incorrect bits. In the event of more than two errors the identification circuit can identify incorrect BCH blocks with up to five errors.

The BCH block is operated on by a syndrome calculator, the result controls the lines of an error correction matrix. The output of this matrix corrects (inverts) the incorrect bits when data is shifted out from its buffer. The BCH block is then fed through a second syndrome calculator. In the event of more than two errors the result of the whole calculation will be other than zero. This information provides the concealment in the next stages.

The two adjacent samples related to the detected incorrect sample are added and divided by two, the result replaces the incorrect sample (interpolation). In the event of successive bad samples the last corrected sample is held until a good sample is detected (hold function). A high error frequency in the event of synchronization loss will activate the muting function and set the output data to zero.

This information, if concealment is not active, is used in the synchronization circuit as described in that section. When the samples are correct it can be assumed that the synchronization is also correct.

Scale factor, program type evaluation and shift function

The transmitted samples are returned to their original range of values by the scale factor, which is obtained by decoding the ZI-subframe. The start of this frame is coupled to the start of the special services frame, synchronization for this frame uses the same principle as for the main frame. In the scale factor evaluation unit the BCH 14/6 code words (transmitted three times) are fed into a majority selection circuit operating at bit level. Subsequently the error check and the correction of a maximum of two errors is carried out.

The SAA7501 contains the synchronization word detection and error check for the subframe synchronization word with its repetition time of 2 ms. The program type evaluation with its superior synchronization has to be performed external to the chip, for example, by a microcomputer. For this purpose data is available in 8-bit blocks at a serial interface (INTR, PAUP and TUP; block rate = 4000/s). The same microcomputer can also perform the program selection (inputs PA, PB, PC and PD).

At the input to the concealment buffer the corrected 11 bits (MSB) are combined with the 3 unprotected transmitted bits (LSB). The scale factor determines the required shift-back operations required to convert the transmitted values back into the original values. Voids that occur are filled with noughts or ones corresponding to the sign bit. The shift-back and filling of voids ensures that no incorrect bits occur above the range defined by the scale factor. The upper 16 bits represent the regenerated audio sample.

Digital-to-analog conversion and interfaces

The SAA7501 enables different DAC systems to be used. For control of the SAA7220P/C and TDA1541 a 2.5 external divider must be connected to the 20.48 MHz clock signal to produce the required 8.192 MHz clock signal.

A serial interface is built in with the following outputs: bit clock (AWT), word select (AWR) and audio data (AWD). In addition the mute signal (AMUN) and the concealment flag (ACM) are also available. The SAA7220P/C and TDA1541 are equipped with a digital audio interface for domestic use equivalent to 'IEC proposal No. 84 (secretariat 28; from June 1985)'.

Additional information, including the scale factor is available through the program information (PI) interface (PID, PITN and PIF). Another interface, using the ASC, BSC and T10N outputs, makes available signals from the differential decoder. These signals are used for bit error measurement and an optimized phase adjustment of the internal clock (refer to **Clock recovery** section).

An optional application of the control signals for mute and concealment operations is possible using the outputs AMUN and ACM. For the mute signal a different time relationship to the unwanted pulse with very low C/N values may be obtained.

The external application of the concealment signal is recommended; if an additional interpolation is required between additional samples with different levels in the external circuitry (such as the SAA7220P/C).

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Truth tables

Table 1 Delay adjustment (pins 1 to 3).

LZC	LZB	LZA	DELAY
0	0	0	4 x τ
0	0	1	3 x τ
0	1	0	2 x τ
0	1	1	1 x τ
1	0	0	0 x τ
1	0	1	−1 x τ
1	1	0	−2 x τ
1	1	1	−3 x τ

Where: τ ≈ 1.5 x gate delay time (NAND).

Table 2 Master reset (pin 64).

MCR	FUNCTION
0	operation
1	master reset

Table 3 Mute (pin 16).

UPMU	FUNCTION
0	no
1	yes

Table 4 Program number (pins 12 to 15).

PD	PC	PB	PA	PROGRAM NUMBER
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
.	.	.	.	.
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Table 5 Phase control signal (pin 8).

PHD	PHASE
0	lead phase
1	lag phase

Table 6 Synchronization indication (pin 11).

SYLN	SYNCHRONIZATION
0	yes
1	no

Table 7 Mode select for data outputs ASC and BSC for 10.24 Mbit/s interface (pin 67).

ST3	DATA ASC/BSC
0	after unscrambler
1	before unscrambler

Table 8 Channel mode select (pins 50 and 51).

M2N	M1N	CHANNEL MODE
0	0	mono (1 + 2)
0	1	mono R (2)
1	0	mono L (1)
1	1	stereo

Table 9 Concealment (pin 42).

ACM	FUNCTION
0	no
1	yes

Table 10 Mute (pin 46)

AMUN	MUTE
0	yes
1	no

Table 11 Interrupt (pin 47)

INTR	INTERRUPT
0	no
1	yes

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LIMITING VALUES

In accordance with the Absolute Rating Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	7.0	V
V_I	input voltage (note 1)	−0.5	V_{DD} +0.5	V
I_I	input current	–	±10	mA
I_O	output current	–	±10	mA
I_{SS}	supply current in V_{SS}	–	28	mA
I_{DD}	supply current in V_{DD}	–	28	mA
P_{tot}	total power dissipation	–	500	mW
T_{amb}	operating ambient temperature	−25	+85	°C
T_{stg}	storage temperature	−55	+150	°C

Note

1. V_{DD} +0.5 must not exceed 7 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see Handling MOS Devices).

The PLCC-68 package can only be guaranteed with soldering temperatures up to a maximum of 235 °C.

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DC CHARACTERISTICS

T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.5	–	5.5	V
I_{DD}	supply current		–	12.5	–	mA
I_{DDq}	quiescent supply current	note 1	–	–	50	µA
Inputs (CMOS level)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_{IL}	LOW level input current	note 2	–	–	–10	µA
I_{IH}	HIGH level input current	note 2	–	–	10	µA
Inputs (TTL level)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2	–	–	V
I_{IL}	LOW level input current	note 2	–	–	–10	µA
I_{IH}	HIGH level input current	note 2	–	–	10	µA
Inputs (CMOS level with pull-down resistor)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
R_I	pull-down resistor		25	50	100	kΩ
Outputs						
V_{OL}	LOW level output voltage	I_{OL} = –1 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = 1 mA	4.0	–	–	V

Notes

1. T_{amb} = 25 °c; all inputs at V_{SS} or V_{DD}; all outputs open-circuit.
2. At 25 °C maximum 1 µA.

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AC CHARACTERISTICS

T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T20N clock pulse (see Fig.3)						
t_{WH}	pulse width HIGH		15	20	–	ns
t_{WL}	pulse width LOW		15	22	–	ns
t_{P20}	T20N pulse period		48	48.8	–	ns
Data input timing (see Fig.4)						
t_{SWL}	set-up time for data SWA and SWB to T10N	note 1	–	50	–	ns
t_{P10}	T10N pulse period t_{PSW}	note 2	–	97.6	–	ns
Main frame timing (see Fig.5)						
t_{SYNC}	main frame sync pulse		–	$11t_{P10}$	–	ns
I²S timing (see Fig.6)						
f_{AWT}	frequency AWT signal		–	1.024	–	MHz
t_{SAMP}	audio sample repetition time		–	31.25	–	µs
PI interface timing (see Fig.7)						
f_{PITN}	frequency PTIN signal		–	32	–	kHz
t_{PITN}	PTIN pulse period		–	31.25	–	µs
t_{PIFH}	PIF pulse width HIGH		–	$22t_{PITN}$	–	µs
t_{ZI}	PIF pulse period		–	2	–	ms
Output timing Program type interface (see Fig.8)						
t_{INTR}	INTR pulse period		–	250	–	µs
t_{PINH}	INTR pulse width HIGH		–	31.25	–	µs

Notes

1. Due to noise, the period t_{SWL} may occasionally vary between 30 and 70 ns.
2. Due to noise, the period t_{PSW} may occasionally vary between 77.6 and 117.6 ns.

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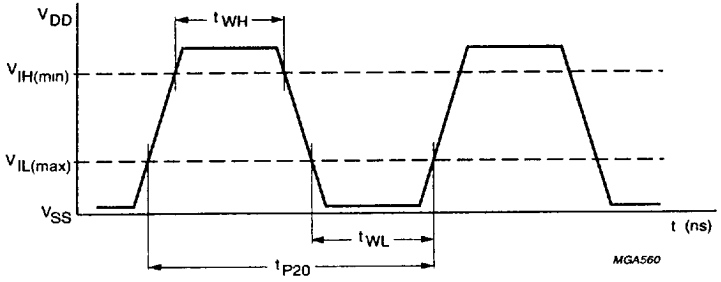

Fig.3 Waveform at clock input T20N (pin 5).

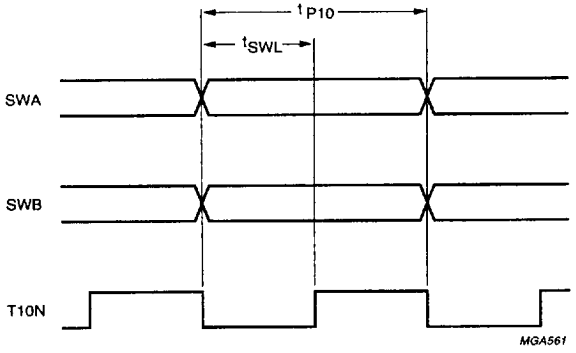

Fig.4 Data input timing (pins 59, 61 and 63).

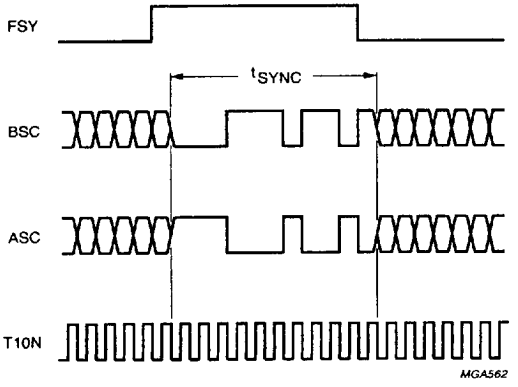

Fig.5 Output timing for 10.24 Mbit/s interface (pins 56, 57, 58 and 59).

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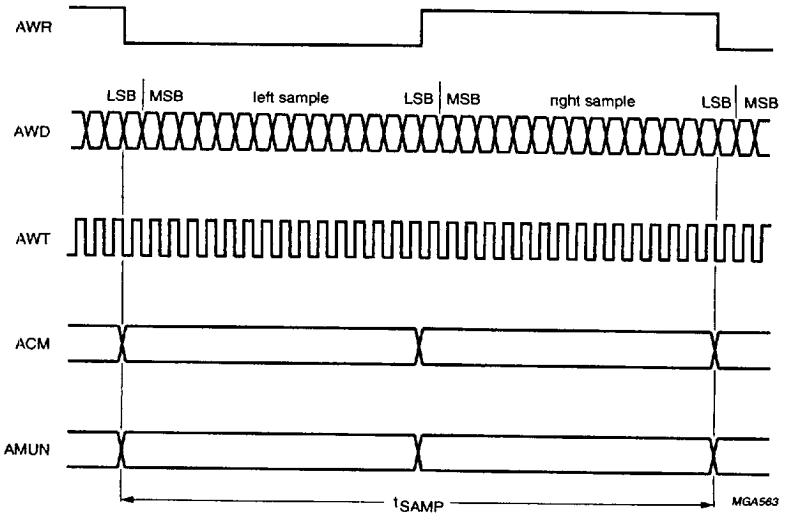

Fig.6 Inter-IC Sound (I²S) timing and mute and interpolation flags (pins 42 to 46).

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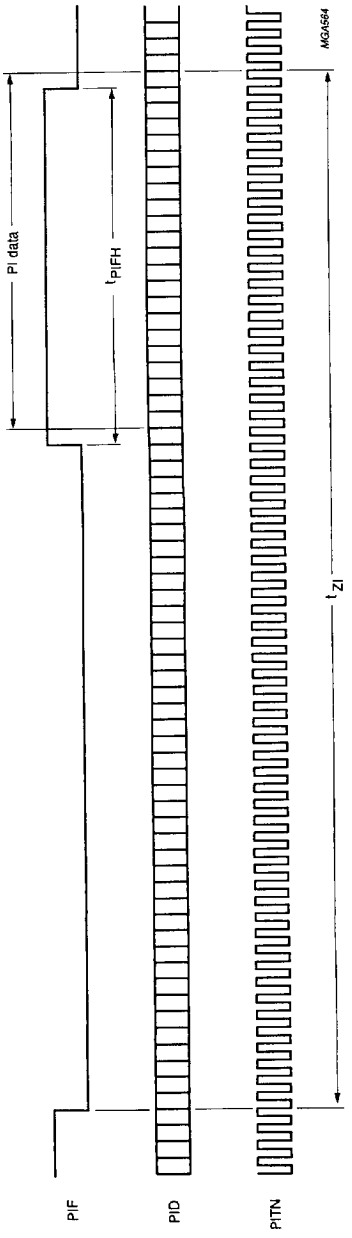

Fig.7 PI interface timing (pins 52 to 54).

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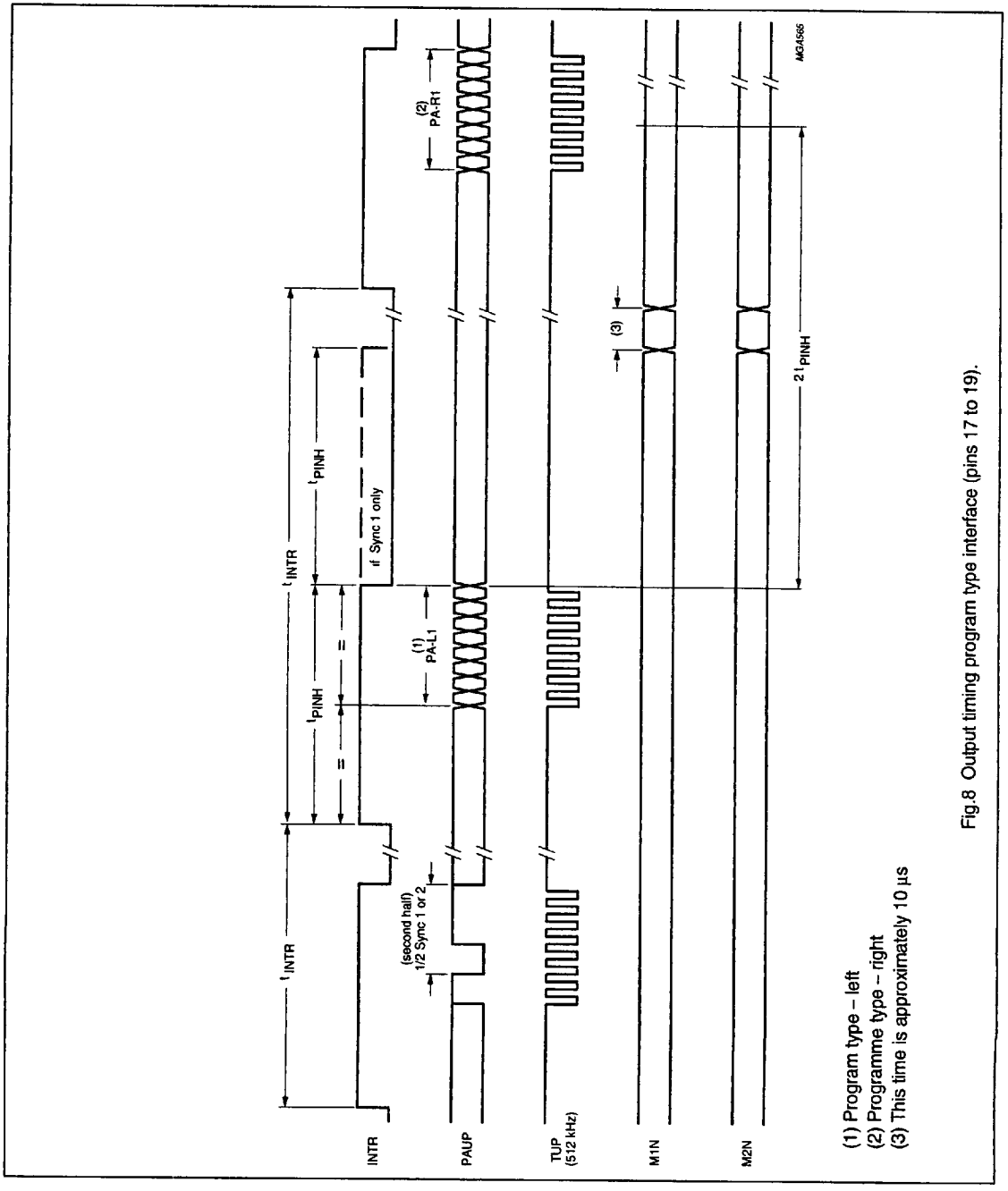

Fig.8 Output timing program type interface (pins 17 to 19).

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APPLICATION INFORMATION

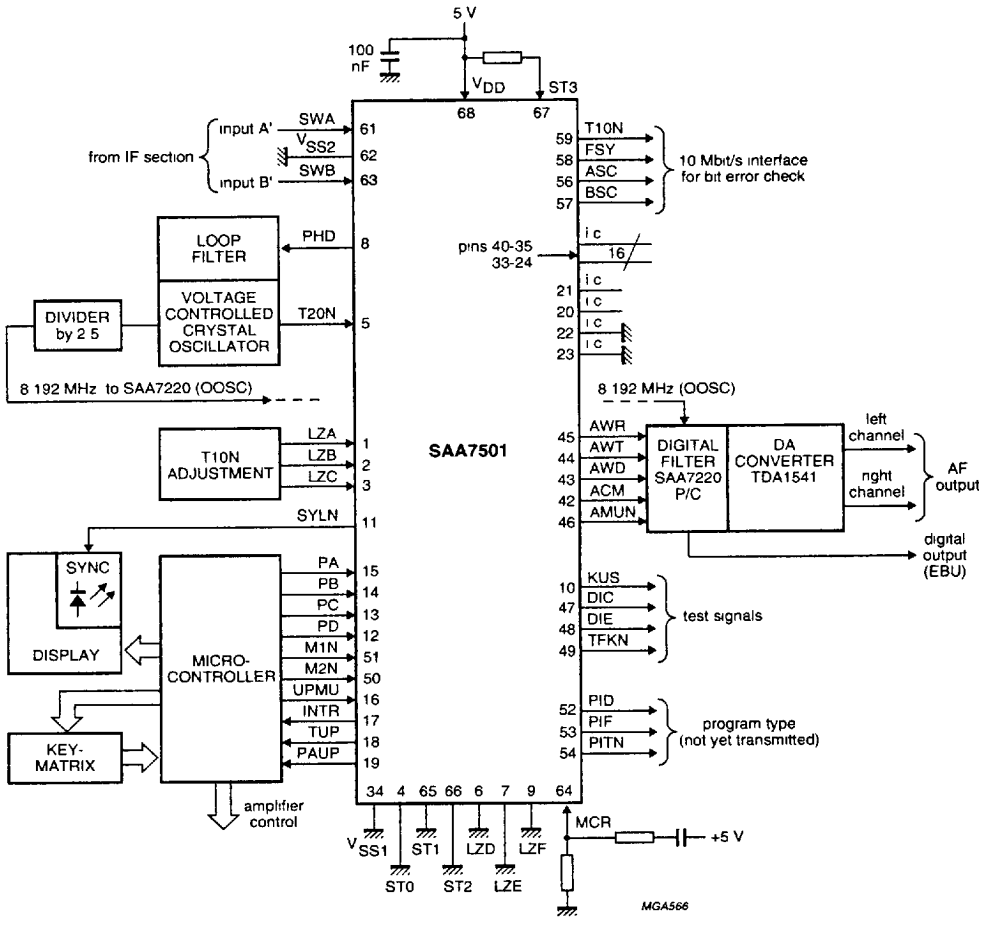

Fig.9 Application diagram.

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