Clock signal generator circuit for Digital TV systems (CGC)

SAA9057B

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5, LL3 and LL3T (4th and 2nd multiples of input frequency)
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	40	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.25	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.4	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA9057B generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, adventageous for a digital TV system based on display standard conversion concepts.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9057B	20	DIL	plastic	SOT146
SAA9057BT	20	mini-pack (SO20)	plastic	SOT163A

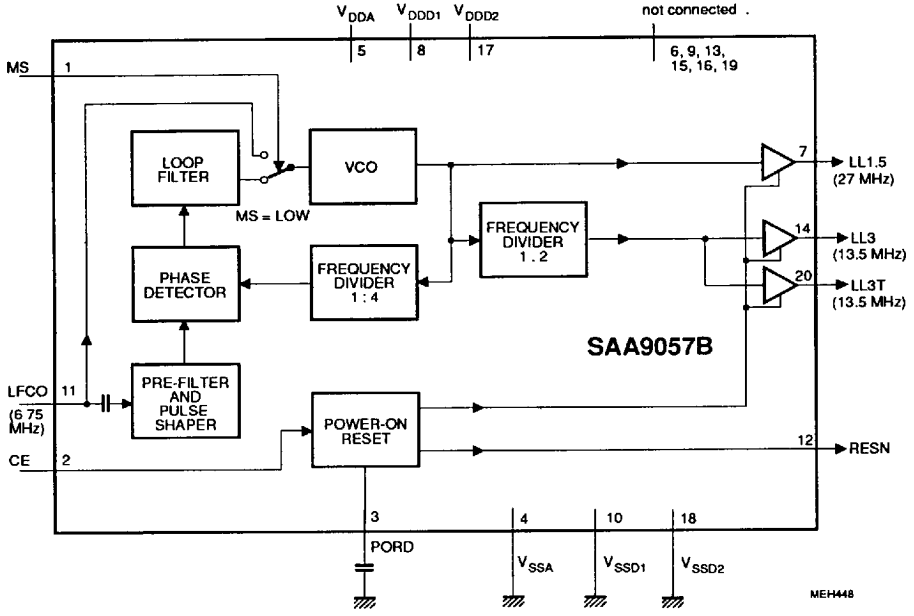

Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA9057B generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO, coming from SAA 9051, is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5 (pin7). 13.5 MHz frequency is also generated by 1:2 divider and output on LL3 and LL3T (pins 14 and 20).
The rectangular output signals have 50 % duty factor.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. MS function is not tested.

Chip enable CE

The buffer outputs are enabled and power-on reset is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuit of this digital TV system.
The LFCO input signal has to be applied before RESN becomes HIGH.

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PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
n.c.	6	not connected
LL1.5	7	line-locked clock output signal (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
n.c.	9	not connected
V_{SSD1}	10	digital ground 1 (0 V)
LFCO	11	line-locked input frequency
RESN	12	reset output (active-LOW)
n.c.	13	not connected
LL3	14	line-locked clock output signal (2 times f_{LFCO})
n.c.	15	not connected
n.c.	16	not connected
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD2}	18	digital ground 2 (0 V)
n.c.	19	not connected
LL3T	20	line-locked clock output signal (2 times f_{LFCO})

PIN CONFIGURATION

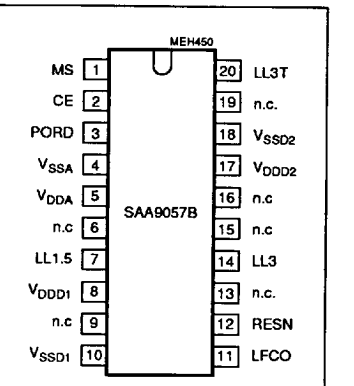

Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	tbf	V

* Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 6.25$ to 7.25 MHz and $T_{amb} = 0$ to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	40	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.25	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS and CE (pins 1 and 2)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
I_{LI}	input leakage current		-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.4	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	-	V_{DDD}	V
I_{LI}	output leakage current		-	-	±10	µA
t_d	RESN delay time	$C_3 = 0.1$µF; Fig.4	20	-	200	ms
Output signals LL1.5, LL3 and LL3T (pins 7, 14 and 20)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	-	V_{DDD}	V
I_{LI}	output leakage current	high-impedance	-	-	±10	µA
t_{comp}	composite rise time	note 1; note 2	-	-	9	ns
f_{LL}	output frequency LL1.5	Figures 3 and 6	-	4 f_{LFCO}	-	MHz
	output frequency LL3		-	2 f_{LFCO}	-	MHz
	output frequency LL3T		-	2 f_{LFCO}	-	MHz
t_{LL}	duty factor LL1.5	note 1; Fig.3	40	50	60	%
	duty factor LL3 and LL3T	note 1; Fig.3	43	50	57	%
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	6	ns

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF. VSSA and VSSD short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V.
3. MS function is not tested.

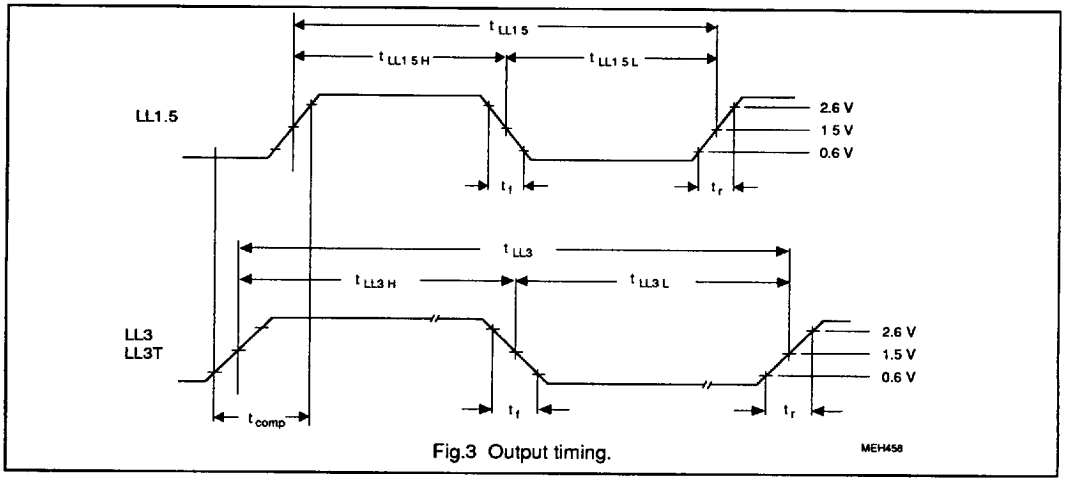

Fig.3 Output timing.

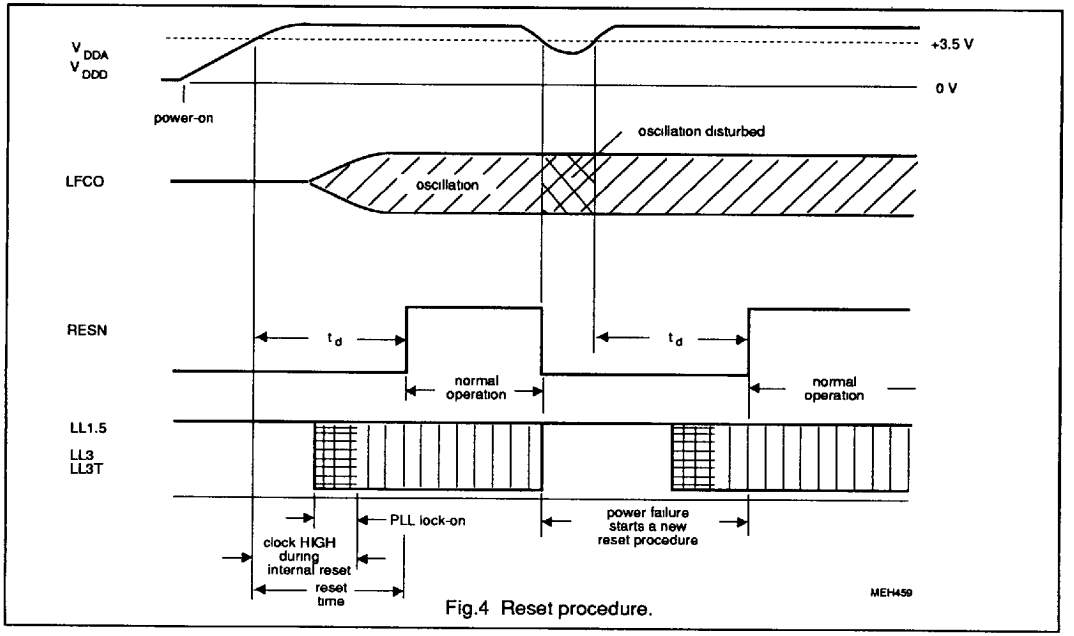

Fig.4 Reset procedure.