CMOS single-chip 8-bit microcontroller

80C31/80C51/87C51

DESCRIPTION

The Philips 80C31/80C51/87C51 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC51 is functionally compatible with the NMOS 8031/8051 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

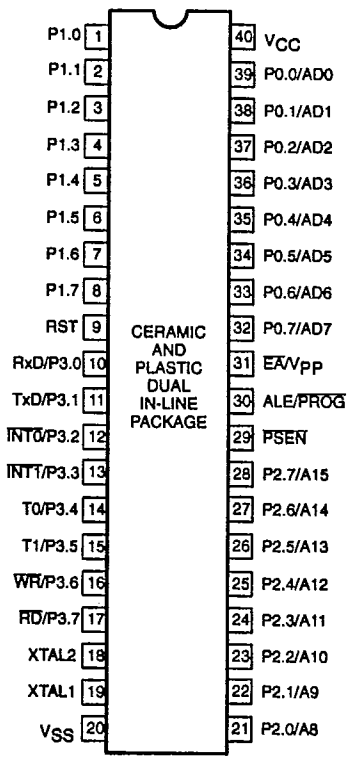
The 8XC51 contains a 4k × 8 ROM (80C51) EPROM (87C51), a 128 × 8 RAM, 32 I/O lines, two 16-bit counter/timers, a five-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

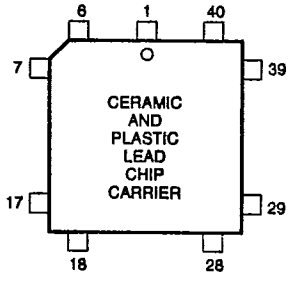
In addition, the device has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

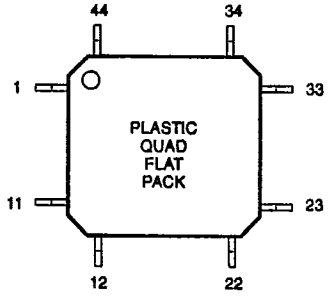
FEATURES

- 8031/8051 compatible
  - 4k × 8 ROM (80C51)
  - 4k × 8 EPROM (87C51)
  - ROMless (80C31)
  - 128 × 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Five speed ranges at V_{CC} = 5V
  - 12MHz
  - 16MHz
  - 24MHz
  - 30MHz
  - 33MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATIONS







SEE PAGE 138 FOR QFP AND LCC PIN FUNCTIONS.

ORDERING INFORMATION

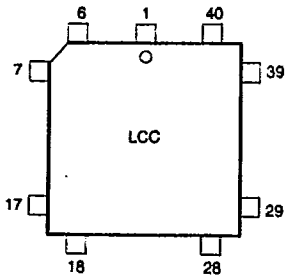
EPROM	DRAWING NUMBER	PHILIPS NORTH AMERICA				
		ROMless	ROM	DRAWING NUMBER	TEMPERATURE RANGE °C AND PACKAGE[1]	Freq MHz
SC87C51CCF40	0590B				0 to +70, Ceramic Dual In-line Package, UV	3.5 to 12
SC87C51CCK44	1472A				0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 12
SC87C51CCN40	0415C	SC80C31BCCN40	SC80C51BCCN40	0415C	0 to +70, Plastic Dual In-line Package, OTP	3.5 to 12
SC87C51CCA44	0403G	SC80C31BCCA44	SC80C51BCCA44	0403G	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 12
SC87C51CCB44	1118D	SC80C31BCCB44	SC80C51BCCB44	1118D	0 to +70, Plastic Quad Flat Pack, OTP	3.5 to 12
SC87C51ACF40	0590B				–40 to +85, Ceramic Dual In-line Package, UV	3.5 to 12
SC87C51ACK44	1472A				–40 to +85, Ceramic Leaded Chip Carrier, UV	3.5 to 12
SC87C51ACN40	0415C	SC80C31BACN40	SC80C51BACN40	0415C	–40 to +85, Plastic Dual In-line Package, OTP	3.5 to 12
SC87C51ACA44	0403G	SC80C31BACA44	SC80C51BACA44	0403G	–40 to +85, Plastic Leaded Chip Carrier, OTP	3.5 to 12
SC87C51CGF40	0590B				0 to +70, Ceramic Dual In-line Package, UV	3.5 to 16
SC87C51CGK44	1472A				0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 16
SC87C51CGN40	0415C	SC80C31BCGN40	SC80C51BCGN40	0415C	0 to +70, Plastic Dual In-line Package, OTP	3.5 to 16
SC87C51CGA44	0403G	SC80C31BCGA44	SC80C51BCGA44	0403G	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 16
SC87C51CGB44	1118D	SC80C31BCGB44	SC80C51BCGB44	1118D	0 to +70, Plastic Quad Flat Pack, OTP	3.5 to 16
SC87C51AGF40	0590B				–40 to +85, Ceramic Dual In-line Package, UV	3.5 to 16
SC87C51AGK44	1472A				–40 to +85, Ceramic Leaded Chip Carrier, UV	3.5 to 16
SC87C51AGN40	0415C	SC80C31BAGN40	SC80C51BAGN40	0415C	–40 to +85, Plastic Dual In-line Package, OTP	3.5 to 16
SC87C51AGA44	0403G	SC80C31BAGA44	SC80C51BAGA44	0403G	–40 to +85, Plastic Leaded Chip Carrier, OTP	3.5 to 16
SC87C51CPF40	0590B				0 to +70, Ceramic Dual In-line Package, UV	3.5 to 24
SC87C51CPK44	1472A				0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 24
SC87C51CPN40	0415C	SC80C31BCPN40	SC80C51BCPN40	0415C	0 to +70, Plastic Dual In-line Package, OTP	3.5 to 24
SC87C51CPA44	0403G	SC80C31BCPA44	SC80C51BCPA44	0403G	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 24
SC87C51APF40	0590B				–40 to +85, Ceramic Dual In-line Package, UV	
SC87C51APK44	1472A				–40 to +85, Ceramic Leaded Chip Carrier, UV	3.5 to 24
SC87C51APN40	0415C	SC80C31BAPN40	SC80C51BAPN40	0415C	–40 to +85, Plastic Dual In-line Package, OTP	3.5 to 24
SC87C51APA44	0403G	SC80C31BAPA44	SC80C51BAPA44	0403G	–40 to +85, Plastic Leaded Chip Carrier, OTP	3.5 to 24
SC87C51CYF40	0590B				0 to +70, Ceramic Dual In-line Package, UV	3.5 to 33
SC87C51CYK44	1427A				0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 33
SC87C51CYN40	0415C	SC80C31BCYN40	SC80C51BCYN40	0415C	0 to +70, Plastic Dual In-line Package, OTP	3.5 to 33
SC87C51CYA44	0403G	SC80C31BCYA44	SC80C51BCYA44	0403G	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 33
SC87C51AYF40	0590B				–40 to +85, Ceramic Dual In-line Package, UV	3.5 to 33
SC87C51AYK44	1472A				–40 to +85, Ceramic Leaded Chip Carrier, UV	3.5 to 33
SC87C51AYN40	0415C	SC80C31BAYN40	SC80C51BAYN40	0415C	–40 to +85, Plastic Dual In-line Package, OTP	3.5 to 33
SC87C51AYA44	0403G	SC80C31BAYA44	SC80C51BAYA44	0403G	–40 to +85, Plastic Leaded Chip Carrier, OTP	3.5 to 33

1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM
2. SOT311 replaced by SOT307-2.

ORDERING INFORMATION

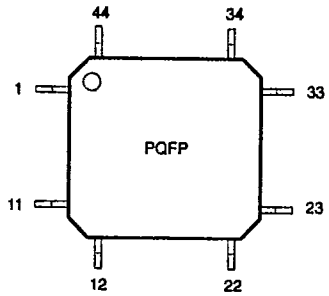
PHILIPS					
ROMless (ORDER NUMBER)	ROMless (MARKING NUMBER)	ROM	DRAWING NUMBER	TEMPERATURE RANGE °C AND PACKAGE[1]	Freq MHz
PCB80C31-2 N	PCB80C31BH2-12P	PCB80C51BH-2P	SOT129	0 to +70, Plastic Dual In-line Package, OTP	0.5 to 12
PCB80C31-2 A	PCB80C31BH2-12WP	PCB80C51BH-2WP	SOT187	0 to +70, Plastic Leaded Chip Carrier, OTP	0.5 to 12
	PCB80C31BH2-12H	PCB80C51BH-2H	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack, OTP	0.5 to 12
PCB80C31-3 N	PCB80C31BH3-16P	PCB80C51BH-3P	SOT129	0 to +70, Plastic Dual In-line Package, OTP	1.2 to 16
PCB80C31-3 A	PCB80C31BH3-16WP	PCB80C51BH-3WP	SOT187	0 to +70, Plastic Leaded Chip Carrier, OTP	1.2 to 16
	PCB80C31BH3-16H	PCB80C51BH-3H	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack, OTP	1.2 to 16
PCF80C31-3 N	PCF80C31BH3-16P	PCF80C51BH-3P	SOT129	–40 to +85, Plastic Dual In-line Package, OTP	1.2 to 16
PCF80C31-3 A	PCF80C31BH3-16WP	PCF80C51BH-3WP	SOT187	–40 to +85, Plastic Leaded Chip Carrier, OTP	1.2 to 16
	PCF80C31BH3-16H	PCF80C51BH-3H	SOT307-2[2]	–40 to +85, Plastic Quad Flat Pack, OTP	1.2 to 16
	PCA80C31BH3-16P	PCA80C51BH-3P	SOT129	–40 to +125, Plastic Dual In-line Package	1.2 to 16
	PCA80C31BH3-16WP	PCA80C51BH-3WP	SOT187	–40 to +125, Plastic Leaded Chip Carrier	1.2 to 16
PCB80C31-4 N	PCB80C31BH4-24P	PCB80C51BH-4P	SOT129	0 to +70, Plastic Dual In-line Package, OTP	1.2 to 24
PCB80C31-4 A	PCB80C31BH4-24WP	PCB80C51BH-4WP	SOT187	0 to +70, Plastic Leaded Chip Carrier, OTP	1.2 to 24
	PCB80C31BH4-24H	PCB80C51BH-4H	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack, OTP	1.2 to 24
PCF80C31-4 N	PCF80C31BH4-24P	PCF80C51BH-4P	SOT129	–40 to +85, Plastic Dual In-line Package, OTP	1.2 to 24
PCF80C31-4 A	PCF80C31BH4-24WP	PCF80C51BH-4WP	SOT187	–40 to +85, Plastic Leaded Chip Carrier, OTP	1.2 to 24
	PCF80C31BH4-24H	PCF80C51BH-4H	SOT307-2[2]	–40 to +85, Plastic Leaded Chip Carrier, OTP	1.2 to 24
PCB80C31-5 N	PCB80C31BH5-30P	PCB80C51BH-5P	SOT129	0 to +70, Plastic Dual In-line Package	1.2 to 33
PCB80C31-5 A	PCB80C31BH5-30WP	PCB80C51BH-5WP	SOT187	0 to +70, Plastic Leaded Chip Carrier	1.2 to 33
PCB80C31-5 B	PCB80C31BH5-30H	PCB80C51BH-5H	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack	1.2 to 33

CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



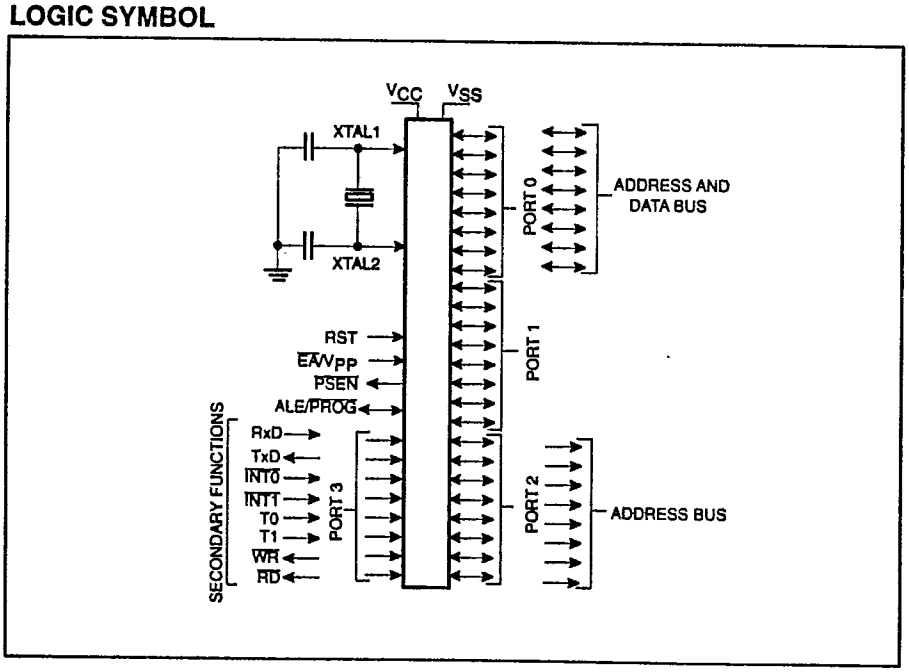
Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6	30	P2.6/A14
9	P1.7	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE/$\overline{PROG}$
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$/V_{PP}
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{CC}

PLASTIC QUAD FLAT PACK PIN FUNCTIONS

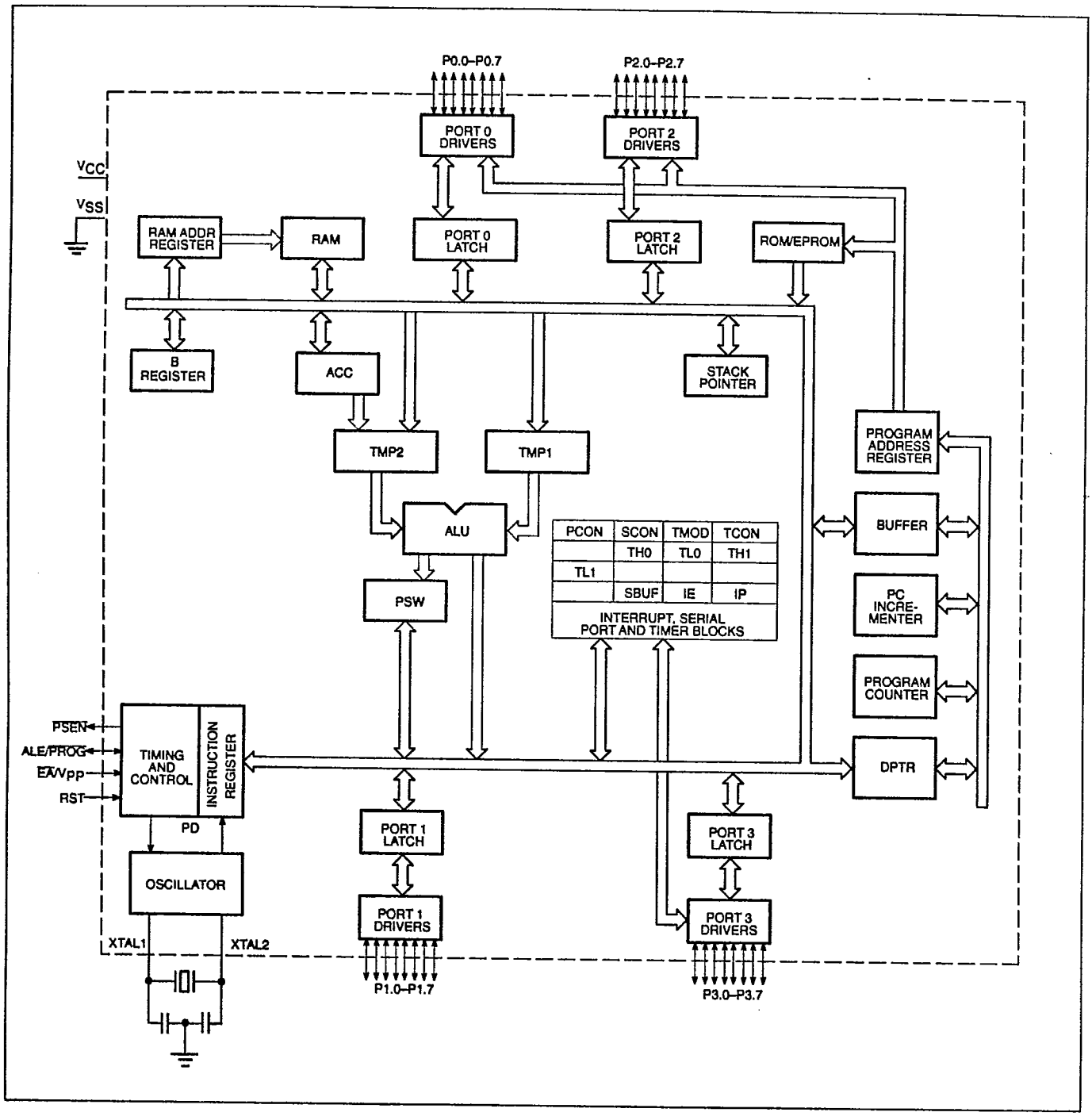


Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6	24	P2.6/A14
3	P1.7	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE/$\overline{PROG}$
6	NC	28	NC
7	P3.1/TxD	29	$\overline{EA}$/V_{PP}
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{CC}
17	NC	39	NC
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO. DIP	PIN NO. LCC	PIN NO. QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C51. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40-44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. the control bits for the reduced power modes are in the special function register PCON.

Table 1 shows the state of I/O ports during low current operating modes.

ROM CODE SUBMISSION

When submitting ROM code for the 80C51, the following must be specified:

1. 4k byte user ROM data
2. 32 byte ROM encryption key (SC80C51 only)
3. ROM security bits (SC80C51 only).

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 0FFFH	DATA	7:0	User ROM Data
1000H to 101FH	KEY	7:0	ROM Encryption Key
1020H	SEC	0	ROM Security Bit 1
1020H	SEC	1	ROM Security Bit 2

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. EA# is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Electrical Deviations from Commercial Specifications for Extended Temperature Range (87C51)
DC and AC parameters not included here are the same as in the commercial temperature range table.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (Philips North America Parts Only)
T_{amb} = –40°C to +125°C, V_{CC} = 5V ±10%, V_{SS} = 0V (Philips Parts Only)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$ (Philips North America)		–0.5	$0.2V_{CC}$–0.15	V
V_{IL}	Input low voltage, except $\overline{EA}$ (Philips)		–0.5	$0.2V_{CC}$–0.25	V
V_{IL1}	Input low voltage to $\overline{EA}$		–0.5	$0.2V_{CC}$–0.45	V
V_{IH}	Input high voltage, except XTAL1, RST		$0.2V_{CC}$+1	V_{CC}+0.5	V
V_{IH1}	Input high voltage to XTAL1, RST		$0.7V_{CC}$+0.1	V_{CC}+0.5	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.45V		–75	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	V_{IN} = 2.0V		–750	µA
I_{CC}	Power supply current: Active mode[1] @ 16MHz (Philips) Active mode @ 12MHz (Philips North America) Idle mode[2] @ 16MHz (Philips) Idle mode @ 12MHz (Philips North America) Power-down mode[3] (Philips) Power-down mode (Philips North America)	V_{CC} = 4.5–5.5V		 25 20 6.5 5 75 50	 mA mA mA mA µA µA

NOTES:
1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{CC}$ – 0.5V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{CC}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{CC}$ – 0.5V; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}.
3. The power-down current is measured with all output pins disconnected, XTAL2 not connected, $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}$/V_{PP} pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±20%, V_{SS} = 0V (80C31/51) (12, 16, and 24MHz versions)
T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (87C51) (80C31/80C51 33MHz version)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYPICAL[1]	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$[7]		–0.5		$0.2V_{CC}$–0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$[7]		0		$0.2V_{CC}$–0.3	V
V_{IH}	Input high voltage, except XTAL1, RST[7]		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST[7]		$0.7V_{CC}$		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3[11]	I_{OL} = 1.6mA[2]			0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[11]	I_{OL} = 3.2mA[2]			0.45	V
V_{OH}	Output high voltage, ports 1, 2, 3, ALE, $\overline{PSEN}$[3]	I_{OH} = –60µA, I_{OH} = –25µA I_{OH} = –10µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
V_{OH1}	Output high voltage (port 0 in external bus mode)	I_{OH} = –800µA, I_{OH} = –300µA I_{OH} = –80µA	2.4 $0.75V_{CC}$ $0.9V_{CC}$			V V V
I_{IL}	Logical 0 input current, ports 1, 2, 3[7]	V_{IN} = 0.45V			–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[7]	See note 4			–650	µA
I_{LI}	Input leakage current, port 0	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{CC}	Power supply current:[7] Active mode @ 12MHz[8] (Philips) Active mode @ 12MHz[5] (Philips North America) Idle mode @ 12MHz[9] (Philips) Idle mode @ 12MHz (Philips North America) Power-down mode[10] (Philips and Philips North America)	See note 6		 11.5 1.3 3	 18 19 4.4 4 50	 mA mA mA mA µA
R_{RST}	Internal reset pull-down resistor (Philips North America) (Philips)		 50 50		 300 150	 kΩ kΩ
C_{IO}	Pin capacitance (12)				10	pF

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. I_{CCMAX} at other frequencies (for Philips North America parts) is given by: Active mode: I_{CCMAX} = 1.43 X FREQ + 1.90; Idle mode: I_{CCMAX} = 0.14 X FREQ +2.31, where FREQ is the external oscillator frequency in MHz. I_{CCMAX} is given in mA. See Figure 7.
6. See Figures 8 through 11 for I_{CC} test conditions.
7. For Philips North America parts when T_{amb} = –40°C to +85°C or Philips parts when T_{amb} = –40°C to +125°C, see DC Electrical Characteristics table on previous page.
8. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{CC}$ – 0.5V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{CC}.
9. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ + 0.5V; $V_{IH} = V_{CC}$ – 0.5V; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}.
10. The power-down current is measured with all output pins disconnected, XTAL2 not connected, $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}.
11. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
    Maximum I_{OL} per port pin: 15mA
    Maximum I_{OL} per 8-bit port: 26mA
    Maximum I_{OL} total for all outputs: 67mA
    If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
12. Pin capacitance for the ceramic DIP package is 15pF maximum.

AC ELECTRICAL CHARACTERISTICS FOR 12–33MHz PHILIPS NORTH AMERICA DEVICES

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±20%, V_{SS} = 0V (80C31/51)[1, 2, 4] (12, 16, and 24MHz versions)
T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (87C51) (80C31/80C51 33MHz version)

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK[3]		UNIT
			MIN	MAX	
$1/t_{CLCL}$		Oscillator frequency: **Speed Versions** SC80C31/51 C G P Y	 3.5 3.5 3.5 3.5	 12 16 24 33	 MHz MHz MHz MHz
t_{LHLL}	1	ALE pulse width	$2t_{CLCL}-40$		ns
t_{AVLL}	1	Address valid to ALE low	$t_{CLCL}-13$		ns
t_{LLAX}	1	Address hold after ALE low	$t_{CLCL}-20$		ns
t_{LLIV}	1	ALE low to valid instruction in		$4t_{CLCL}-65$	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	$t_{CLCL}-13$		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	$3t_{CLCL}-20$		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		$3t_{CLCL}-45$	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		$t_{CLCL}-10$	ns
t_{AVIV}	1	Address to valid instruction in		$5t_{CLCL}-55$	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		10	ns
Data Memory					
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	$6t_{CLCL}-100$		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	$6t_{CLCL}-100$		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		$5t_{CLCL}-90$	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		$2t_{CLCL}-28$	ns
t_{LLDV}	2, 3	ALE low to valid data in		$8t_{CLCL}-150$	ns
t_{AVDV}	2, 3	Address to valid data in		$9t_{CLCL}-165$	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}-75$		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	$t_{CLCL}-20$		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	$t_{CLCL}-20$		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	$t_{CLCL}-20$	$t_{CLCL}+25$	ns
External Clock					
t_{CHCX}	4	High time	12		ns
t_{CLCX}	4	Low time	12		ns
t_{CLCH}	4	Rise time		20	ns
t_{CHCL}	4	Fall time		20	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. For all Philips North America speed versions only.
4. Interfacing the 80C31/51 to devices with float times up to 50ns is permitted. This limited bus contention will not cause damage to port 0 drivers.

AC ELECTRICAL CHARACTERISTICS FOR PHILIPS DEVICES

T_{amb} = 0°C to +70°C, V_{CC} = 5V ±20%, V_{SS} = 0V (80C31/51)[1, 2, 4, 5]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK[3]		UNIT
			MIN	MAX	
$1/t_{CLCL}$		Oscillator frequency: **Speed Versions** PCB8031/51 –2 PCA/PCB/PCF80C31/51 –3 PCB/PCF80C31/51 –4 PCB/FB80C31/51 –5	 0.5 1.2 1.2 1.2	 12 16 24 33	 MHz MHz MHz MHz
t_{LHLL}	1	ALE pulse width	$2t_{CLCL}-40$		ns
t_{AVLL}	1	Address valid to ALE low	$t_{CLCL}-25$		ns
t_{LLAX}	1	Address hold after ALE low	$t_{CLCL}-25$		ns
t_{LLIV}	1	ALE low to valid instruction in		$4t_{CLCL}-65$	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	$t_{CLCL}-25$		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	$3t_{CLCL}-45$		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		$3t_{CLCL}-60$	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		$t_{CLCL}-25$	ns
t_{AVIV}	1	Address to valid instruction in		$5t_{CLCL}-80$	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		10	ns
Data Memory					
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	$6t_{CLCL}-100$		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	$6t_{CLCL}-100$		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		$5t_{CLCL}-90$	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		$2t_{CLCL}-28$	ns
t_{LLDV}	2, 3	ALE low to valid data in		$8t_{CLCL}-150$	ns
t_{AVDV}	2, 3	Address to valid data in		$9t_{CLCL}-165$	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}-75$		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	$t_{CLCL}-30$		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	$t_{CLCL}-25$		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	$t_{CLCL}-25$	$t_{CLCL}+25$	ns
External Clock					
t_{CHCX}	4	High time	15		ns
t_{CLCX}	4	Low time	15		ns
t_{CLCH}	4	Rise time		20	ns
t_{CHCL}	4	Fall time		20	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. For all Philips speed versions only.
4. Interfacing the 80C31/51 to devices with float times up to 30ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
5. V_{CC} = 5V ±10% for 33MHz.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.

t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

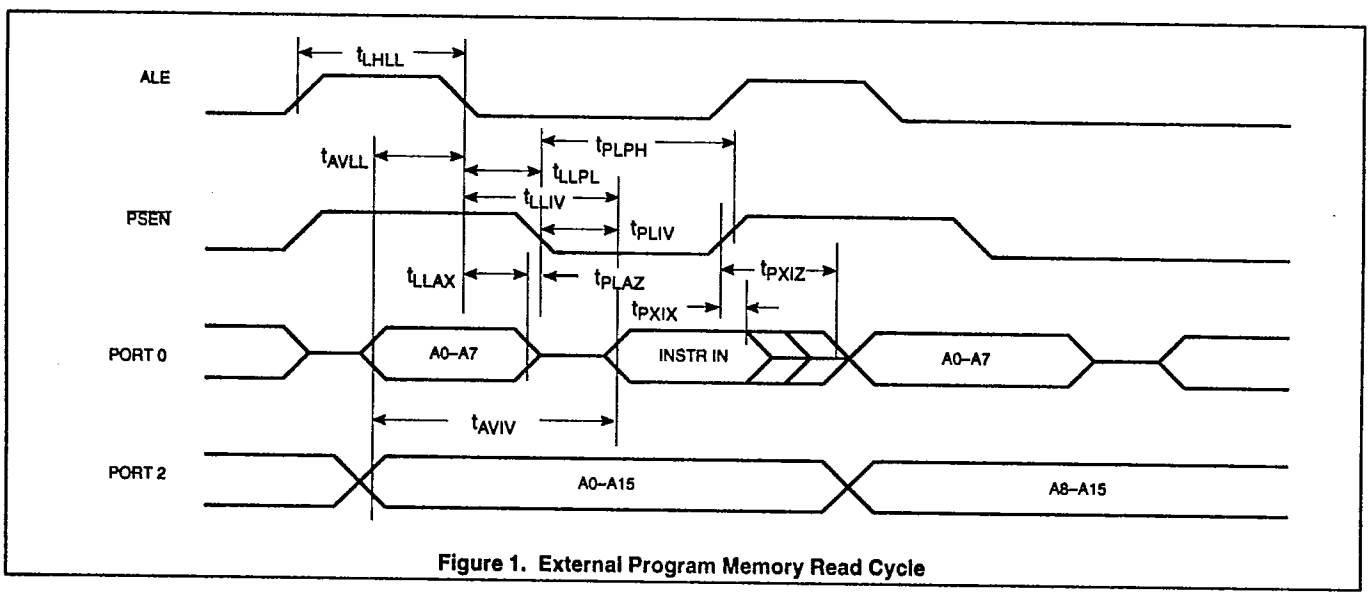


Figure 1. External Program Memory Read Cycle

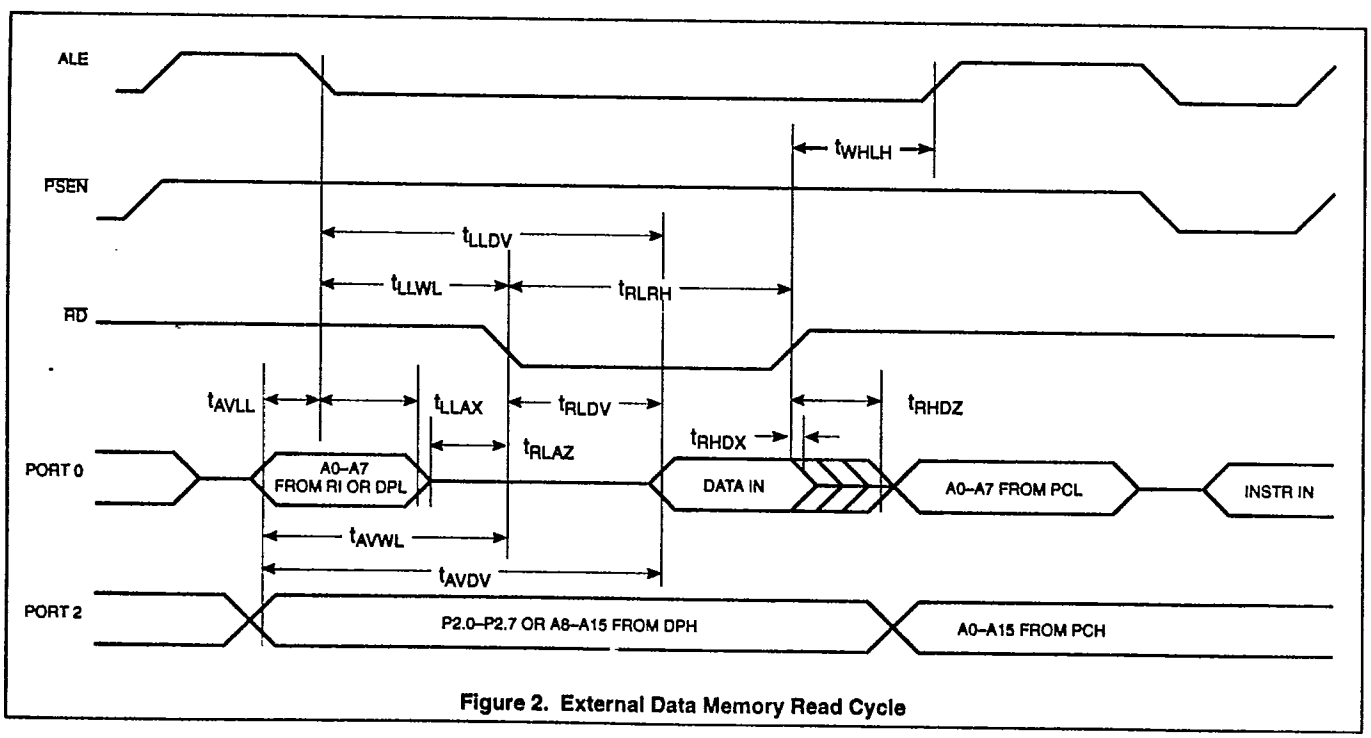


Figure 2. External Data Memory Read Cycle

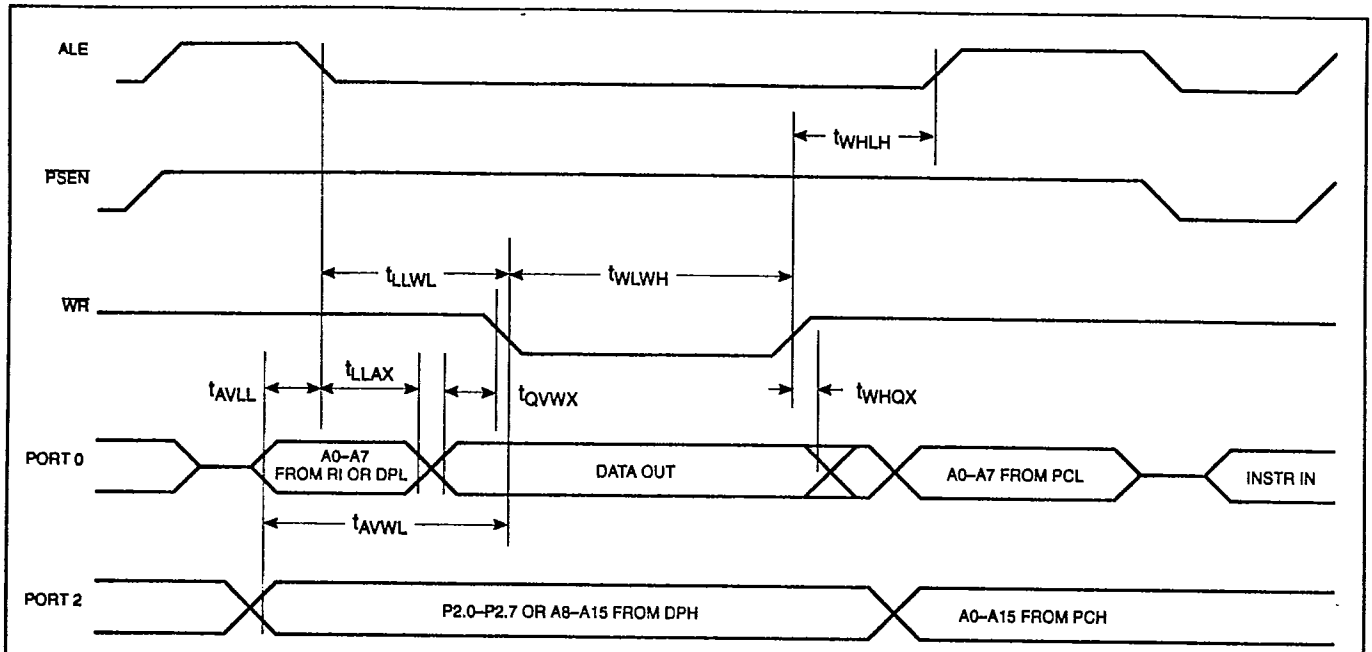


Figure 3. External Data Memory Write Cycle

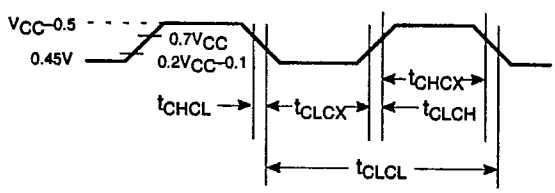
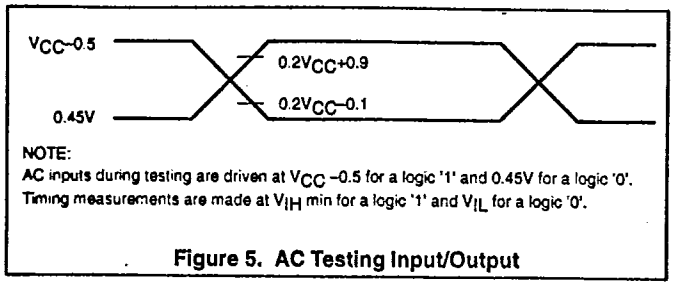
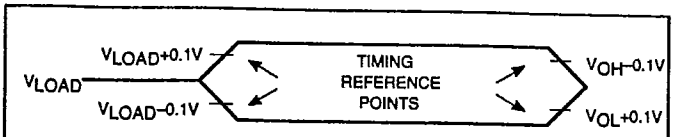


Figure 4. External Clock Drive



NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} for a logic '0'.

Figure 5. AC Testing Input/Output



NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20$mA.

Figure 6. Float Waveform

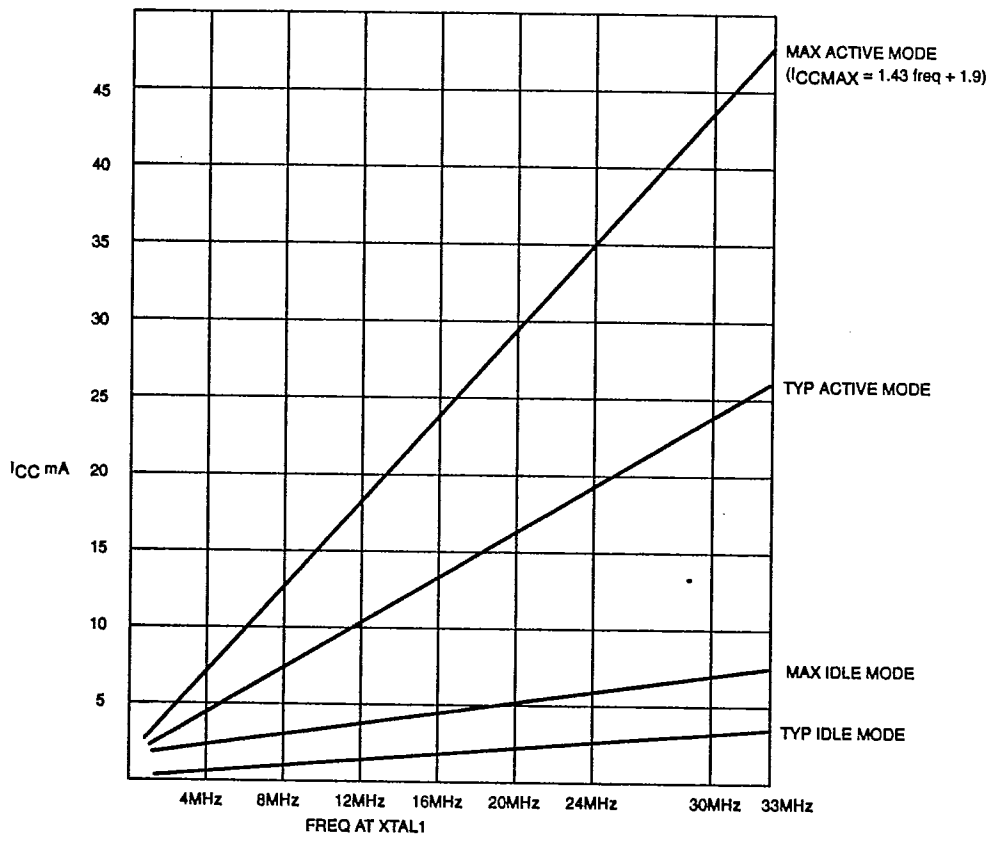


Figure 7. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

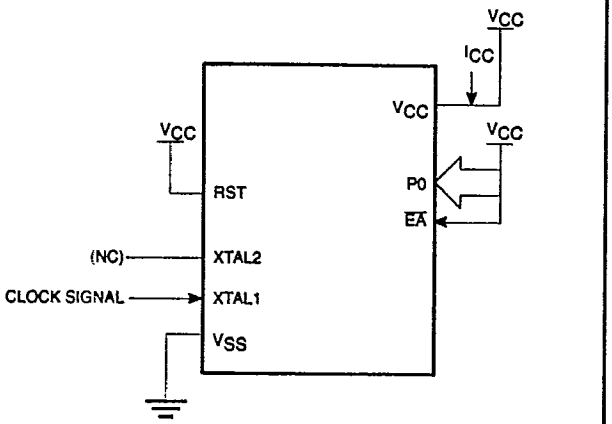


Figure 8. I_{CC} Test Condition, Active Mode
All other pins are disconnected

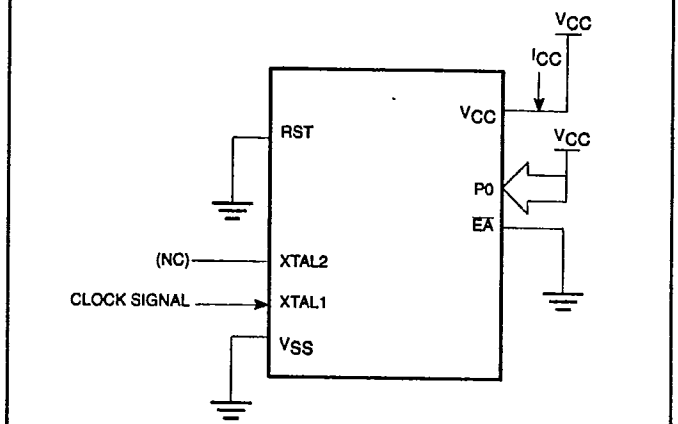


Figure 9. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

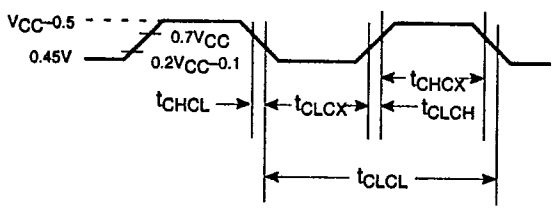


Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

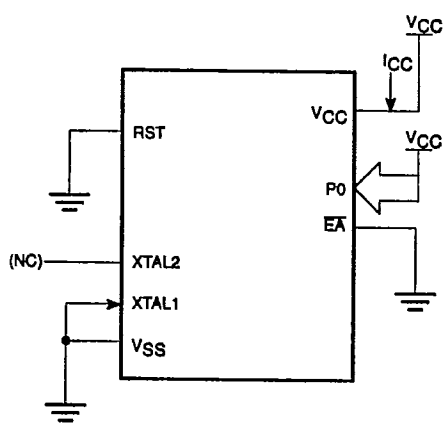


Figure 11. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. V_{CC} = 2V to 5.5V

EPROM CHARACTERISTICS

The 87C51 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C51 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C51 manufactured by Philips Corporation.

Table 2 shows the logic levels for reading the signature bytes, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 12 and 13. Figure 14 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 12. Note that the 87C51 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 12. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 2 are held at the 'Program Code Data' levels indicated in Table 2. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 13.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 14. The other pins are held at the 'Verify Code Data' levels indicated in Table 2. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips
(031H) = 92H indicates 87C51

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 2, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 2. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm security bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm security bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. V_{PP} = 12.75V ±0.25V.
3. V_{CC} = 5V±10% during programming and verification.
4. *ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

™Trademark phrase of Intel Corporation.

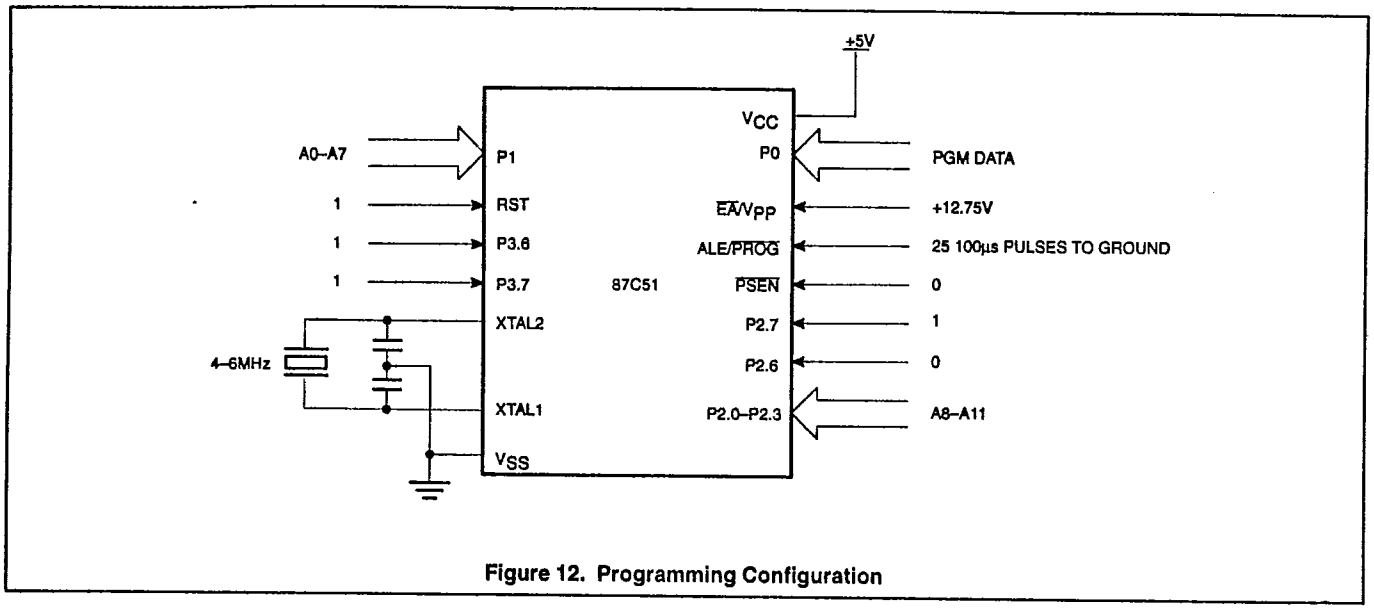


Figure 12. Programming Configuration

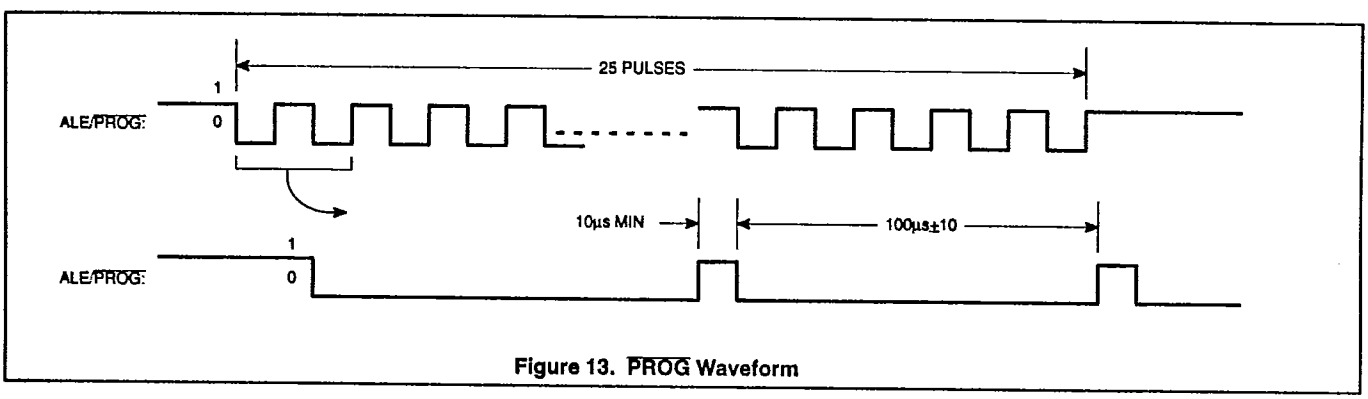


Figure 13. PROG Waveform

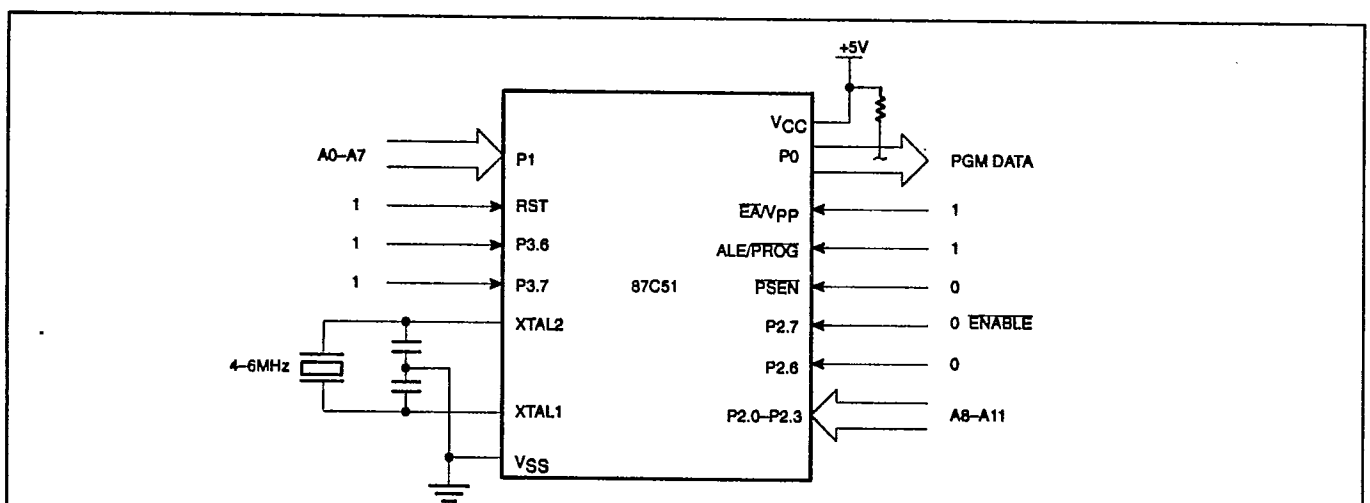


Figure 14. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 15)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		us
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		us
t_{GLGH}	$\overline{PROG}$ width	90	110	us
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		us

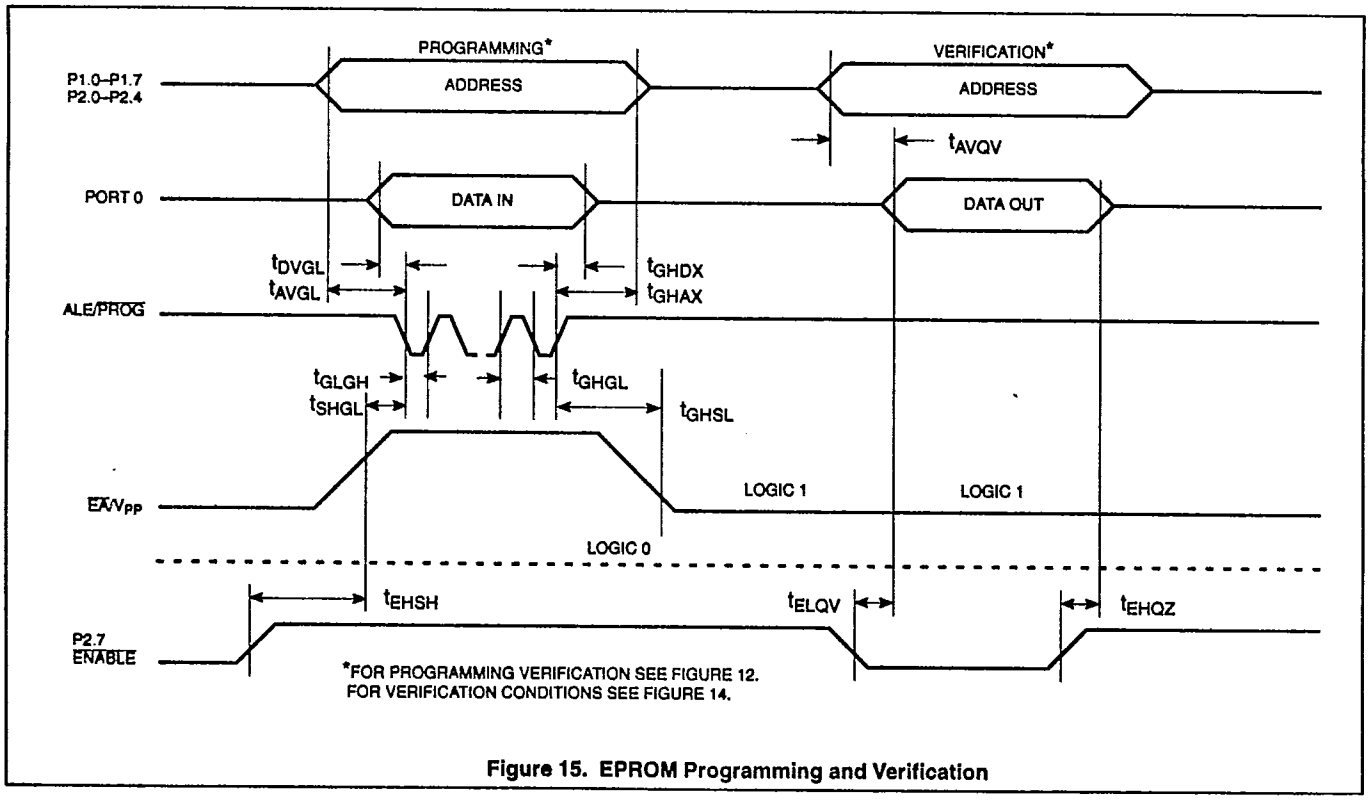


Figure 15. EPROM Programming and Verification