Dual universal serial communications controller (DUSCC) SCN26562

DESCRIPTION

The Philips Semiconductors SCN26562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN26562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multi-function counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

This document contains the electrical specifications for the SCN26562. See SCN26562/SCN68562 User's Guide for complete functional description.

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA EOPN input
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbit/sec data rate Receives up to 2Mbit/sec data rate

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Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and detection
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line-fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C		DWG #
	Serial Data Rate = 2.5Mbps Maximum	Serial Data Rate = 4Mbps Maximum	
48-Pin Plastic Dual In-Line Package (DIP)	SCN26562C2N48	SCN26562C4N48	0416C
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCN26562C2A52	SCN26562C4A52	0397E

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V

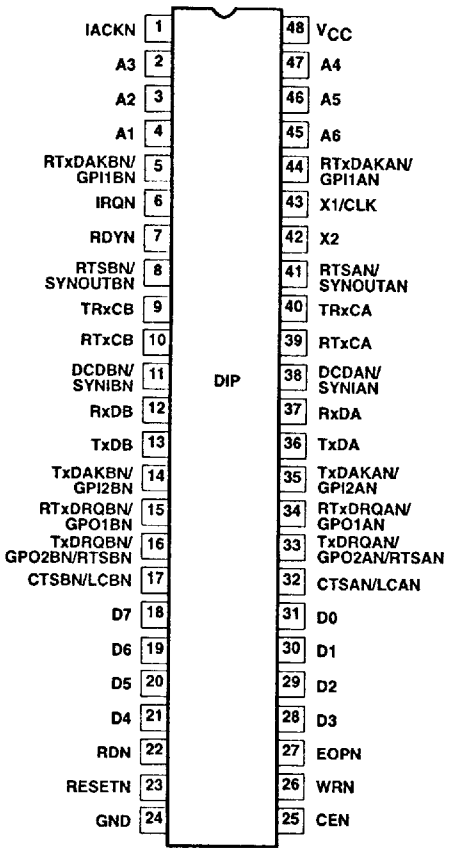
NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 36°C/W junction to ambient for ceramic DIP, 40°C/W for plastic DIP, and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

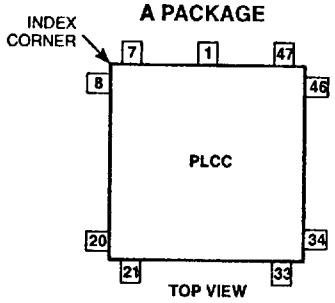
Dual universal serial communications controller (DUSCC) SCN26562

PIN CONFIGURATIONS

N PACKAGE



A PACKAGE



PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RDYN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	VCC

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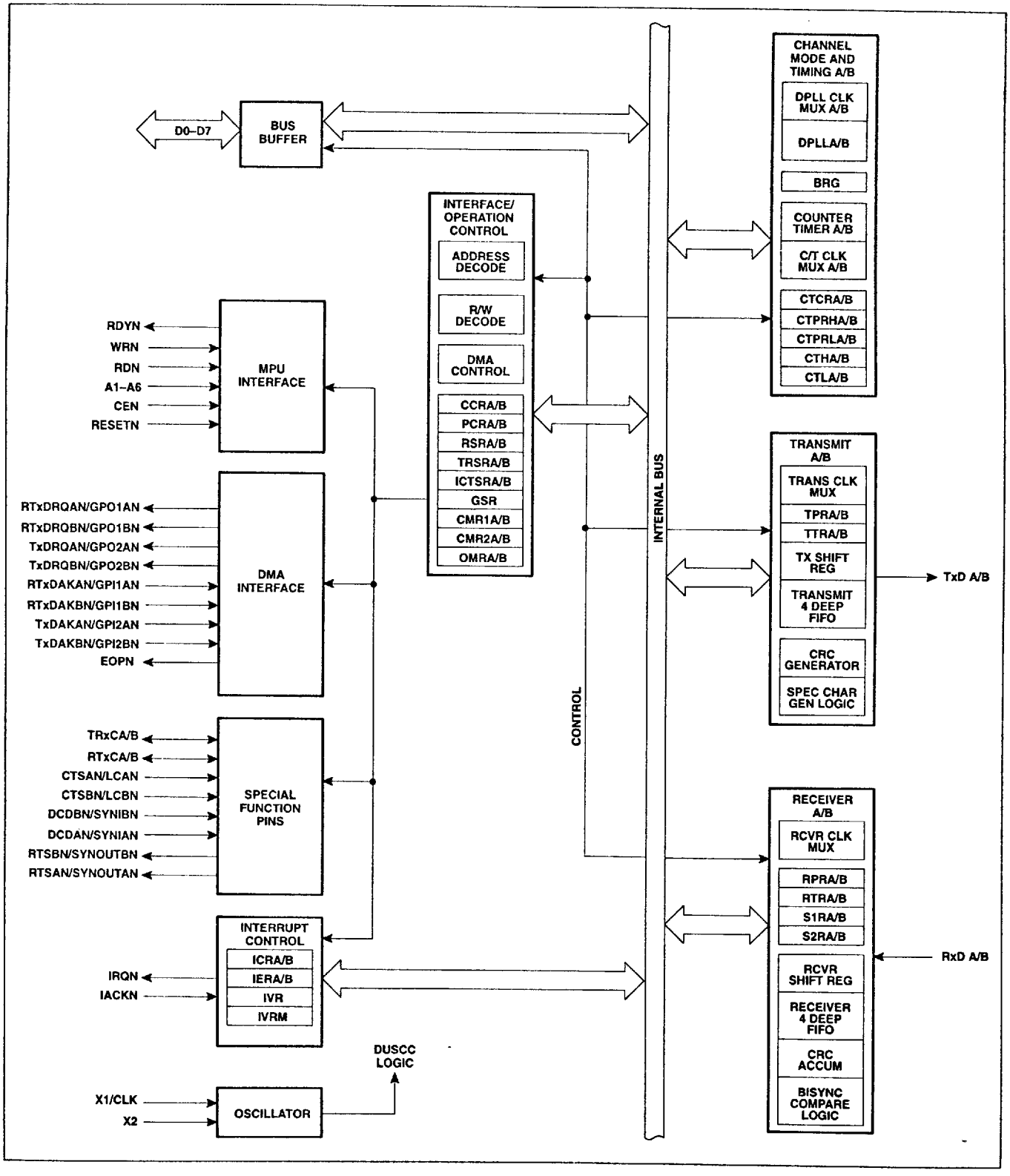
BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4–2, 47–45	4–2, 51–49	I	Address lines.
D0–D7	31–28, 21–18	33–30, 23–20	I/O	Bidirectional data bus.
RDN	22	24	I	Read strobe.
WRN	26	28	I	Write strobe.
CEN	25	27	I	Chip select.
RDYN	7	8	O	Ready.
IRQN	6	6	O	Interrupt request.
IACKN	1	1	I	Interrupt acknowledge.
X1/CLK	43	47	I	Crystal 1 or external clock.
X2	42	46	I	Crystal 2.
RESETN	23	25	I	Master reset.
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) receiver serial data.
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) transmitter serial data.
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) receiver/transmitter clock.
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) transmitter/receiver clock.
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) clear-to-send input or loop control output.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) data carrier detected or external sync.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) receiver/transmitter DMA service request or general purpose output.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) transmitter DMA service request, general purpose output or request-to-send.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) receiver/transmitter DMA acknowledge or general purpose input 1.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	Channel A (B) transmitter DMA acknowledge or general purpose input 2.
EOPN	27	29	I/O	DMA transfer complete.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) request-to-send or Sync detect.
V_{CC}	48	52	I	Power input.
GND	24	26	I	Signal and power ground.

DC ELECTRICAL CHARACTERISTICS[1, 3] T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage: All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage: All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage: All except IRQN	I_{OL} = 5.3mA				V
	IRQN	I_{OL} = 8.8mA			0.5	V
V_{OH}	Output high voltage: (Except open drain outputs)	I_{OH} = −400µA	2.4		0.5	V
I_{ILX1}	X1/CLK input low current[3]	V_{IN} = 0, X2 = GND	−5.5		0.0	mA
I_{IHX1}	X1/CLK input high current[3]	V_{IN} = V_{CC}, X2 = GND			1.0	mA
I_{ILX2}	X2 input low current[3]	V_{IN} = 0, X1 = open	−100			µA
I_{IHX2}	X2 input high current[3]	V_{IN} = V_{CC}, X1 = open			100	µA
I_{IL}	Input low current RESETN, TxDAKN, RxDAKN	V_{IN} = 0	−40			µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	−5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	−5			µA
I_{ODL}	Open drain output low current in off state: EOPN	V_{IN} = 0			−25	µA
	IRQN, RDYN		−120			µA
I_{ODH}	Open drain output high current in off state: EOPN, IRQN, RDYN	V_{IN} = V_{CC}	−5		5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}			275	mA
C_{IN}	Input capacitance[2]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[2]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[2]	V_{CC} = GND = 0			20	pF

NOTES:
1. Parameters are valid over specified temperature range.
2. These values were not explicitly tested; they are guaranteed by design and characterization data.
3. X1/CLK and X2 are not tested with a crystal installed.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = 0°C to +70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RELREH}	RESETN low to RESETN high	1.2		1.2		µs

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.8V and 2.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.4V. All time measurements are referenced at input voltages of 0.4V and 2.4V and output voltages of 1.2V and 2.0V, as appropriate.
3. See Figure 16 for test conditions for outputs.
4. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures true switching has occurred.

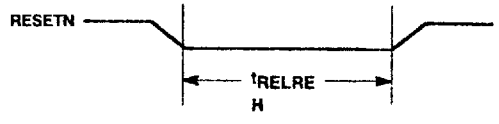
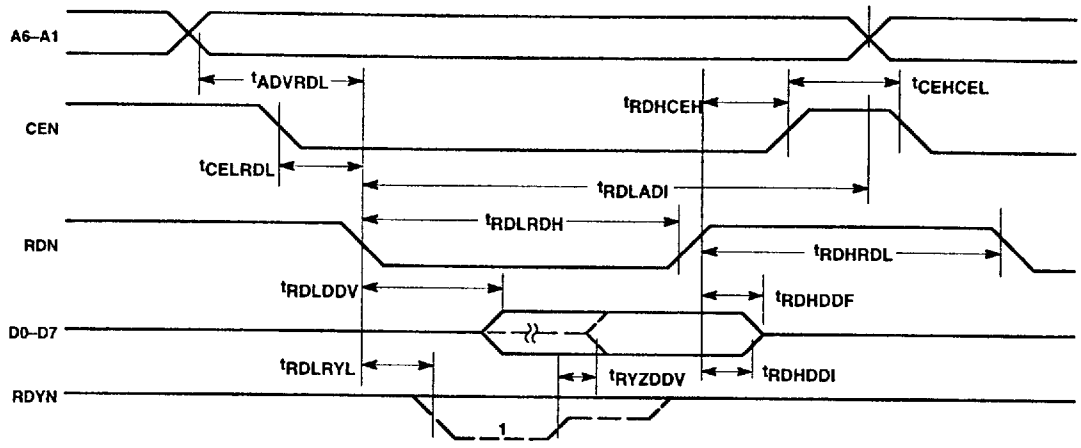


Figure 1. Reset Timing

AC ELECTRICAL CHARACTERISTICS (Continued)

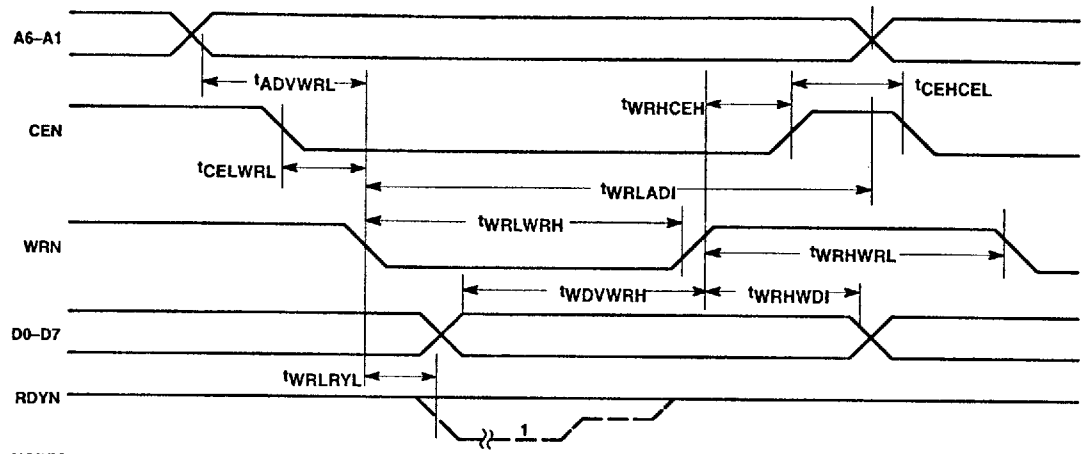


NOTES:
1. Wait on Rx. Receiver FIFO empty.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

Figure 2. Read Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVRDL}	Address valid to RDN low	10		10		ns
t_{CELRDL}	CEN low to RDN low	0		0		ns
t_{RDLADI}	RDN low to address invalid	150		150		ns
t_{RDLRYL}	RDN low to RDYN low		275		275	ns
t_{RDLDDV}	RDN low to read data valid		280		300	ns
t_{RDLRDH}	RDN low to RDN high	300		310		ns
t_{RYZDDV}	RDYN high impedance to read data valid		100		100	ns
t_{RDHCEH}	RDN high to CEN high	0		0		ns
t_{CEHCEL}	CEN high to CEN low	160		170		ns
t_{RDHDDI}	RDN high to read data invalid	10		10		ns
t_{RDHRDL}	RDN high to RDN low	160		170		ns
t_{RDHDDF}	RDN high to data bus floating		75		75	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

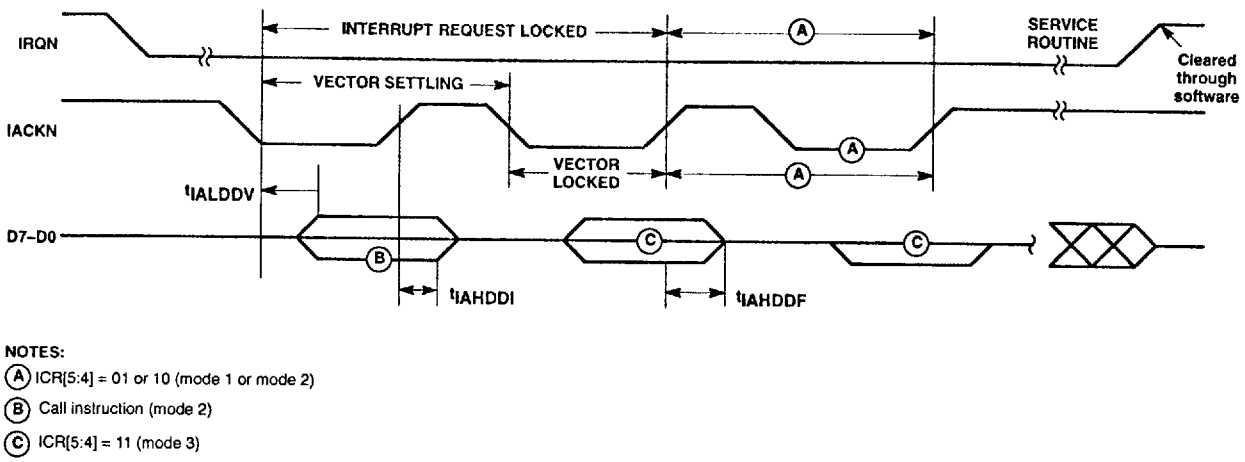


NOTES:
1. Wait on Tx. Transmitter FIFO full.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

Figure 3. Write Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVWRL}	Address valid to WRN low	10		10		ns
t_{CELWRL}	CEN low to WRN low	0		0		ns
t_{WRLRYL}	WRN low to READY low					ns
t_{WRHCEH}	WRN high to CEN high	0		0		ns
t_{WRLWRH}	WRN low to WRN high	300		310		ns
t_{WDVWRH}	Write data valid to WRN high	100	275	100	275	ns
t_{CEHCEL}	CEN high to CEN low	160		170		ns
t_{WRLADI}	WRN low to address invalid	150		150		ns
t_{WRHWRL}	WRN high to WRN low	160		170		ns
t_{WRHWDI}	WRN high to write data invalid	10		10		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) ICR[5:4] = 01 or 10 (mode 1 or mode 2)
(B) Call instruction (mode 2)
(C) ICR[5:4] = 11 (mode 3)

Figure 4. Interrupt Acknowledge Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{IALDDV}	IACKN low to data bus valid		280		280	ns
t_{IAHDDF}	IACKN high to data bus floating		150		150	ns
t_{IAHDDI}	IACKN high to data bus invalid	10		10		ns

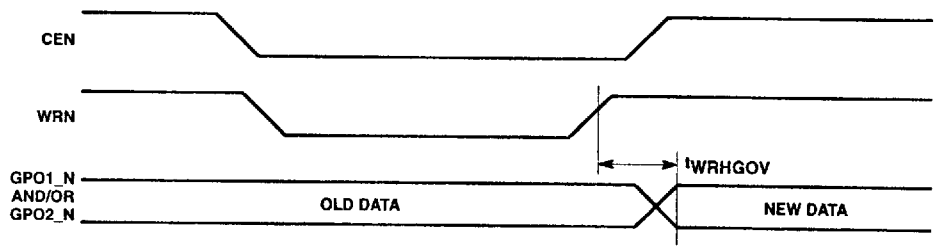


Figure 5. Output Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{WRHGOV}	WRN high to GPO output data valid		300		300	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

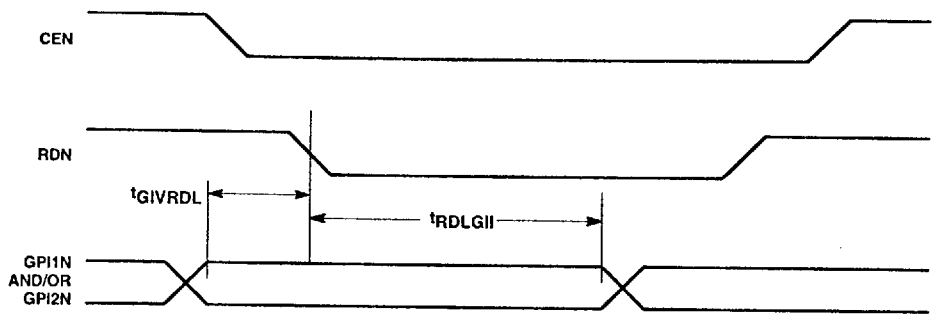


Figure 6. Input Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{GIVRDL}	GPI input valid to RDN low	20		20		ns
t_{RDLGII}	RDN low to GPI input invalid	100		100		ns

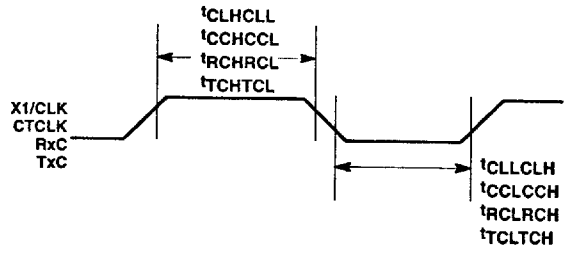


Figure 7. Clock Timing

SYMBOL	PARAMETER	LIMITS						UNIT
		SCN26562C4			SCN26562C2			
		Min	Typ	Max	Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			25			ns
t_{CLLCLH}	X1/CLK low to high time	25			25			ns
t_{CCHCCL}	C/T CLK high to low time	100			100			ns
t_{CCLCCH}	C/T CLK low to high time	100			100			ns
t_{RCHRCL}	RxC high to low time	110			150			ns
t_{RCLRCH}	RxC low to high time	110			150			ns
t_{TCHTCL}	TxC high to low time	110			150			ns
t_{TCLTCH}	TxC low to high time	110			150			ns
f_{CL}	X1/CLK frequency	2.0		16.0	2.0		16.0	MHz
f_{CC}	C/T CLK frequency	0		4.0	0		4.0	MHz
f_{RC}	RxC frequency (16X or 1X)	0	14.7456	4.0	0	14.7456	2.5	MHz
f_{TC}	TxC frequency (16X or 1X)	0		4.0	0		2.5	MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

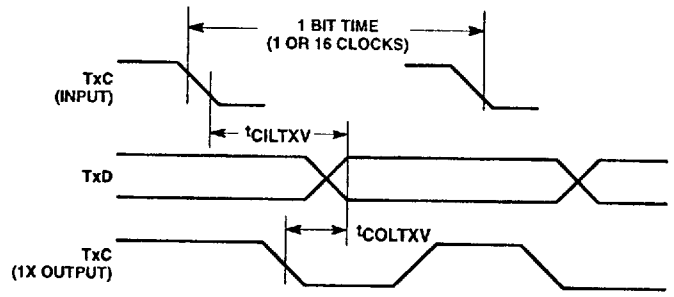


Figure 8. Transmit Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{CILTXV}	TxC input low (1X) to TxD output		240		240	ns
	TxC input low (16X) to TxD output		435		435	ns
t_{COLTXV}	TxC output low to TxD output		50		50	ns

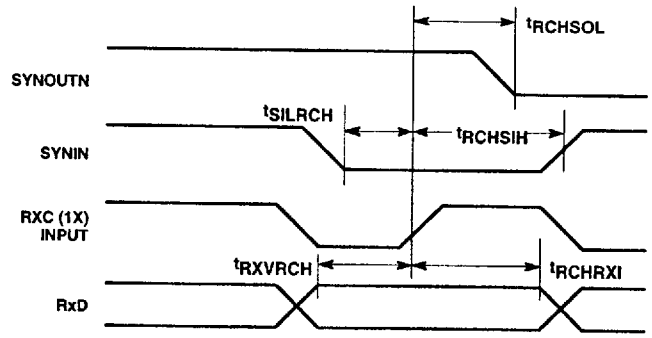


Figure 9. Receive Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RXVRCH}	RxD data valid to RxC high:					
	For NRZ data	50		50		ns
t_{RCHRXI}	For NRZI, Manchester, FM0, FM1 data	120		130		ns
	RxC high to RxD data invalid:					
	For NRZ data	50		50		ns
	For NRZI, Manchester, FM0, FM1 data	10		10		ns
t_{SILRCH}	SYNIN low to RxC high	100		100		ns
t_{RCHSIH}	RxC high to SYNIN high	50		50		ns
t_{RCHSOL}	RxC high to SYNOUT low		300		300	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

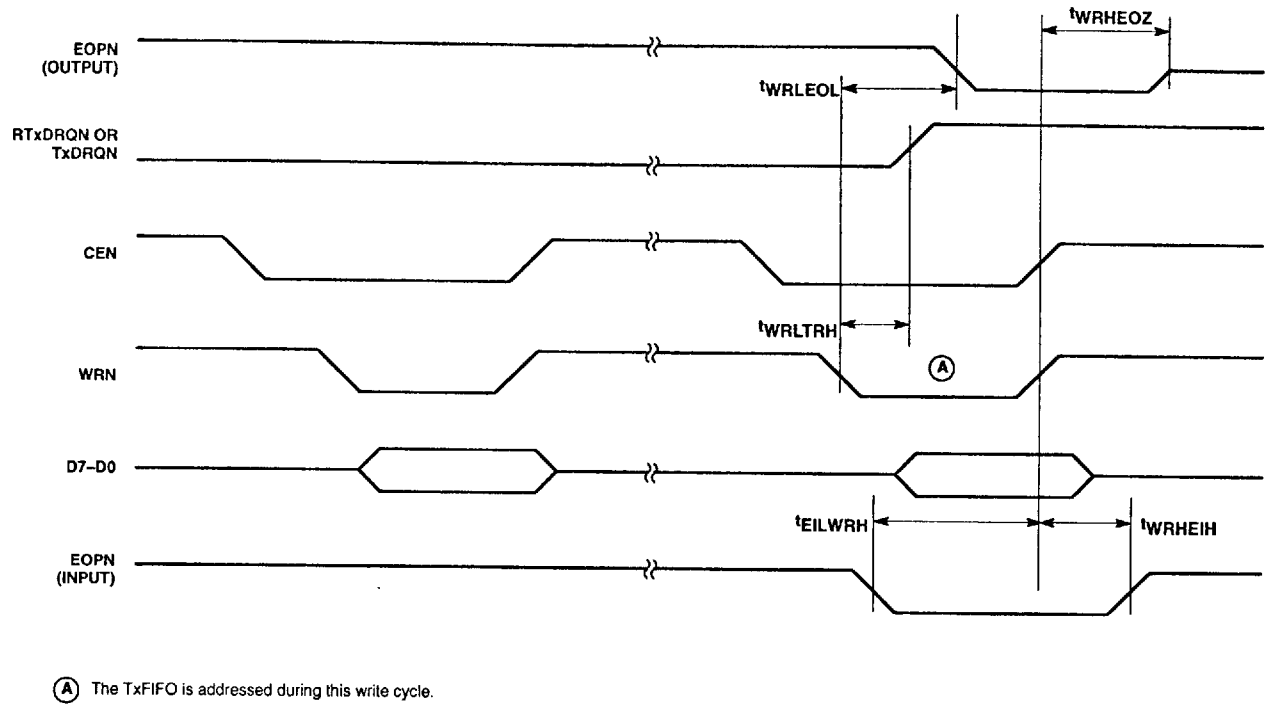
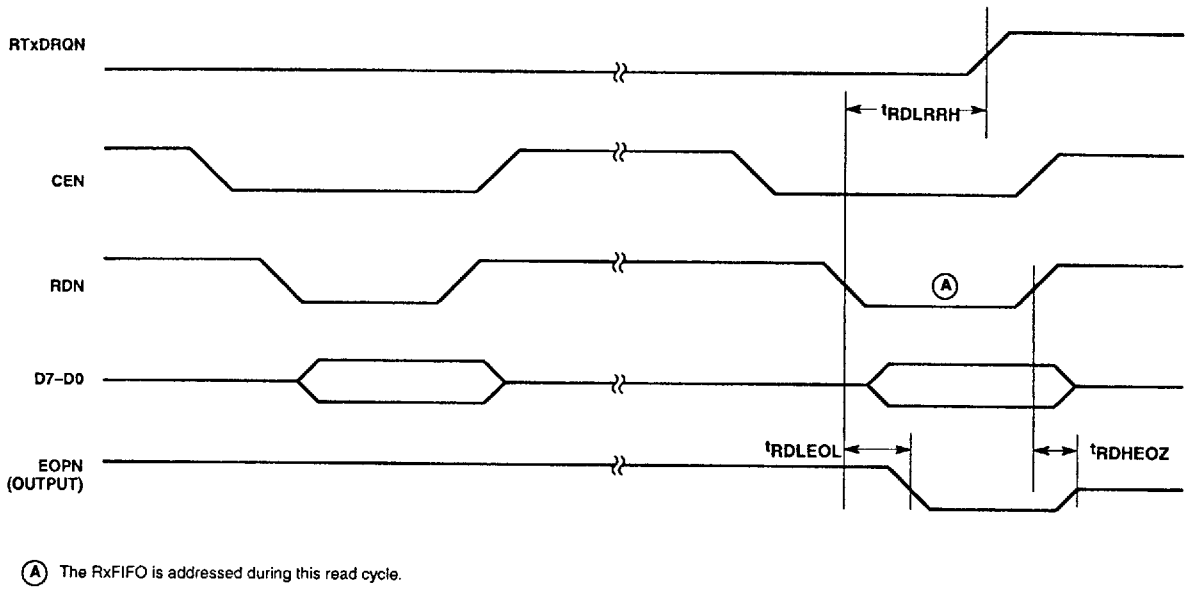


Figure 10. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{WRLTRH}	WRN low to Tx DMA REQN high					ns
t_{WRLEOL}	WRN low to EOPN output low		320		320	ns
t_{WRHEOZ}	WRN high to EOPN output high impedance		225		225	ns
t_{EILWRH}	EOPN input low to WRN high	50	225	50	225	ns
t_{WRHEIH}	WRN high to EOPN input high	50		50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

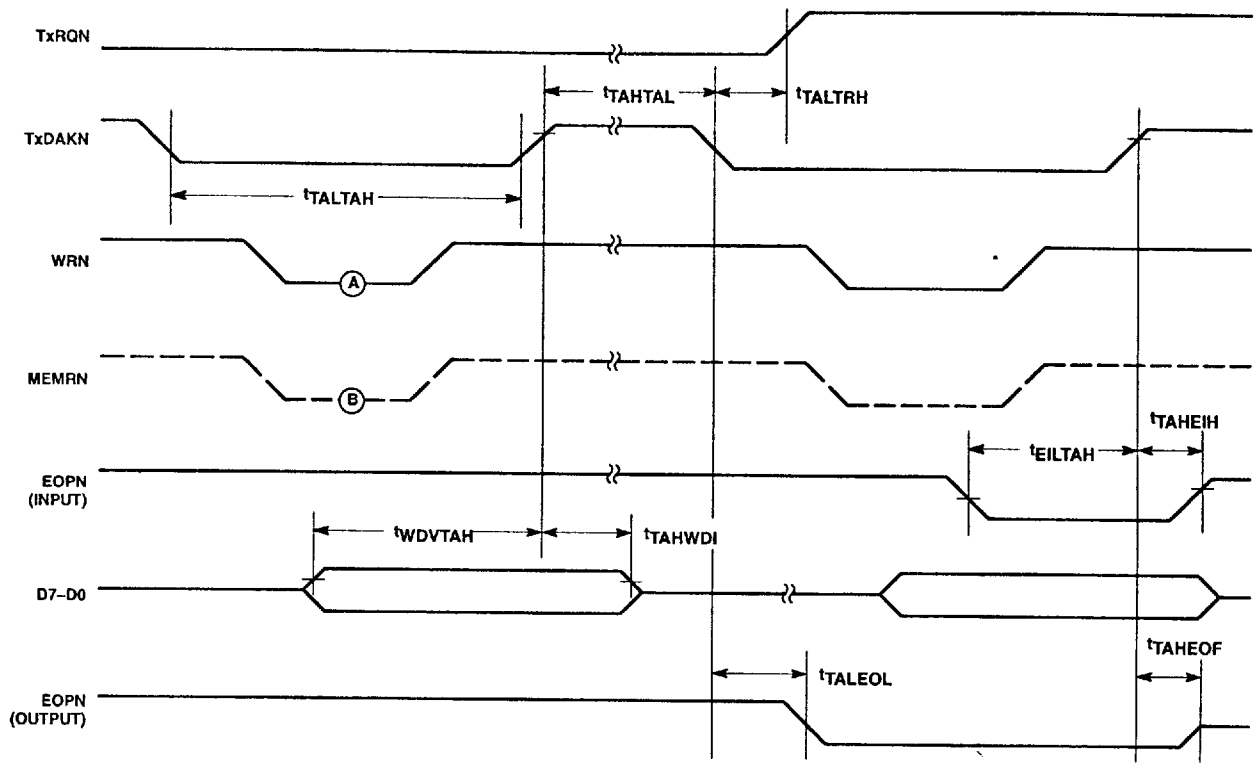


(A) The RxFIFO is addressed during this read cycle.

Figure 11. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RDLRRH}	RDN low to Rx DMA REQN high		320		320	ns
t_{RDLEOL}	RDN low to EOPN output low		300		300	ns
t_{RDHEOZ}	RDN high to EOPN output high impedance		225		225	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

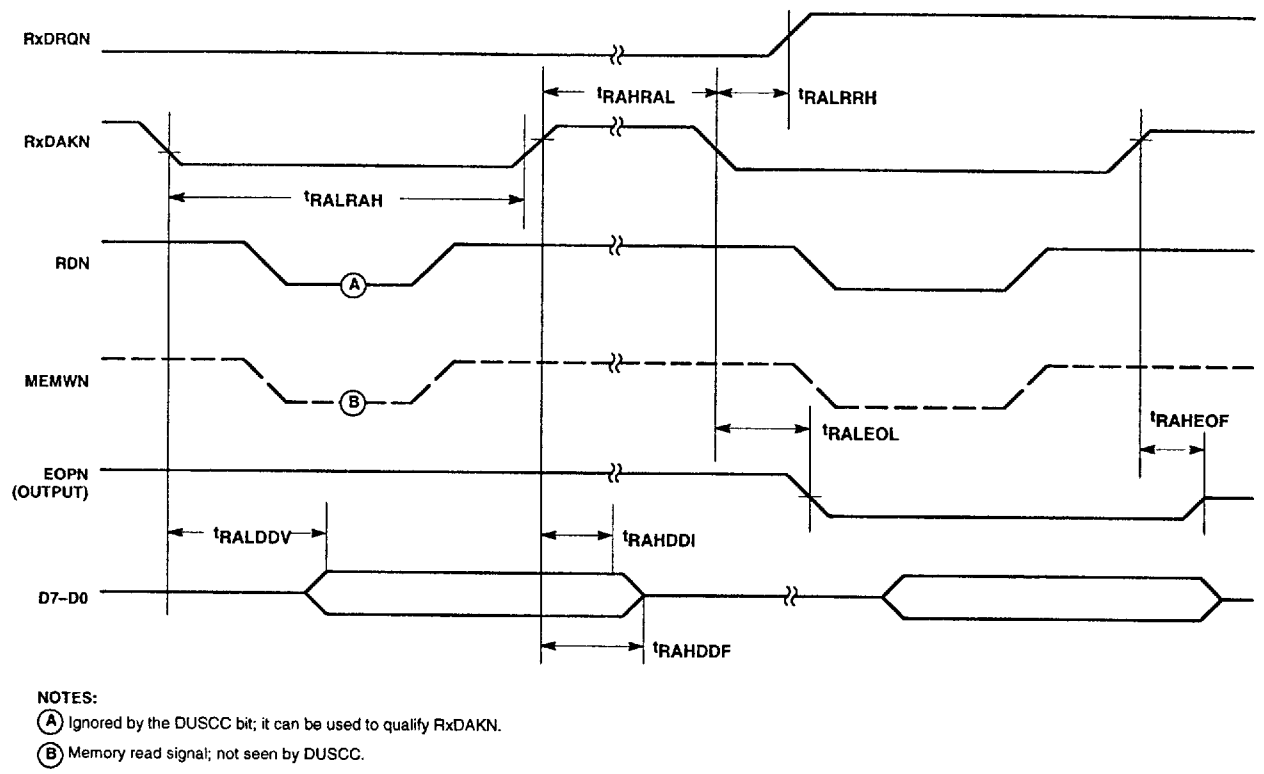


NOTES:
(A) Ignored by the DUSCC since CEN is not asserted, but it can be used externally to qualify TxDAKN.
(B) Memory read signal; not seen by DUSCC.

Figure 12. DMA-Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{TAHTAL}	Transmit DMA ACKN high to low time	100		100		ns
t_{TALTAH}	Transmit DMA ACKN low to high time	250		250		ns
t_{TALTRH}	Tx DMA ACKN low to Tx DMA REQN high					ns
t_{WDVTAH}	Write data valid to Tx DMA ACKN high	90	250	90	250	ns
t_{TAHWDI}	Tx DMA ACKN high to write data invalid	30		30		ns
t_{TALEOL}	Tx DMA ACKN low to EOPN output low					ns
t_{TAHEOF}	Tx DMA ACKN high to EOPN output float		170		170	ns
t_{EILTAH}	EOPN input low to Tx DMA ACKN high	50	200	50	200	ns
t_{TAHEIH}	Tx DMA ACKN high to EOPN input high	50		50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) Ignored by the DUSCC bit; it can be used to qualify RxDAKN.
(B) Memory read signal; not seen by DUSCC.

Figure 13. DMA-Receive Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RAHRAL}	Receive DMA ACKN high to low time	160		160		ns
t_{RALRAH}	Receive DMA ACKN low to high time	250		250		ns
t_{RALRRH}	Rx DMA ACKN low to Rx DMA REQN high		320		320	ns
t_{RALEOL}	Rx DMA ACKN low to EOPN output low		200		200	ns
t_{RAHEOF}	Rx DMA ACKN high to EOPN output float		225		225	ns
t_{RALDDV}	Rx DMA ACKN low to read data valid		225		225	ns
t_{RAHDDI}	Rx DMA ACKN high to read data invalid	10		10		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		125		125	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

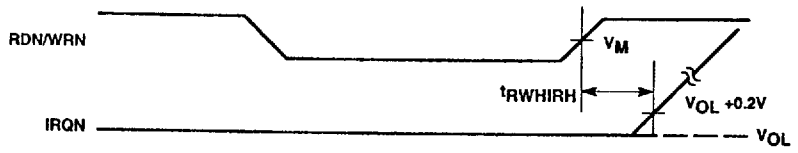


Figure 14. Interrupt Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RWHIRH}	RDN/WRN high to IRQN high for:					
	Read RxFIFO (RxRDY interrupt)		450		450	ns
	Write TxFIFO (TxRDY interrupt)		450		450	ns
	Write RSR (Rx condition interrupt)		400		400	ns
	Write TRSR (Rx/Tx interrupt)		400		400	ns
	Write ICTSR (counter/timer interrupt)		400		400	ns

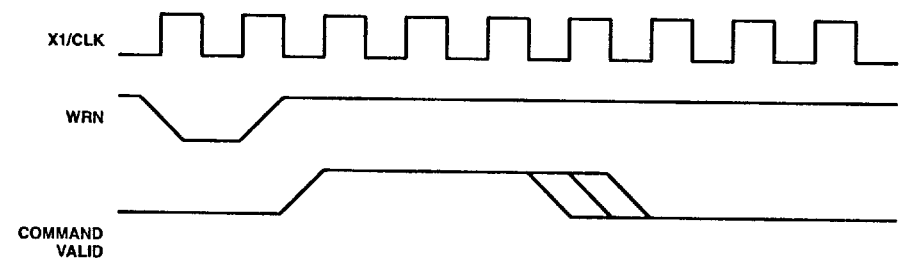


Figure 15. Command Timing

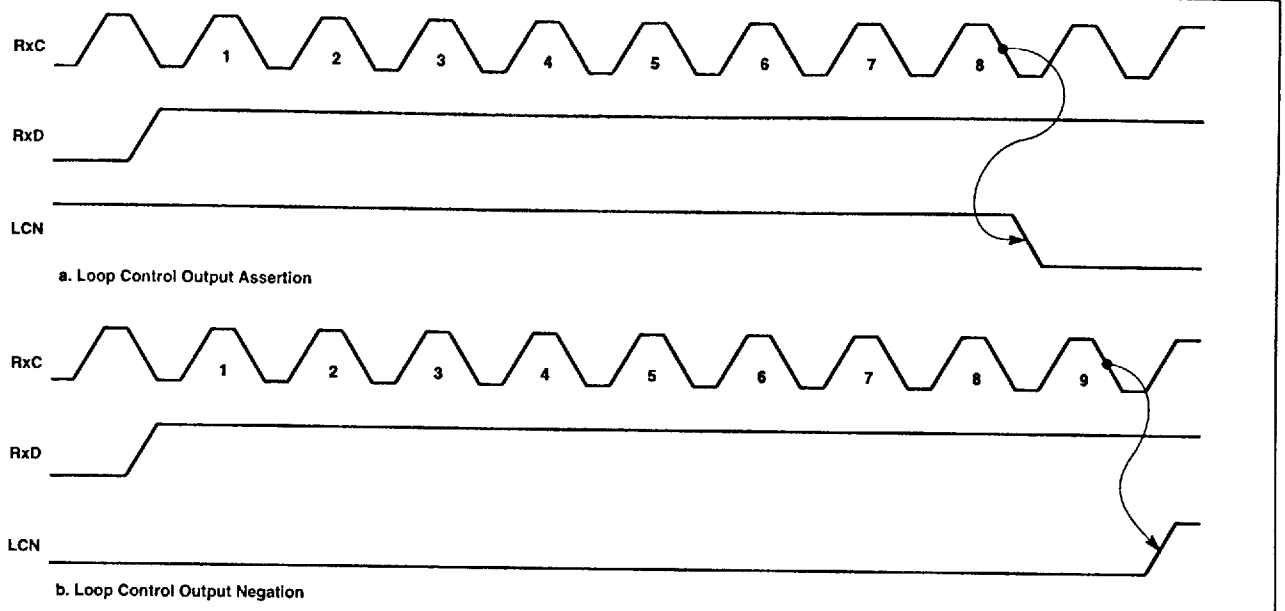
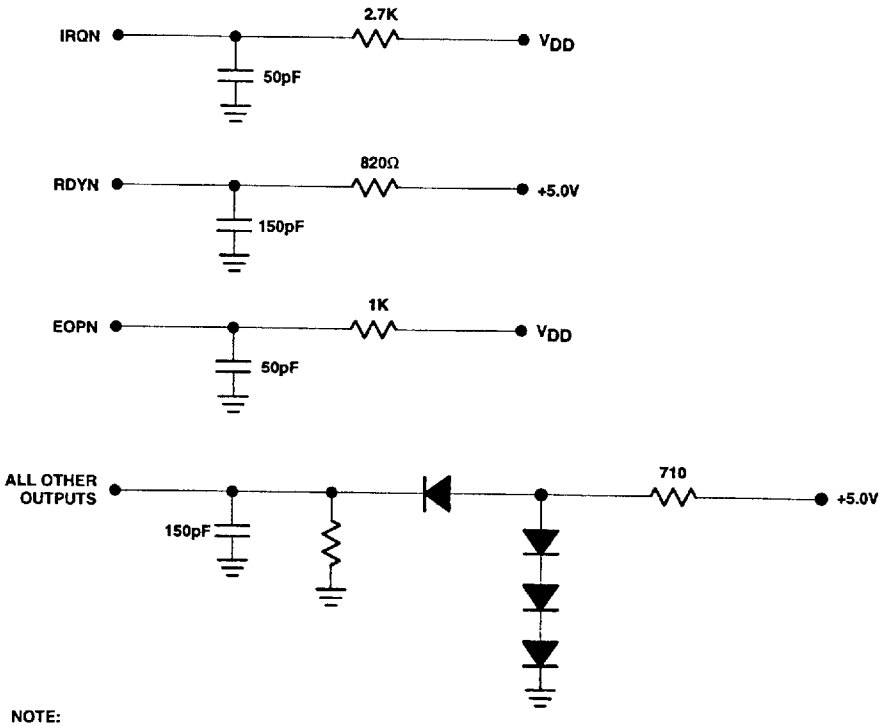


Figure 15. Relationship Between Received Data and the Loop Control Output



NOTE:
All C_L includes 50pF stray capacitance,
i.e., C_L = 150pF = 100pF discrete +50pF stray.

Figure 16. Test Conditions for Outputs