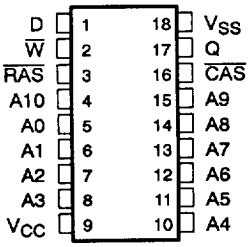
- **Processed to MIL-STD-883, Class B**
- **Organization . . . 4194304 × 1**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

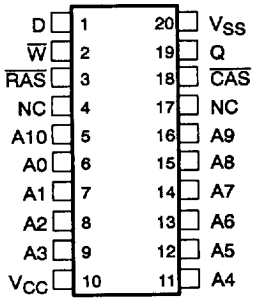
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44100-80	80 ns	20 ns	40 ns	150 ns
SMJ44100-10	100 ns	25 ns	50 ns	180 ns
SMJ44100-12	120 ns	30 ns	55 ns	210 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  1024-Cycle Refresh in 16 ms (Max)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **Packaging Options:**
  - **18-Pin, 400 mil Ceramic DIP (JD Suffix)**
  - **18-Pin, 300 mil Ceramic DIP (JDB Suffix)**
  - **20-Pin, Ceramic Flatpack (HR Suffix)**
  - **20-Pad, 350 × 675 Ceramic Chip Carrier (HL Suffix)**
  - **Additional Package Options Planned**
- **Military Temperature Range**
  –55 °C to 125°C

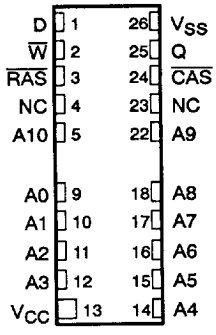
JD/JDB PACKAGES
(TOP VIEW)



HR PACKAGE
(TOP VIEW)



HL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44100 is a series of high-speed 4194304-bit dynamic random-access memories (DRAMs), organized as 4194304 words of one bit each. They employ state-of-the-art enhanced performance implanted CMOS EPIC™ technology for high performance, reliability, and low power operation.

The SMJ44100 features maximum row access time of 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 385 mW operating and 22 mW standby.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data-out lines are unlatched to allow greater system flexibility.

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description (continued)

The SMJ44100 is offered in a 300-mil 18-pin ceramic dual-in-line package (JDB suffix), an 18-pin ceramic dual-in-line package (JD suffix), a 20-pin ceramic flatpack (HR suffix), and a 20-pad 350 × 675 ceramic chip carrier package (HL suffix). All packages are guaranteed for operation from – 55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44100 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} maximum (access time from $\overline{CAS}$ low), if t_{AA} maximum (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A10)

Twenty-two address bits are required to decode 1 of 4194304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by $\overline{RAS}$. The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ is already low, the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

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data out (Q)

The high-impedance state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output follows the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every 16 ms to retain data. This can be achieved by strobing each of the1024 rows (A0–A9, A10 is ignored). A normal read or write cycle refreshes all bits in each row that is selected as well as the corresponding row relative to A10. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

test mode

An industry standard design for test (DFT) mode is incorporated in the SMJ44100. A $\overline{CBR}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data-out pin goes high. If any one bit is different, the data-out pin goes low. Any combination read, write, read-write, or page-mode can be used in test mode. The test mode function reduces test times by enabling the 4M DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

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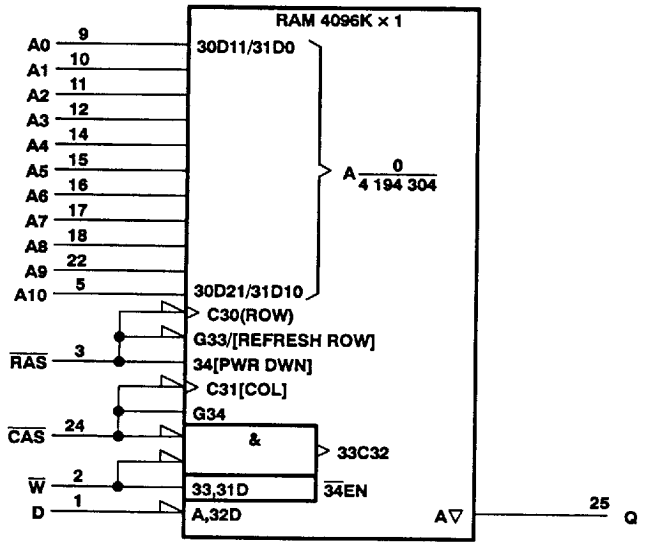
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the HM package.

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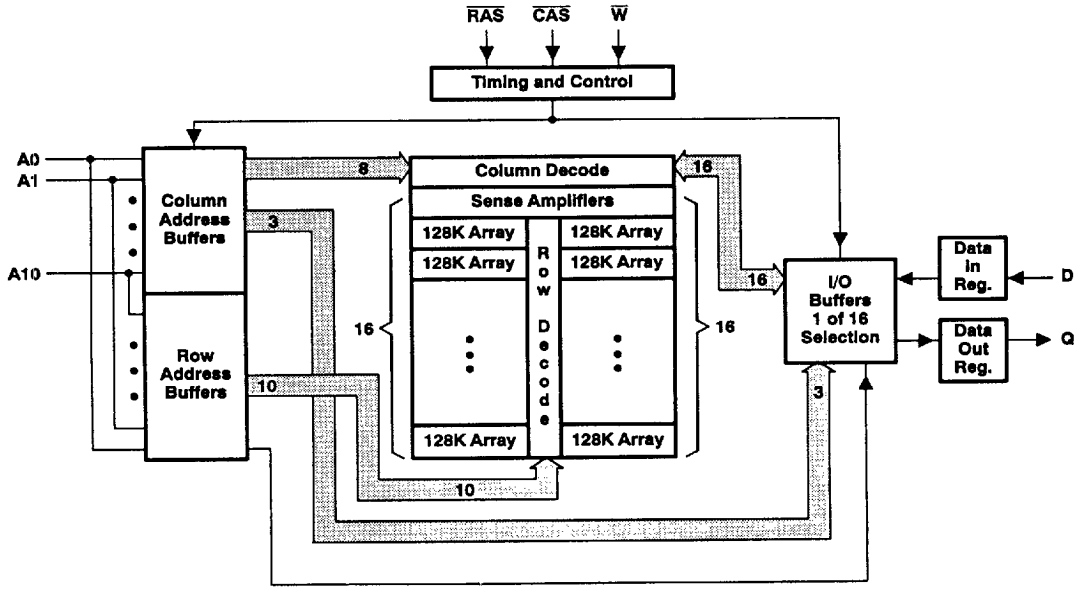
functional block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... – 55°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Minimum operating temperature	– 55			°C
T_C	Maximum operating case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44100-80		'44100-10		'44100-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only, or $\overline{CBR}$) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		40		35	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		7	pF
$C_{i(D)}$	Input capacitance, data inputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		10	pF
$C_{i(W)}$	Input capacitance, write-enable input		10	pF
C_o	Output capacitance		10	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V. Capacitance is sampled only at initial design and after any major change.

switching characteristics over recommended ranges of supply voltage range and operating free-air temperature

PARAMETER		'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		40		50		55	ns
t_{CAC}	Access time from $\overline{CAS}$ low		20		25		30	ns
t_{CPA}	Access time from column precharge		45		50		55	ns
t_{RAC}	Access time from $\overline{RAS}$ low		80		100		120	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)		20		25		30	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven. The output is disabled when $\overline{CAS}$ is brought high.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	150		180		210		ns
t_{RWC}	Cycle time, read-write	175		210		245		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	50		60		65		ns
t_{PRWC}	Cycle time, page-mode read-write	70		85		95		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low (see Note 9)	80	100 000	100	100 000	120	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 9)	80	10 000	100	10 000	120	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	25	10 000	30	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		15		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	60		70		80		ns
t_{WP}	Pulse duration, write	15		20		25		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 11)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	20		25		30		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	20		25		30		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	15		20		20		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low	60		75		90		ns
t_{DH}	Hold time, data (see Note 11)	15		20		25		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	60		75		90		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		15		15		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (early-write operation only)	15		20		25		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	40		50		55		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	20		20		25		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	80		100		120		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)	20		25		30		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The minimum value is measured when t_{RDC} is set to t_{RCD} min as a reference.

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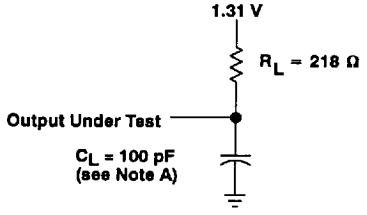
timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

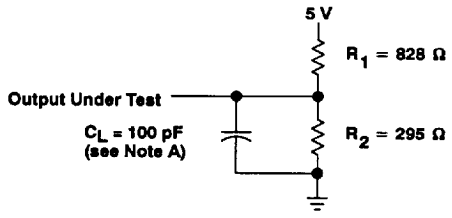
		'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 14)	15	40	20	50	20	65	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	40		50		55		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	40		50		55		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	60	25	75	25	90	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)	80		100		120		ns
t_{CLZ}	$\overline{CAS}$ to output in low Z (see Note 15)	0		0		0		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time (see Note 16)							

NOTES: 14. Maximum value specified only to assure access time.
15. Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.
16. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT



(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

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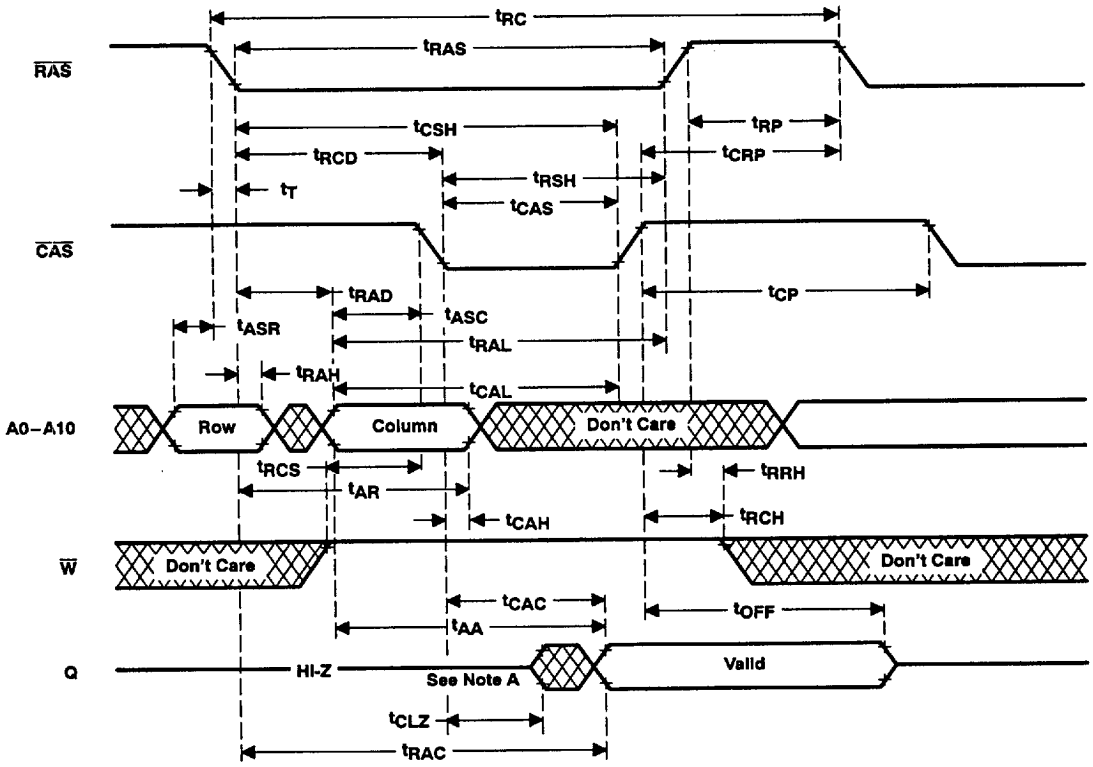

NOTE A: Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 2. Read-Cycle Timing

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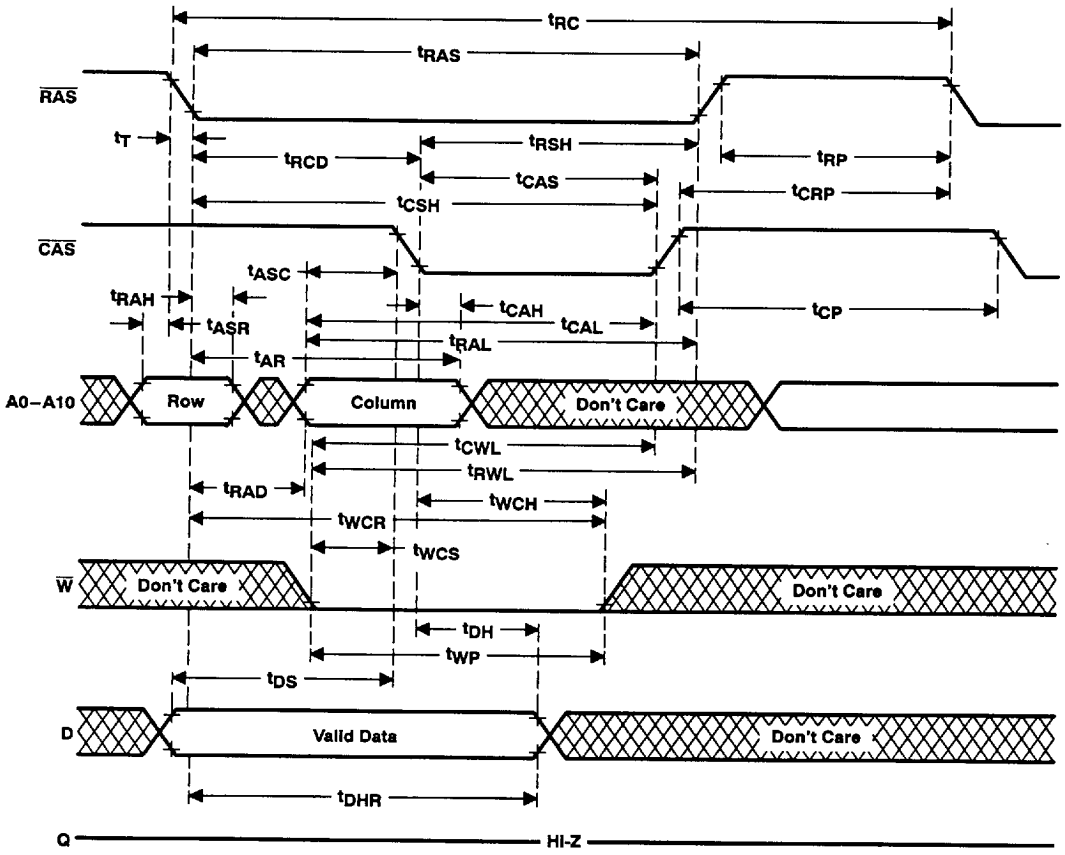

Figure 3. Early-Write-Cycle Timing

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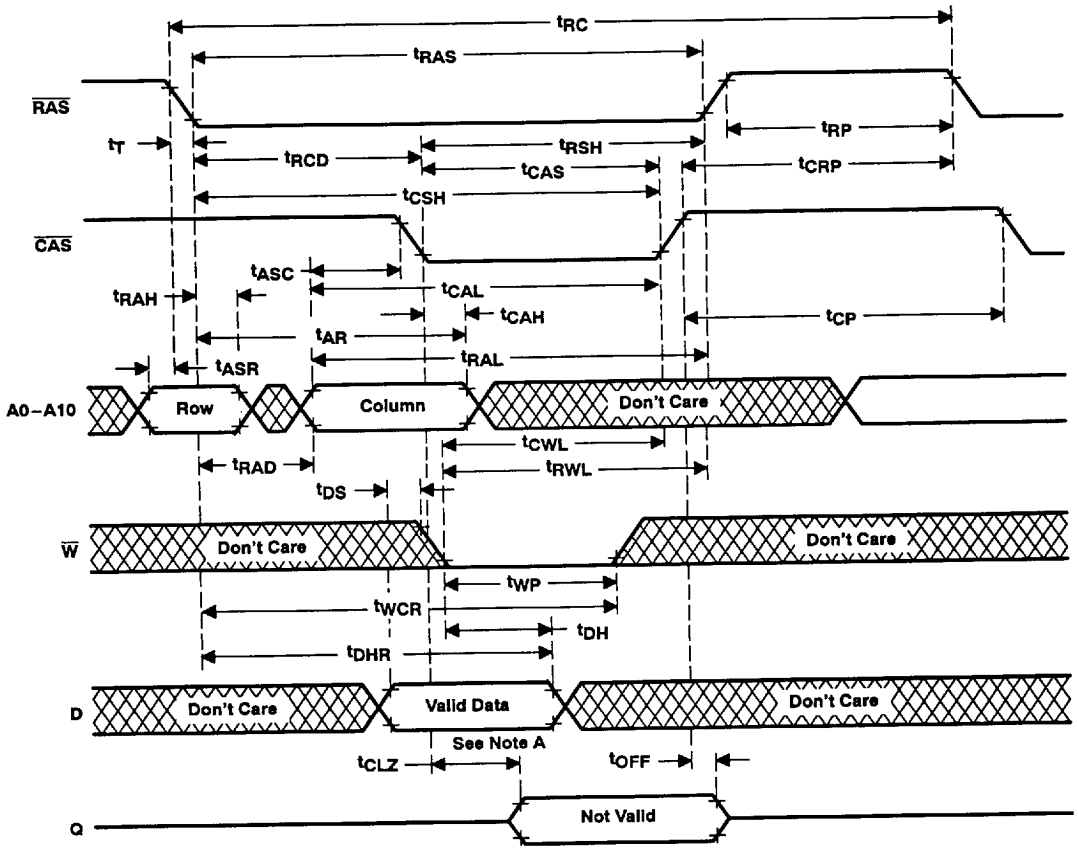

NOTE A: Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 4. Write-Cycle Timing

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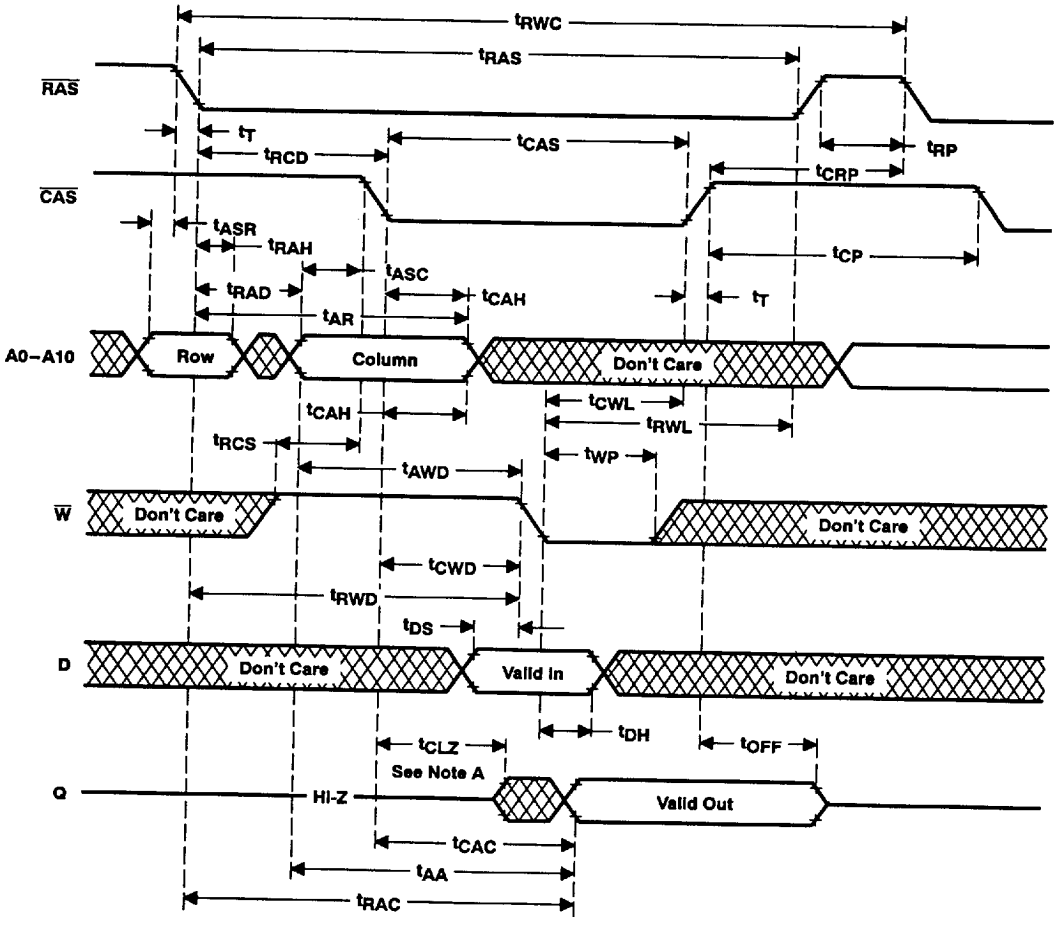
PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 5. Read-Write-Cycle Timing

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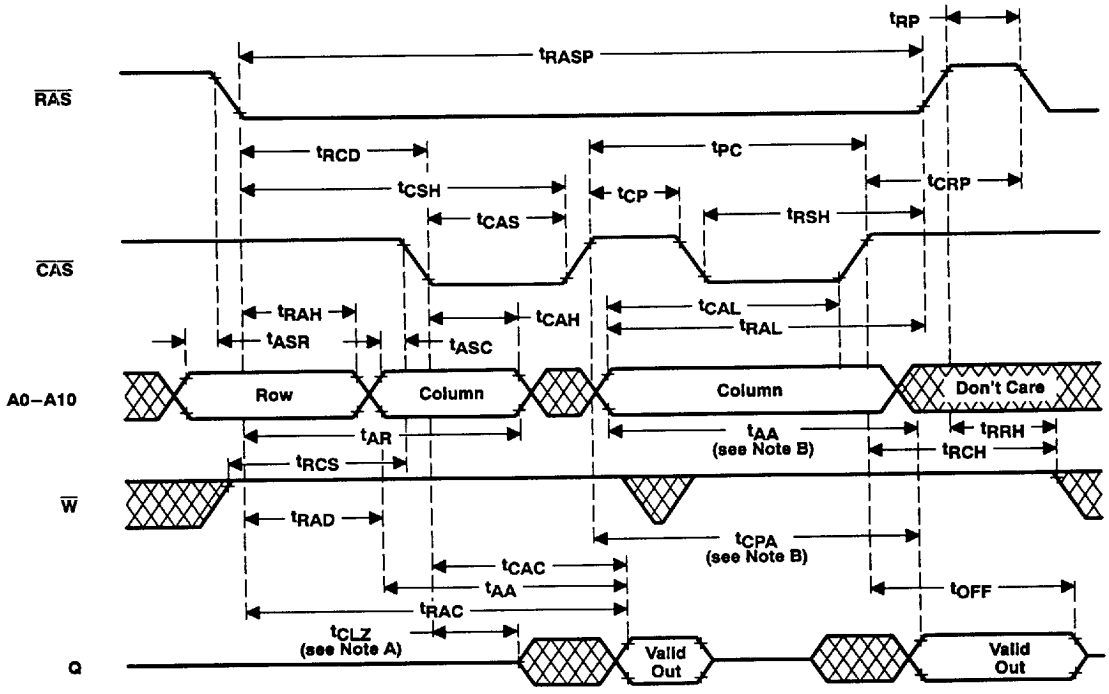
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

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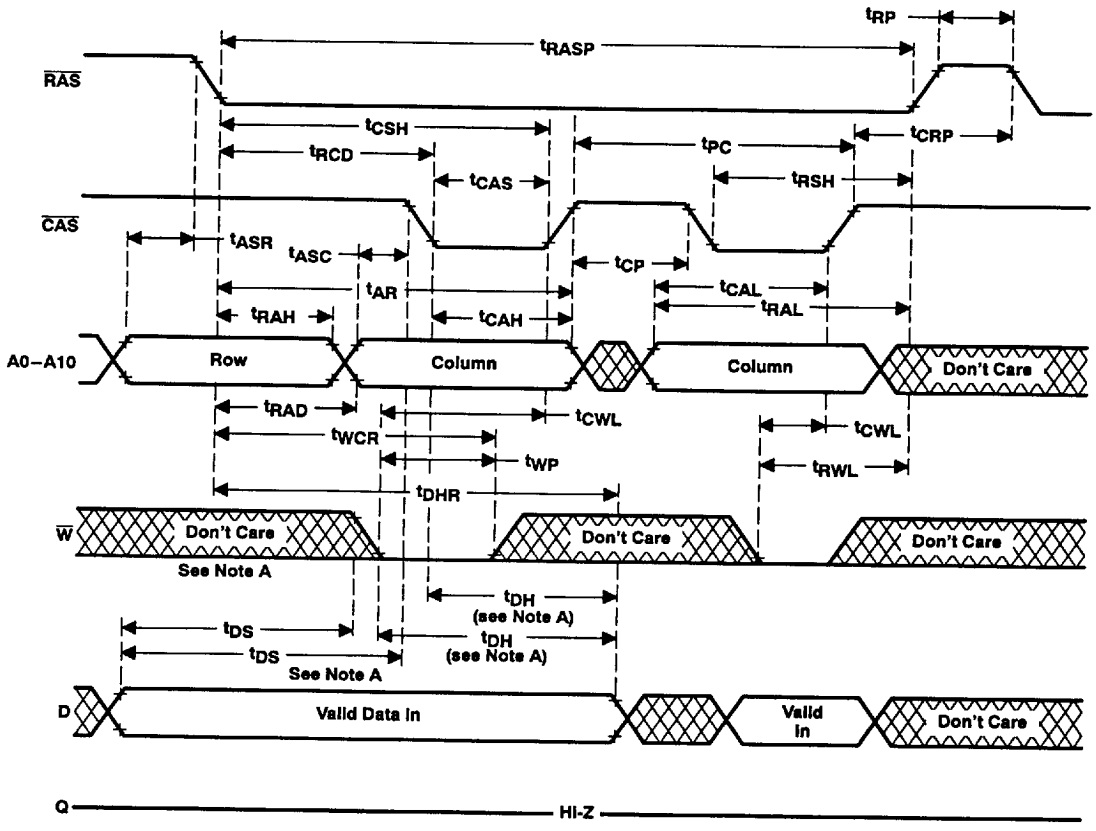
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with a write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

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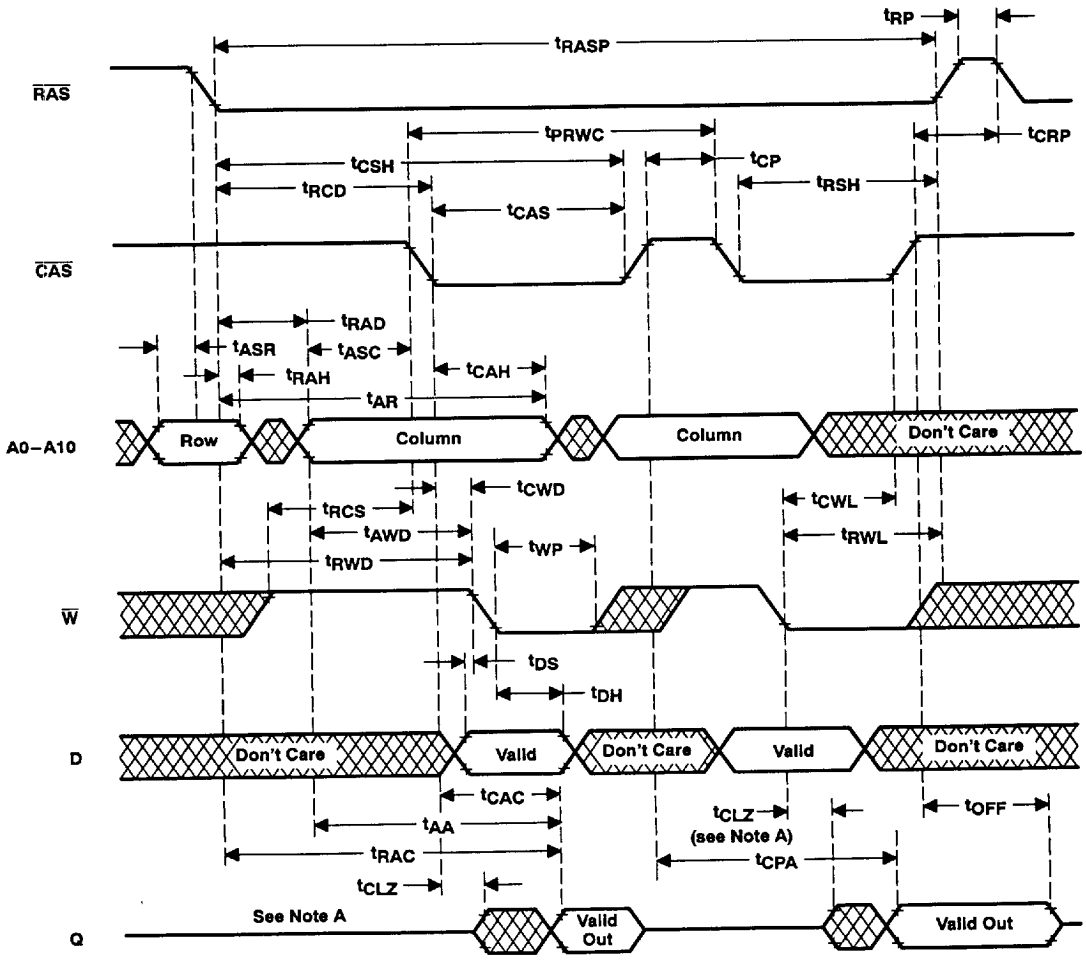
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Valid data is presented at the output after all access times are satisfied. The output can go from the high-impedance state to an invalid-data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Write-Cycle Timing

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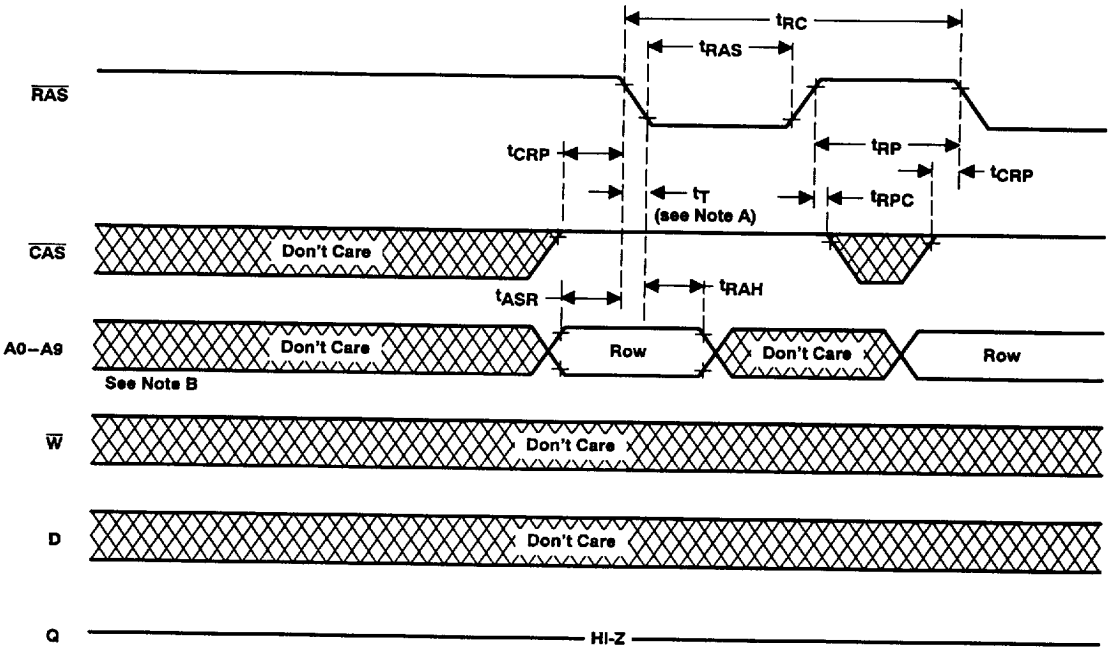

NOTES: A. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.
B. A10 is a don't care.

Figure 9. $\overline{RAS}$-Only Refresh-Cycle Timing

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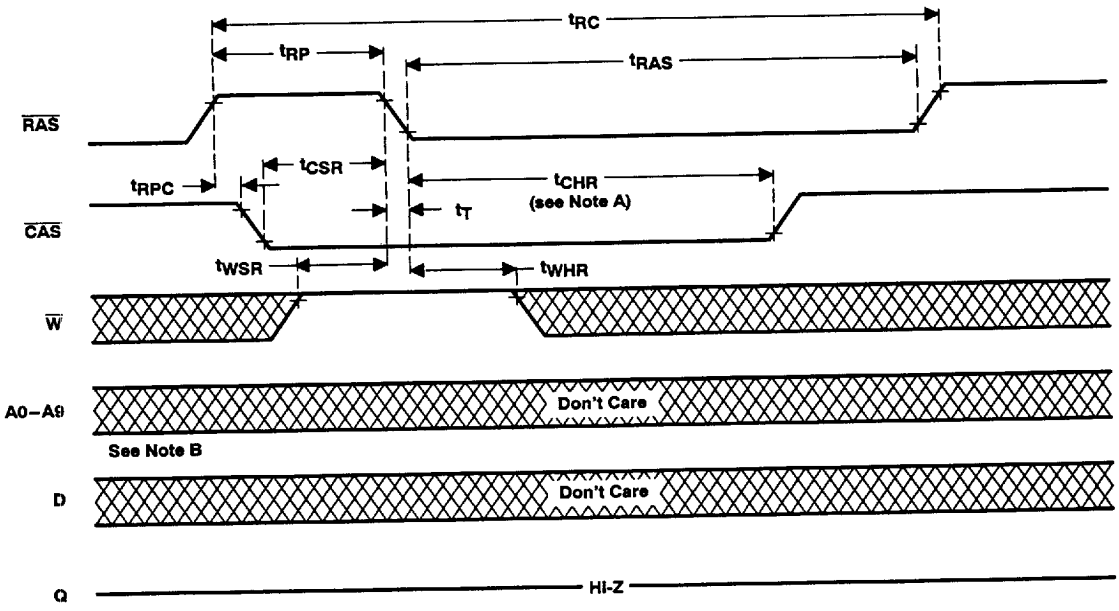
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.
B. A10 is a don't care.

Figure 10. Automatic CBR Refresh-Cycle Timing

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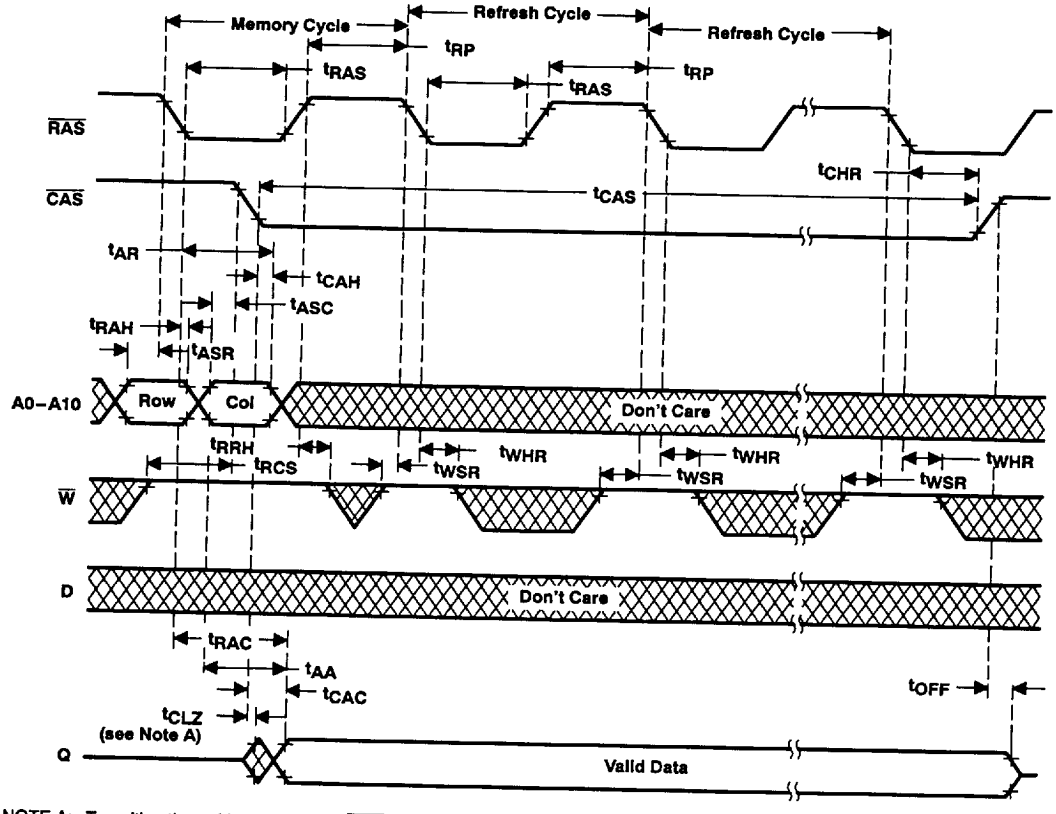

NOTE A: Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.

Figure 11. Hidden-Refresh-Cycle (Read) Timing

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PARAMETER MEASUREMENT INFORMATION

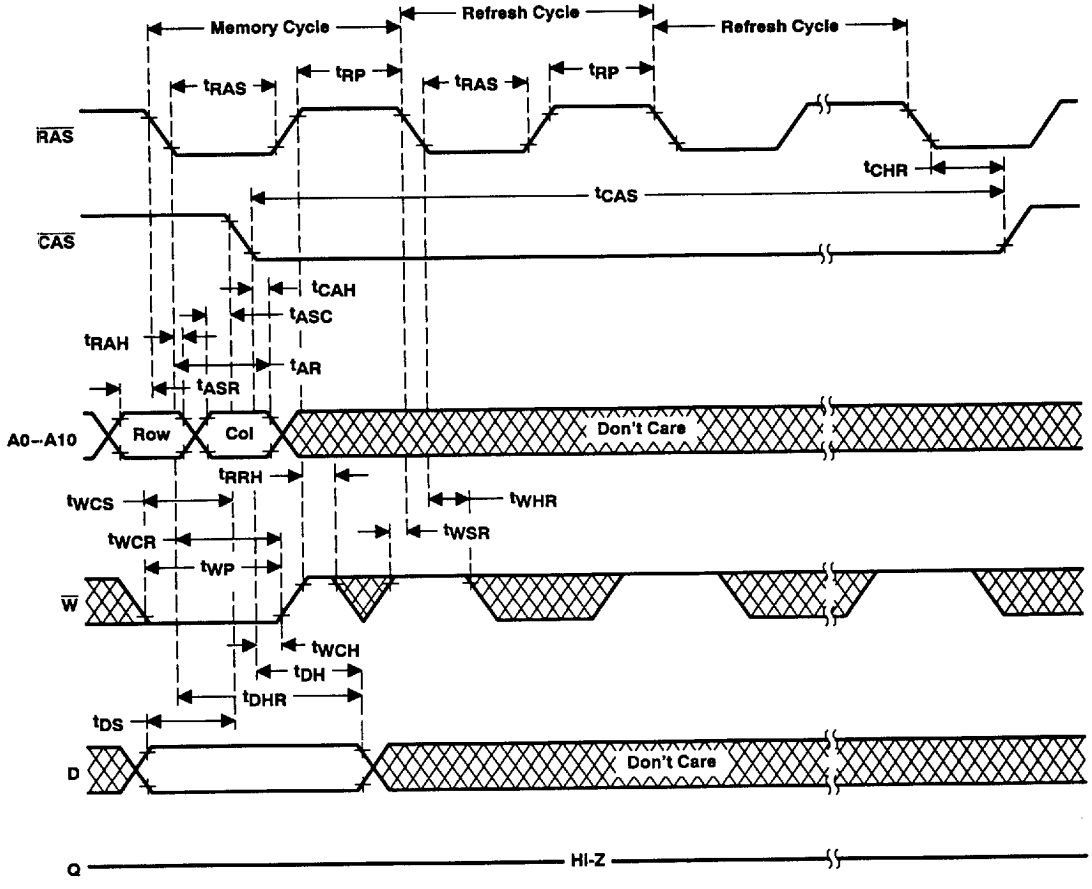

Figure 12. Hidden-Refresh-Cycle (Write) Timing

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