

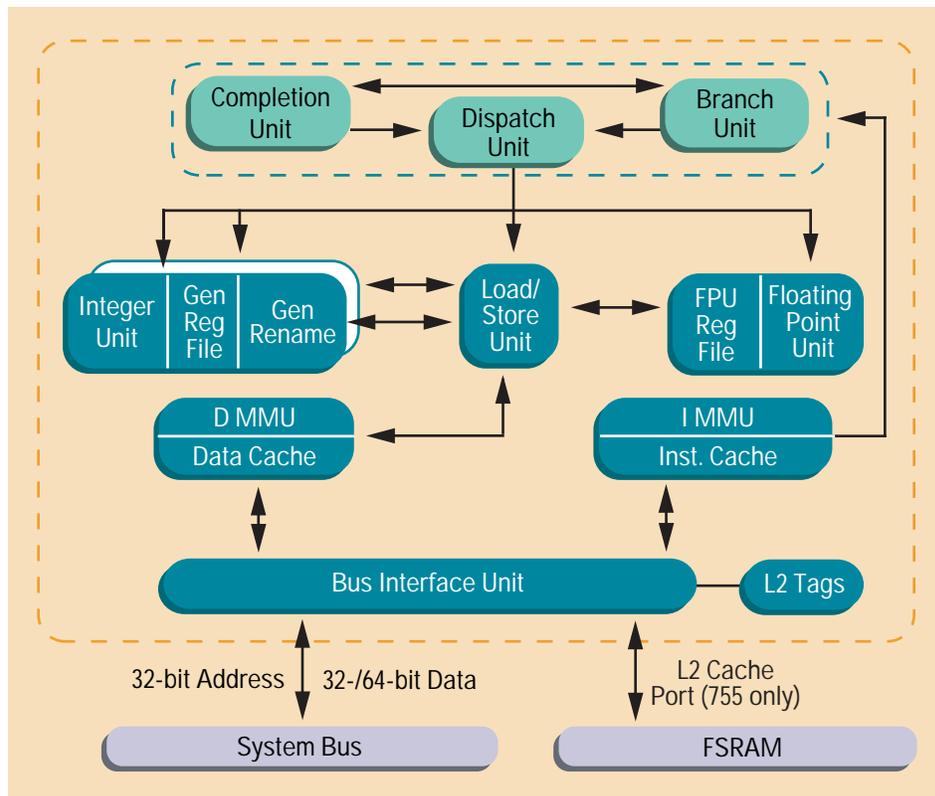
MPC755 and MPC745 microprocessors are high-performance, low-power, 32-bit implementations of the PowerPC architecture, specially enhanced for embedded applications. MPC755 and MPC745 microprocessors differ only in that the MPC755 features an enhanced, dedicated L2 cache interface with on-chip L2 tags. The MPC755 is a drop-in replacement for the award-winning MPC750 microprocessor and is footprint- and user software code-compatible with the MPC7400 microprocessor with AltiVec™ technology. The MPC745 is a drop-in replacement for the MPC740 microprocessor and is also footprint- and user software code-compatible with Motorola G2 microprocessors. MPC755/MPC745 microprocessors provide on-chip debug support and are fully JTAG-compliant.

SUPERSCALAR MICROPROCESSOR

MPC755 and MPC745 microprocessors are superscalar, capable of issuing three instructions per clock cycle (two instructions + branch) into six independent execution units:

- Two integer units
- Load/store unit
- Double-precision floating-point unit
- System register unit
- Branch processing unit

MOTOROLA MPC755/MPC745 BLOCK DIAGRAM



| | MPC745 300-350 MHz | MPC755 300-400 MHz |
|-----------------------------------|---|---|
| CPU Speeds – Internal | 300 and 350 MHz | 300, 350 and 400 MHz |
| CPU Bus Dividers | x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8, x10 | x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8, x10 |
| Bus Interface | 32/64-bit | 32/64-bit |
| Instructions per Clock | 3 (2 + Branch) | 3 (2 + Branch) |
| L1 Cache | 32 KB instruction 32 KB data | 32 KB instruction 32 KB data |
| L2 Cache | — | 256, 512 KB 1 MB |
| Core-to-L2 Frequency | — | 1:1, 1.5:1, 2:1, 2.5:1, 3:1 |
| Typical/Maximum Power Dissipation | TBD | TBD |
| Die Size | 51 mm ² | 51 mm ² |
| Package | 255 PBGA | 360 PBGA |
| Process | 0.22µ 5LM | 0.22µ 5LM |
| Voltage | 1.8/3.3V I/O, 2.0V internal | 1.8/3.3V I/O, 2.0V internal |
| SPECint95 (estimated) | 15.7 @ 350 MHz | 18.1 @ 400 MHz |
| SPECfp95 (estimated) | 11.6 @ 350 MHz | 12.3 @ 400 MHz |
| Other Performance | 641 MIPS @ 350 MHz | 733 MIPS @ 400 MHz |
| Execution Units | Integer(2), Floating-Point, Branch, Load/Store, System Register | Integer(2), Floating-Point, Branch, Load/Store, System Register |

MPC755/MPC745 microprocessors contain separate memory management units (MMUs) for instructions and data, supporting 4 petabytes (2^{52}) of virtual memory and 4 GB (2^{32}) of physical memory. Both feature eight instruction block address translation (iBAT) and eight data block address translation (dBAT) registers. Access privileges and memory protection are controlled on block or page granularities. Large, 128-entry translation lookaside buffers (TLBs) provide efficient physical address translation and support for virtual-memory management on both page- and variable-sized blocks. Both hardware and software tablewalks are provided for the TLBs.

The ability to execute multiple instructions in parallel, the ability to pipeline instructions, and the use of simple instructions with rapid execution times yields maximum efficiency and throughput for MPC755 and MPC745 systems.

POWER MANAGEMENT

The MPC755 and MPC745 microprocessors feature a low-power 2.0V design with three power-saving user-programmable modes—doze, nap, and sleep—which progressively reduce the power drawn by the processor.

These low-power microprocessors offer dynamic power management to selectively activate functional units as they are needed by the executing instructions. Both microprocessors also provide a thermal assist unit and instruction cache throttling for software-controllable thermal management.

CACHE AND MMU SUPPORT

The MPC755/MPC745 microprocessors have separate 32 KB, physically addressed instruction and data caches. Both caches can be locked in part or whole to provide storage of critical data, key performance algorithms, or code loops for fast response time. The MPC755 microprocessor's dedicated L2 cache interface with on-chip L2 tags (up to 1 MB) features support for direct-mapped SRAM mode, physically mapped SRAM mode, a fast (typically 1/2 core speed) interface to memory, instruction-only or data-only modes, and parity checking on both L2 address and data.

FLEXIBLE BUS INTERFACE

MPC755/MPC745 microprocessors have a 64-bit data bus with 32-bit mode and a 32-bit address bus. Support is included for burst, split, and pipelined transactions. The interface provides snooping for data cache coherency. Both microprocessors maintain MEI coherency protocol in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

CONTACT INFORMATION

Motorola offers user's manuals, application notes, and sample code for all of its processors. Local support for these products is also provided. This information can be found at: <http://motorola.com/smartnetworks>

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at: Phone: 800-521-6274 or <http://motorola.com/semiconductors>



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