

SN74ALVC16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS259 – NOVEMBER 1993 – REVISED MARCH 1994

- Member of the Texas Instruments *Widebus+*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- *UBE*™ (Universal Bus Exchanger) Allows Synchronous Data Exchange
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74ALVC16409 allows synchronous data exchange between four different buses.

Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input, provided the select-enable ($\overline{\text{SELEN}}$) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of the CLK, provided $\overline{\text{SELEN}}$ is high.

The data-flow control logic is designed to allow glitch-free data transmission.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16409 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16409 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

PRE	1	56	CLK
SEL0	2	55	$\overline{\text{SELEN}}$
1A1	3	54	1B1
GND	4	53	GND
1A2	5	52	1B2
1A3	6	51	1B3
V_{CC}	7	50	V_{CC}
1A4	8	49	1B4
1A5	9	48	1B5
1A6	10	47	1B6
GND	11	46	GND
1A7	12	45	1B7
1A8	13	44	1B8
1A9	14	43	1B9
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2A9	26	31	2B9
SEL1	27	30	SEL4
SEL2	28	29	SEL3

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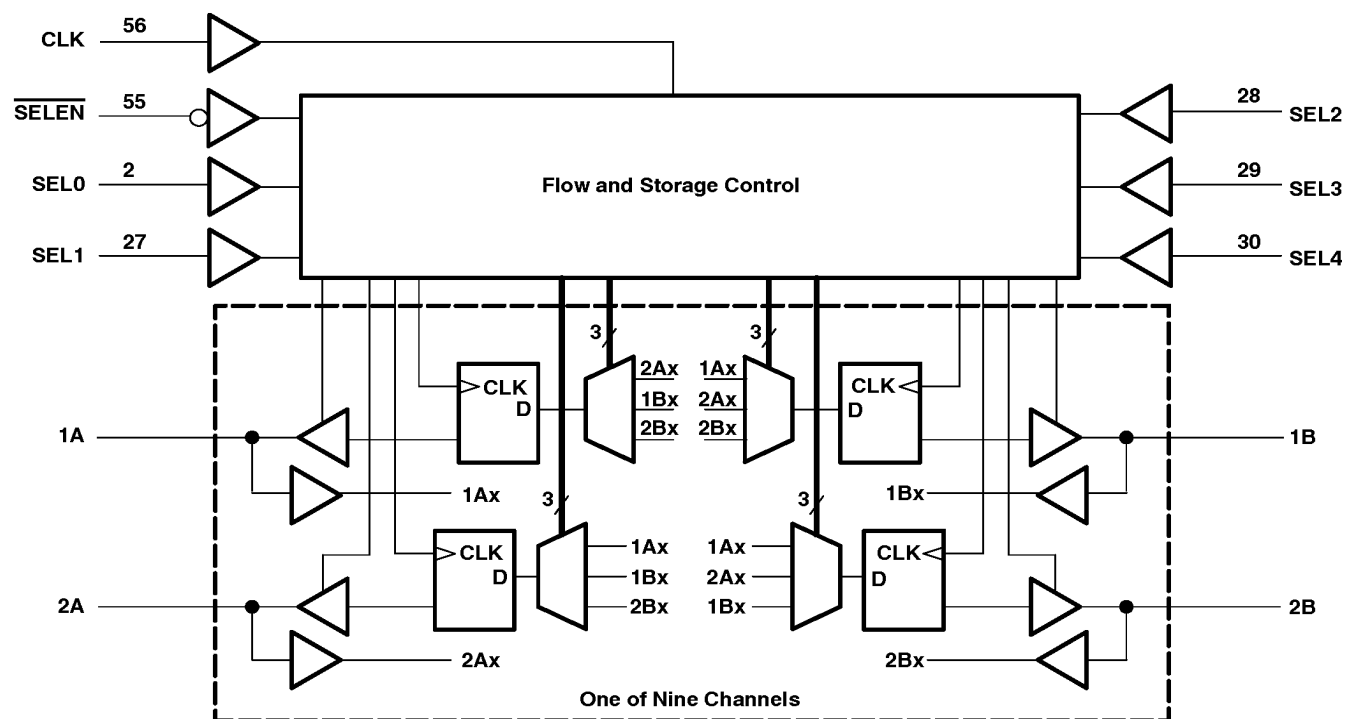
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logic diagram (positive logic)



FUNCTION TABLE

INPUTS		OUTPUT RECEIVE PORT
CLK	SEND PORT	
X	X	$B_0^\dagger$
X	L	L
X	H	H
$\uparrow$	L	L
$\uparrow$	H	H
H	X	$B_0^\dagger$
L	X	$B_0^\dagger$

† Output level before the indicated steady-state input conditions were established.

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DATA-FLOW CONTROL FUNCTION TABLE

INPUTS							DATA FLOW
SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	↑	X	X	X	X	X	No change
L	↑	0	0	0	0	0	None, all I/Os off
L	↑	0	0	0	0	1	Not used
L	↑	0	0	0	1	0	Not used
L	↑	0	0	0	1	1	Not used
L	↑	0	0	1	0	0	Not used
L	↑	0	0	1	0	1	Not used
L	↑	0	0	1	1	0	Not used
L	↑	0	0	1	1	1	Not used
L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	↑	0	1	0	0	1	2A to 1A
L	↑	0	1	0	1	0	2B to 1B
L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	↑	0	1	1	0	1	1A to 2A
L	↑	0	1	1	1	0	1B to 2B
L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	↑	1	0	0	0	1	1A to 1B
L	↑	1	0	0	1	0	2A to 2B
L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	↑	1	0	1	0	1	1B to 1A
L	↑	1	0	1	1	0	2B to 2A
L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	↑	1	1	0	0	1	1B to 2A
L	↑	1	1	0	1	0	2B to 1A
L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	↑	1	1	1	0	1	1A to 2B
L	↑	1	1	1	1	0	2A to 1B
L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1.4 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		–12	mA
		$V_{CC} = 3$ V		–24 [‡]	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12	mA
		$V_{CC} = 3$ V		24 [‡]	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

[‡] Current duty cycle ≤ 50%, $f \geq 1$ kHz

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}^{\dagger}$	MIN	TYP	MAX	UNIT
V_{IK}		$I_I = -18\text{ mA}$	2.7 V			-1.2	V
V_{OH}		$I_{OH} = -100\text{ }\mu\text{A}$	MIN to MAX	$V_{CC}-0.2$			V
		$I_{OH} = -12\text{ mA}$	2.7 V	2.2			
			3 V	2.4			
			$I_{OH} = -24\text{ mA}$	3 V	2		
V_{OL}		$I_{OL} = 100\text{ }\mu\text{A}$	MIN to MAX			0.2	V
		$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
		$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
$I_{I(\text{hold})}$	Data pins	$V_I = 0.8\text{ V}$	3 V	75			μA
		$V_I = 2\text{ V}$		-75			
$I_{OZ}^{\ddagger}$		$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μA
ΔI_{CC}		$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND				750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			$V_{CC} = 3.3 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	MAX	MIN	MAX	MIN	
f_{clock}	Clock frequency		0	75				MHz
t_w	Pulse duration	CLK high or low						ns
t_{su}	Setup time	A or B before CLK $\uparrow$		0.8				ns
		S before CLK $\uparrow$		5				
		SELEN before CLK $\uparrow$						
t_h	Hold time	A or B after CLK $\uparrow$		2				ns
		S after CLK $\uparrow$		0.5				
		SELEN after CLK $\uparrow$						

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.15 \text{ V}$			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$	UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MAX	
f_{max}			75							MHz
t_{pd}	CLK (A or B)	B or A	4							ns
t_{en}	CLK (SEL)	B or A								ns
t_{dis}	CLK (SEL)	B or A								ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



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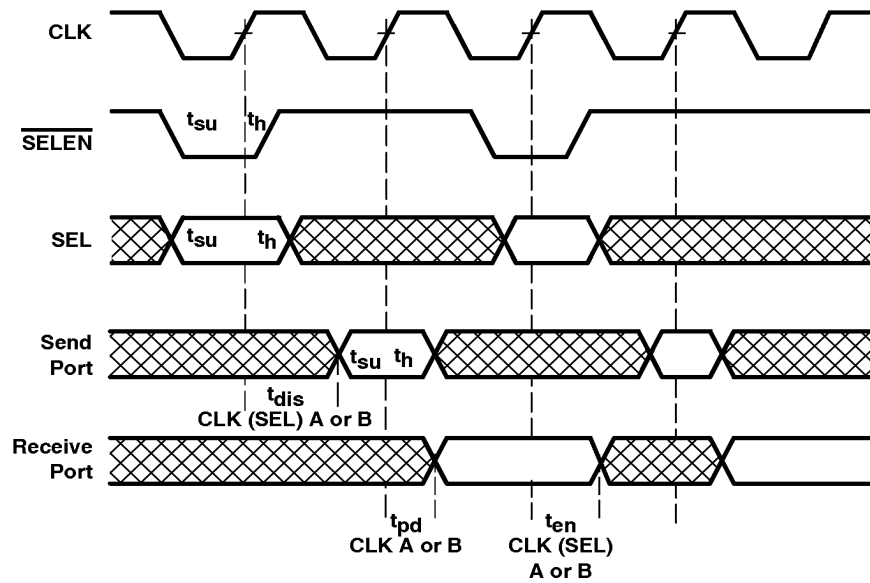
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timing diagram



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