



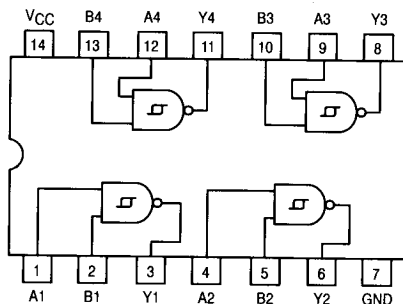
Quad 2-Input Schmitt-Trigger Positive NAND Gate

**ELECTRICALLY TESTED PER:
MIL-M-38510/31303**

The 54LS132 contains four 2-input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+} (MAX).

LOGIC DIAGRAM



Military 54LS132



AVAILABLE AS:

- 1) JAN: JM38510/31303BXA
- 2) SMD: N/A
- 3) 883: 54LS132/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

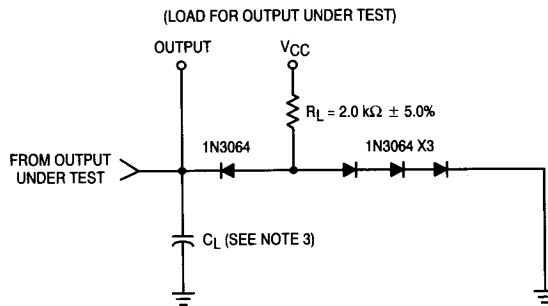
PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
B1	2	2	3	GND
Y1	3	3	4	VCC
A2	4	4	6	VCC
B2	5	5	8	GND
Y2	6	6	9	VCC
GND	7	7	10	GND
Y3	8	8	12	VCC
A2	9	9	13	VCC
B3	10	10	14	GND
Y4	11	11	16	VCC
A4	12	12	18	VCC
B4	13	13	19	GND
VCC	14	14	20	VCC

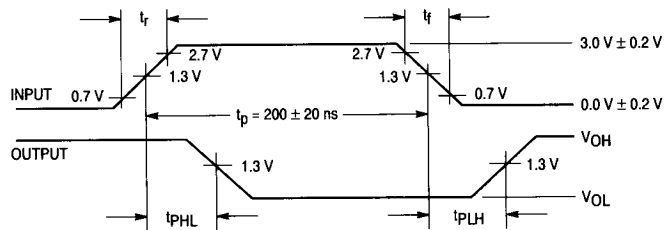
BURN-IN CONDITIONS:
 $V_{CC} = 5.0 \text{ V MIN}/6.0 \text{ V MAX}$

54LS132

AC TEST CIRCUIT



WAVEFORMS



NOTES:

1. The pulse generator has the following characteristics:
 $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $\text{PRR} \leq 1.0 \text{ MHz}$, and $Z_{OUT} = 50 \Omega$.
2. All diodes are 1N3064 or equivalent.
3. $C_L = 50 \text{ pF} \pm 10\%$, including scope probe and jig capacitance.
4. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

54LS132

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH1}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = –0.4 mA, V _{IL} = 0.5 V, V _{IN} = 1.9 V on other inputs.
V _{OL1}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IH} = 1.9 V on both inputs.
V _{OH2}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 5.0 V, I _{OH} = –0.4 mA, V _{IL} = 1.9 V, other input = (See Note 2).
V _{OL2}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 5.0 V, I _{OL} = 4.0 mA, V _{IN} = (See Note 3).
V _{IC}	Input Clamping Voltage		–1.5					V	V _{CC} = 4.5 V, I _{IN} = –18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other input = 0 V.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other input = 0 V.
I _{IL}	Logical "0" Input Current	–0.12	–0.36	–0.12	–0.36	–0.12	–0.36	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, other input = 5.5 V.
I _{OS}	Output Short Circuit Current	–15	–100	–15	–100	–15	–100	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (both inputs), V _{OUT} = 0 V.
I _{CCH}	Power Supply Current		11		11		11	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (both inputs).
I _{CCL}	Power Supply Current		14		14		14	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (both inputs).
V _{IH}	Logical "1" Input Voltage	1.9		1.9		1.9		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL} t _{PHL}	Propagation Delay /Data-Output Output High-Low	5.0 —	32 22	5.0 —	52 47	5.0 —	52 47	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PLH} t _{PLH}	Propagation Delay /Data-Output Output Low-High	5.0 —	32 22	5.0 —	52 47	5.0 —	52 47	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.

NOTES:

1. The limits specified for C_L = 15 pF are guaranteed but not tested.
2. Momentary 0.5 V, then 1.4 V without overshoot during test.
3. Momentary 1.9 V, then 1.0 V without undershoot during test.