MOTOROLA

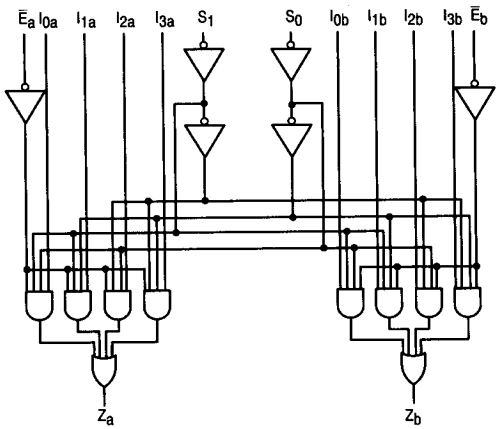
Dual 4-Input Data Selector/Multiplexer (with Enable)

ELECTRICALLY TESTED PER:
MIL-M-38510/30902

The 54LS153 is a very high-speed Dual 4-input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'LS153 can generate any two functions of three variables. The 'LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Non-Inverting Outputs
- Separate Enable for Each Multiplexer
- Input Clamp Diode Limits High-Speed Termination Effects

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The 'LS153 is a Dual 4-Input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The 'LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{0b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

The 'LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The 'LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

Military 54LS153

AVAILABLE AS:

1) JAN: JM38510/30902BXA
2) SMD: 7601101
3) 883: 54LS153/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{E}_a$	1	1	2	GND
S_1	2	2	3	V_{CC}
I_{3a}	3	3	4	V_{CC}
I_{2a}	4	4	5	V_{CC}
I_{1a}	5	5	7	V_{CC}
I_{0a}	6	6	8	V_{CC}
Z_a	7	7	9	V_{CC}
GND	8	8	10	GND
Z_b	9	9	12	V_{CC}
I_{0b}	10	10	13	V_{CC}
I_{1b}	11	11	14	V_{CC}
I_{2b}	12	12	15	V_{CC}
I_{3b}	13	13	17	V_{CC}
S_0	14	14	18	V_{CC}
$\overline{E}_b$	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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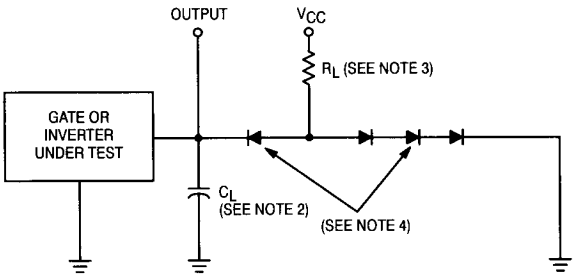
TRUTH TABLE							
Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Immaterial

LOAD FOR OUTPUT UNDER TEST



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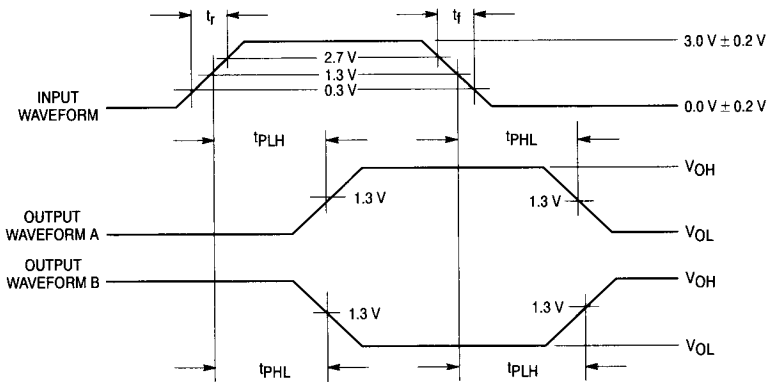
WAVEFORMS



REFERENCE NOTES ON PAGE 5-161

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_{IH} = 2.0 V, other inputs are open, S = 0.7 V, $\overline{E}$ = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, $\overline{E}$ = 2.0 V, all other inputs are open.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are GND, $\overline{E}$ = 2.7 V, 5.5 V or GND, S = 2.7 V, 5.5 V or GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are GND, $\overline{E}$ = 5.5 V, or GND, S = 5.5 V or GND.
$I_{IL(E)}$	Logical "0" Input Current	−0.16	−0.4	−0.16	−0.4	−0.16	−0.4	mA	V_{CC} = 5.5 V, $\overline{E}$ = 0.4 V, S = GND, other inputs are open.
$I_{IL(S)}$	Logical "0" Input Current	−0.12	−0.36	−0.12	−0.36	−0.12	−0.36	mA	V_{CC} = 5.5 V, $\overline{E}$ = GND, S = 0.4 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−0.16	−0.4	−0.16	−0.4	−0.16	−0.4	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V, $\overline{E}$ = GND.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, all other inputs are GND, V_{OUT} = GND.
I_{CC}	Power Supply Current		10		10		10	mA	V_{CC} = 5.5 V, all inputs = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:
1. Input pulse characteristics: PRR ≤ 1.0 MHz, t_r = 15 ns, t_f ≤ 6.0 ns.
2. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
3. R_L = 2.0 kΩ ± 5.0%.
4. All diodes are 1N3064 or 1N916.
5. The limits specified for C_L = 15 pF are guaranteed but not tested.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output I_a or I_b to Z_a or Z_b	3.0 —	31 26	3.0 —	47 42	3.0 —	47 42	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output I_a or I_b to Z_a or Z_b	3.0 —	20 15	3.0 —	30 25	3.0 —	30 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL3} t_{PHL3}	Propagation Delay /Data-Output $\overline{E}_a$ or $\overline{E}_b$ to Z_a or Z_b	3.0 —	37 32	3.0 —	56 51	3.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH3} t_{PLH3}	Propagation Delay /Data-Output $\overline{E}_a$ or $\overline{E}_b$ to Z_a or Z_b	3.0 —	29 24	3.0 —	44 39	3.0 —	44 39	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output S_0 or S_1 to Z_a or Z_b	3.0 —	43 38	3.0 —	65 60	3.0 —	65 60	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH5} t_{PLH5}	Propagation Delay /Data-Output S_0 or S_1 to Z_a or Z_b	3.0 —	34 29	3.0 —	51 46	3.0 —	51 46	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

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