Telecom Instrumentation Filter

GENERAL DESCRIPTION

The XR-1020A is a data communication/telecommunication instrumentation filter. This device provides ten of the filters used to characterize communication links for both IEEE/Bell and CCITT standards. The filters are:

1. C-message weighting filter
2. C-notch filter (1010Hz)
3. Psophometric filter (CCITT equivalent of C-message weighting filter)
4. CCITT psophometric notch filter (825Hz)
5. Program weighting filter
6. 3kHz flat filter
7. 15kHz flat filter
8. 1kHz band-pass filter (phase jitter measurements)
9. 50 kilobit filter (low-pass filter partion only)
10. Peak-to-average ratio band-pass filter (P/AR)

The control and selection of the ten filters is achieved with an eight bit microprocessor bus structure, complete with a strobe line ($\overline{S}$) and chip select ($\overline{CS}$). This simplifies the control of the filter functions. On-chip reconstruction filters provide the smoothing of the signals needed for precise measurements. The XR-1020A provides lower output noise then the original XR-1020.

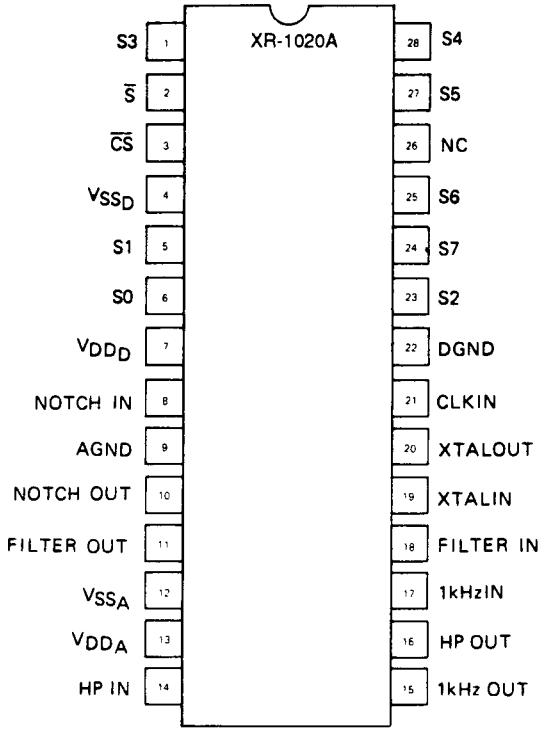
The XR-1020A uses a single 3.579545MHz crystal to provide the clock needed for the switched capacitor filters. This creates a nearly self-contained unit, requiring only digital controls for the filter selection. Additional external clock input is provided if a crystal controlled clock cannot be obtained. Also included is a power down mode allowing the device to be used in battery operated applications.

The XR-1020A uses switched capacitor techniques to implement the filter functions. The XR-1020A is fabricated in 3 micron polysilicon gate CMOS process for low noise.

FEATURES

Ten Filters Provided in One 28 Pin Dual In-Line (DIP) Package
Microprocessor Bus Interface
Low Noise
Power Down Mode for Battery Operation
3.579MHz Clock Operation with On-chip Oscillator
Separate Notch Filter Output
Separate 1 kHz Band-Pass (Phase Jitter Measurements) Filter Output
TTL/CMOS Compatible Digital Inputs
On-chip Output Smoothing Filters

PIN ASSIGNMENT



APPLICATIONS

Telephone Impairment Measurement Sets (TIMS)
C-message Weighted Meters
Telecommunication Test Instruments
Audio Test Systems
General Instrumentation Purposes
Network Management Systems

ABSOLUTE MAXIMUM RATINGS

Power Supply (Relative to V_{SS})	14 VDC
Power Dissipation (Package Limitation)	
Ceramic Package	1.4W
Derate Above 25°C	5mW/°C
Plastic Package	1 W
Derate Above 25°C	6 mW/°C
Operating Temperature	0°C to +70°C
Storage Temperature	65°C to + 150°C
Voltage at any Input	V_{SS} – 0.3 to V_{DD} + 0.3 VDC

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ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1020ACN	Ceramic	0°C to 70°C
XR-1020ACP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-1020A provides most of the filters used to characterize telephone line quality as well as other telecommunication lines. It can be used with a microprocessor, allowing easy selection of a particular filter function.

The XR-1020A supplies the filters for the Bell Systems Technical Reference 41009, the IEEE Standard 743-1984 and the CCITT Series 0 Recommendations. The XR-1020 is used either with an external clock or with a 3,579545MHz Colorburst crystal.

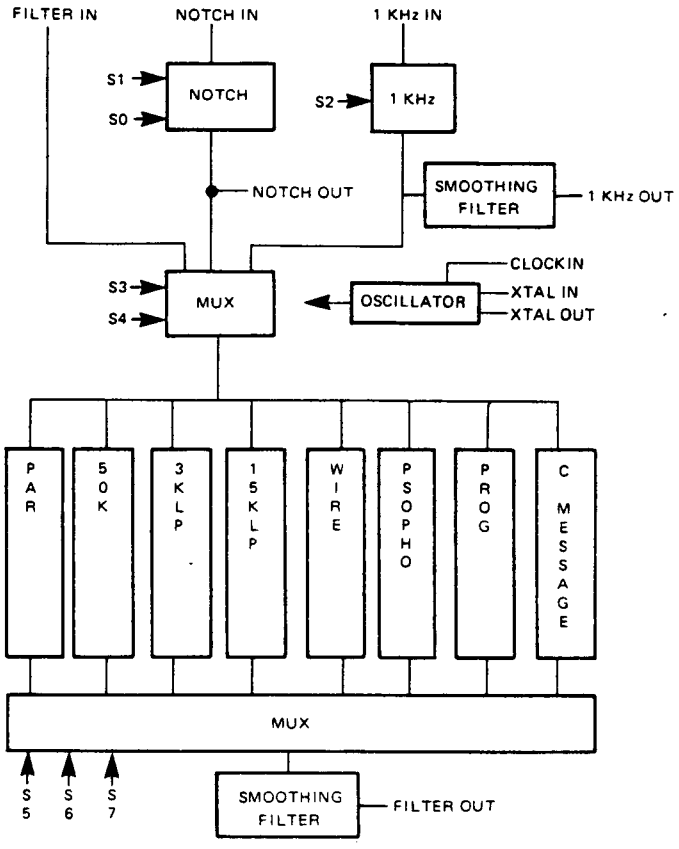
The XR-1020A provides an on-chip latch which allows the device to be memory mapped, that is, considered 8 memory location rather than a special access port. This simplifies the software writing and increases the versatility of the device.

The functional block diagram of the device is illustrated in Figure 1.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +5 VDC, V_{SS} = −5 VDC, R_{load} = 1MΩ, C_{load} = 40pF, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS						
V_{DD}	Positive Supply Voltage					
	Single Supply	9.5	10	10.50	VDC	V_{SS} = 0 VDC
	Split Supply	4.75	5	5.25	VDC	
V_{SS}	Negative Supply Voltage					
	Split Supply	−5.25	−5	−4.75	VDC	
I_{DD}	Positive Supply Current					
	Single Supply		10	14	mA	V_{SS} = 0 VDC
	Split Supply		10	14	mA	
I_{SS}	Negative Supply Current		−10	−14		
BUS INPUT CHARACTERISTICS						
V_{IL}	Input Voltage, Logic Low			0.8	V	
V_{IH}	Input Voltage, Logic High	2.8			V	
I_{IL}	Input Current, Logic Low	−1.0		+1.0	µA	
I_{IH}	Input Current, Logic High	−1.0		+1.0	µA	
t_{CS}	Time for Chip, Select to Latch	100			nS	See Figure 5
t_{SB}	Time for Strobe to Latch	100			nS	See Figure 5
t_{data}	Time for Data to be Stable	150			nS	See Figure 5
t_{delay}	Delay Time from Strobe or Chip Select to Data Change	50			nS	



S1	S0	FUNCTION
X	0	Notch Off (Powered Down)
0	1	1010Hz Notch
1	1	825Hz Notch

S2	FUNCTION
0	1K Off (Powered Down)
1	1K

S4	S3	FUNCTION
0	X	FILTER IN PIN
1	0	NOTCH OUTPUT
1	1	1K OUTPUT

* S4-S3 determine what is selected by the input mux as input to the mode selected by S7-S5.

S7	S6	S5	FUNCTION
0	0	0	PAR
0	0	1	50K
0	1	0	3K LP
0	1	1	15K LP
1	0	0	WIRE
1	0	1	PSOPHOMETRIC
1	1	0	PROG-WEIGH
1	1	1	C MESSAGE

— The 1KHz and NOTCH (825Hz & 1010Hz) filters have separate outputs. The 1KHz output is possed through a smoothing filter. The WIRE mode can be used for smoothing the NOTCH filter output, if desired.

— The highpass portion of the 50K filter (external) is connected in between the HPIN and HPOUT terminals: HPIN is connected to the output of the highpass? HPOUT is connected to the input of the highpass.

— 3.579545MHz colorburst crystal is connected in between the XTALIN and XTALOUT pins. In this case, the CLKIN pin should be connected HI or LO. 20pF capacitors on both sides of the crystal to ground, as well as a 10MΩ resistor across the crystal are needed.

If the above clock frequecy is already available in the system then the CLKIN Pin can be used. In this case, the XTALIN pin should be connected to V_{DD} or to V_{SS}.

— The microcompatibility is controlled by the S (strobe) and CS (chip select) pins. Both inputs must be LO for input to latch.

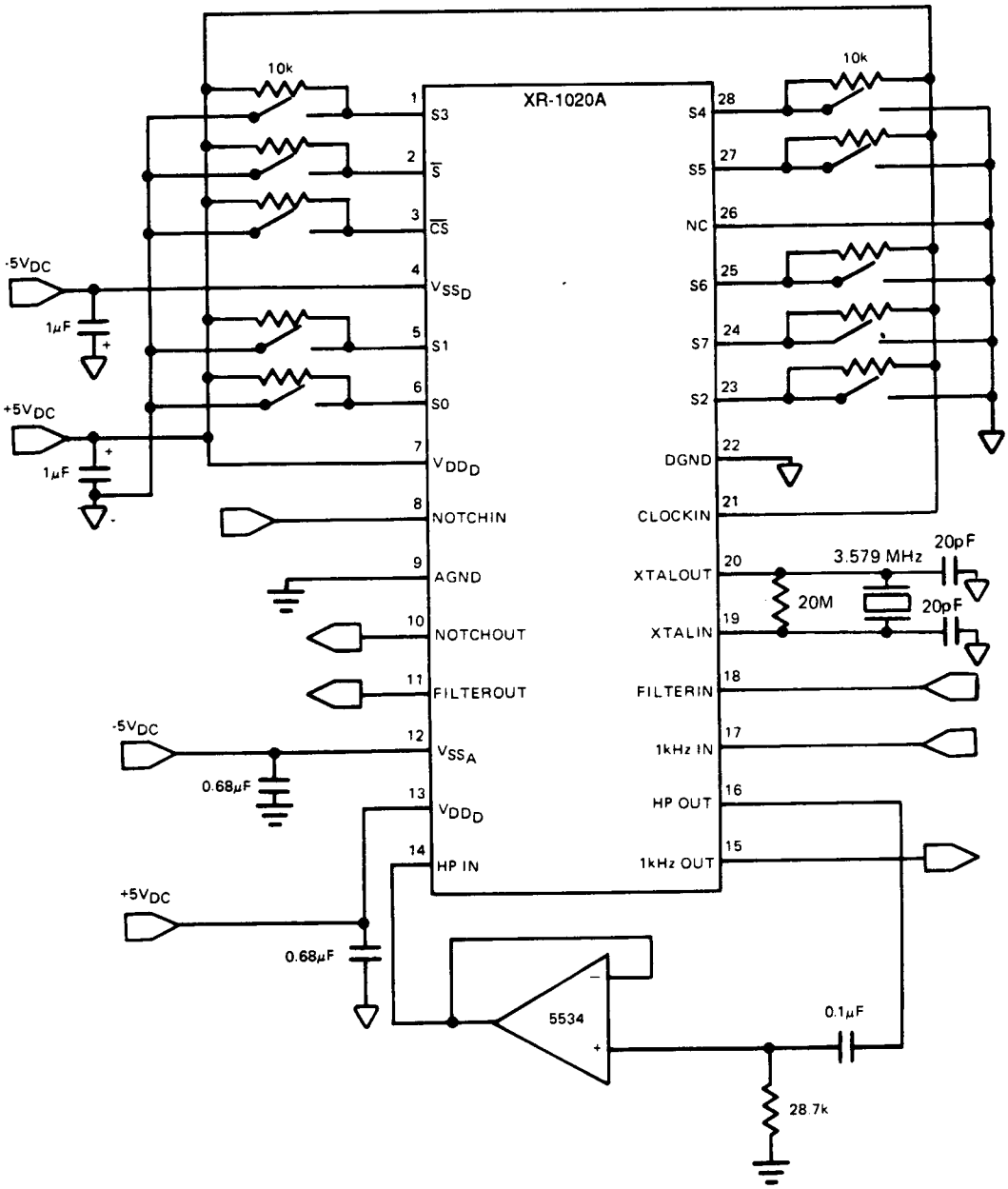


Figure 2. Typical Test Circuit

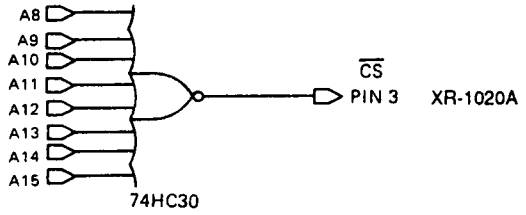


Figure 3. Typical Method for High Order Byte Decoding

SYSTEM DESIGN USING THE XR-1020A

The XR-1020A has been optimized for use with a standard 16 bit wide address bus. A decoder circuit will be needed for using the CS pin of the XR-1020, The lower 8 bits should be tied directly to the S0 through S7 digital inputs of the XR-1020A

The higher order bits, A8 through A15, need a decoder depending upon the system and the present use of the microprocessor. In one application, where location OXFFXX is to be used for the XR-1020A, the 74HC30 can be used for decoding the location. Figure 3 shows the use of the XR-1020A with the 74HC30. When the high order byte is high, the output of the 74HC30 will go low, which would select the XR-1020A for use. With the use of inverters, other locations can be decoded and used.

Figure 1 gives information as to which function is selected. The pin description provides information as to which bit controls which filter function.

The strobe pin, used to latch in the information present on the address bus, can be used when the data lines and lower byte address are multiplexed on the same eight lines.

In applications where a microprocessor will not be used (analog meters or other manual select systems), a decoder can be used such as the 74HC148 to convert the switch information to a binary format. Figure 5 shows the use of the XR-1020A with the 74HC148 for a push button system. The pin descriptions can be used in this application to determine the decoding of the button function of the system.

The use of the 50 kilobit filter requires a 50Hz high-pass filter to be added to the HPOUT and HPIN pins of the XR-1020A. Figure 13 shows the filter shape used for this: The schematic for this first order, continuous time high-pass filter is shown in Figure 1. To prevent degradation of the performance of the XR-1020A, it is recommended that a low noise operational amplifier such as the XR-5532 be used for the filter shaping. Also, the components should be 1% precision in order to prevent the filter shape from changing with production variations. Such a situation may cause peaking in the pass-band response and affect the measurements obtained with the 50 KBPS filter.

If no consideration is given to the layout of the external operational amplifier circuit, additional noise may be added to the signal present on the output of the low-pass reducing the dynamic range of the 50 KBPS amplitude and distortion tests. The feedback trace from the operational amplifier output to the inverting input should be kept as short as possible. This will reduce the chance of any stray noise from being amplified by the filter.

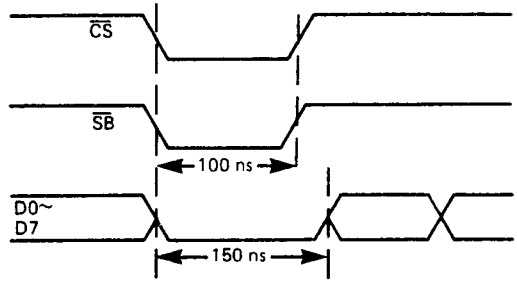


Figure 4. Typical Timing for CS and S Data Bus

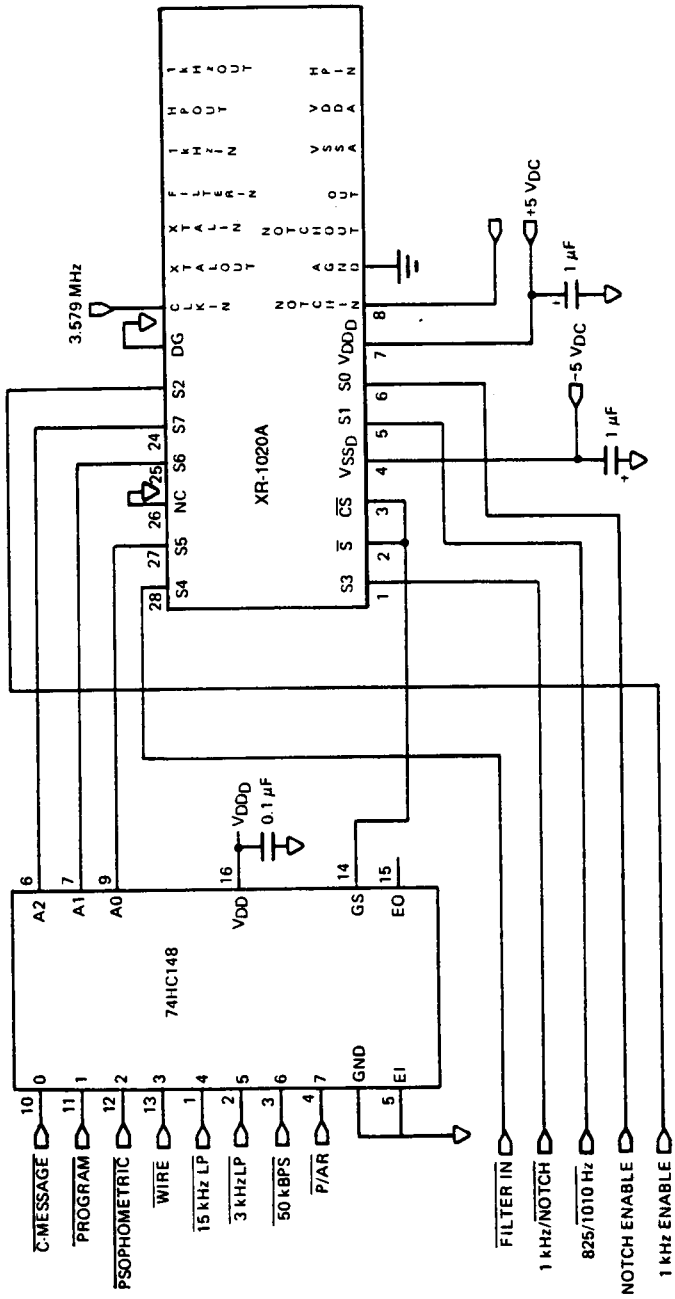


Figure 5. Push Button Interface with the XR-1020 (without microprocessor)

PIN DESCRIPTIONS

Pin#	Symbol	Desciption
1	S3	*Digital Input S3:* This with S4, Pin 28 selects which input is applied to the filter bank as shown in the block diagram.
2	S	*Strobe:* This input, when high, latches in the data present on the lines S0 through S7. When S is high, changes on the address bus will not affect the state of XR-1020A.
3	CS	*Chip Select:* This input, when low, selects the XR-1020A for addressing. The delay between chip select going high and strobing in the new address is 50ns.
4	V_{SS_D}	*Digital V_{SS}:* This input is the negative supply for the digital portion of the XR-1020A. In order to obtain the low noise operation that is needed in an instrumentation filter, this input must be decoupled with a 10µF tantalum, in parallel with a 0.68µF ceramic capacitor.
5	S1	*Digital Input S1:* Selection of the 825Hz or 1010Hz filter is done with this input. When this input is latched high, the 825Hz notch for CCITT standard measurements is selected. When this input is latched low, the 1010Hz notch filter for Bell standard measurements is selected. This assumes that S0 is latched high.
6	S0	When high, the notch filter is selected. When a logic low is latched on this pin, the notch filter is in the power down mode. S1 input is in a "don't care" situation when S0 is latched low.
7	V_{DD_D}	*Digital V_{DD}:* This input is the positive supply for the digital portion of the XR-1020A. Proper decoupling of this pin is required for low noise operation of this instrumentation filter. Decoupling with a 10µF tantalum capacitor, in parallel with a 0.68µF ceramic capacitor is required.
8	NOTCH IN	*Notch filter input:* This is the input to the notch filter. The location of the notch (1010Hz or 825Hz) is set with the address bus as outlined in Figure 1. Since this is an analog input, it is best to keep this signal as far as possible from any digital inputs. Shielding is recommended in most applications to prevent any clock coupling from occurring. The input impedance at this pin is 1MΩ.
9	AGND	*Analog ground:* This pin is the analog reference for the XR-1020A. In order to obtain the low noise operation possible with the XR-1020A, it is very important to have a very low noise ground available. For split supply operation, the AGND pin should have its own separate trace from the supply connector on the edge of the system board-to here. To prevent any inductive components, this trace should be as wide as possible, or as short as possible. An ideal case would be to have the analog ground also act as ground plane or shield for pins 8 through 18. The shield should be kept away from the digital inputs and clocks.
10	NOTCHOUT	*Notch filter output:* This is the output of the 1010 or 825Hz notch filter. It is designed to drive a typical 10kΩ load. For distortion analysis, it is necessary to keep this signal from any clocks or other signals that may couple to this trace and cause an error in measurements. Note that the notch filter input (Pin 8) is separated from the output by analog ground for this reason. To combine the notch output with other portions of the system, the SD5000 quad NMOS field-effect transistors or the 74HC4053 is recommended, due to the low on resistance and the small cross coupling.

5

11 FILTEROUT *Filter output:* This is the output of the output multiplexer and continous-time smoothing filter. The filter shape available at this point is controlled by the address lines S0 through S7. The C-message weighting, Program weighting, psophometric, 3 or 15kHz low pass, 50 KBPS low pass, and peak-to-average filters can be obtained at this pin.

This output should be kept away from other clocks in the system to avoid coupling of this signal to the signal present at this pin.

As with the notch filter output, this output is designed to typically drive a 10kΩ load.

12 V_{SS_A} *Analog V_{SS}:* This is the negative supply for the analog portions of the XR-1020A. It must be a low noise, low impedance supply to obtain satisfactory performance from the XR-1020A and avoid any degradation in the operation of the filters.

With split supply operation, this pin is tied to –5 VDC ± 5%. It must be decoupled with a 0.68µF ceramic capacitor to analog ground. In parallel with the ceramic capacitor, a 10µF tantalum capacitor must be used. This will prevent any noise on the supply lines from being coupled to the signals to be filtered. These two caps must be located as close as possible to Pin 12 of the device. If possible, the best arrangement is obtained when a separate V_{SS} regulator is used. The LM79L05AC could be used in such a case. The output of the regulator should be tied only to V_{SS_A}, Pin 12 of the XR-1020A.

13 V_{DD_A} *Analog V_{DD}:* This is the positive analog supply and must be decoupled to analog ground with a 10µF tantalum capacitor as well as a 0.68µF ceramic capacitor. These capacitors should be as physically close to Pin 13 of the package as possible.

This analog V_{DD} should be separated from the digital V_{DD} throughout the system connecting only at the supply connector of the system This pin is set to +5 VDC (±5%).

Note that in both single and split supply operation, decoupling is needed. In single supply operation, this pin should be tied to +10 VDC (±5%).

For optimum performance, a regulator such as the XR-4194 with the above decoupling should be used. This regulated should only be used with the XR-1020 V_{DD_A}. An LM78L-05AC could be used as well. This prevents any noise present on the system V_{DD} from affecting the measurements made with the XR-1020A.

14 HP IN *50 KBPS input:* This, in most applications, is tied to the output of the external 50Hz high-pass filter. Note that this input is tied internally to the output multiplexer so that no external selector needs to be used in most applications.

The entire 50 Hz continuous time high-pass filter as well as the input and output of the 50 KBPS filter should be kept away from the rest of the system's clocks, to prevent degradation of the measurements made.

15 1kHz OUT *1kHz band-pass filter output:* This output is provided separate from the other filters for tests requiring phase jitter measurements at the same time as other measurements.

A continuous time smoothing filter is provided to eliminate the need of an external filter.

Note that there are some address selections that can keep the 1kHz (phase jitter) filter in the power down mode and provide no output. Refer to Figure 1 for details.

As with other outputs, this pin can typically drive a 10kΩ load.

16 HP OUT

50 KBPS filter output: This output is used to add the external 50Hz high-pass filter to the 50 KBPS low-pass filter shape.

Note that no output will appear at this pin if the 50 KBPS is not selected using the address bus. Refer to Figure 1 for more information.

The output is designed to drive a 10kΩ load. This should be considered when the external circuit is designed.

17 1kHz IN

1kHz band-pass filter input: This input provides access to the phase jitter band-pass filter input. It is separated from the other filter functions in order to allow for flexibility in measurements.

As with the other filter inputs, this input should be kept away from any system clocks that may add noise to the inputs. A ground plane or trace surrounding this and other filter input pins will be helpful.

The input impedance at this pin is 1MΩ.

18 FILTER IN

Filter multiplexer input: This input provides access to the eight filter functions, as described in Figure 1.

The input impedance at this pin is 1MΩ.

19 XTAL IN

Crystal input: This is used with the XTAL OUT to create a 3.579545MHz oscillator. A parallel ressonant crystal should be used to obtain the ±0.01% accuracy to prevent clock inaccuracy from affecting the position of the filter shape. If not used, it must be tied to either $V_{DD_D} - V_{SS_D}$.

20 XTAL OUT

Crystal output: This input is used with the Pin 19 crystal input to obtain the clock. Note that external capacitors are used to accurately get the crystal oscillating frequency as shown in the Typical Application Circuit diagram.

A parallel resonant crystal must be used to obtain the proper oscillatory frequency. If this pin is not used, it should be disconnected.

21 CLK IN

Clock input: At this pin is applied the 3.579545MHz clock from the system if it is desired not to use the on-chip oscillator. If this pin is not used, it should be tied to either V_{DD_D} or V_{SS_D}.

22 DGND

Digital ground: This input provides the reference for the digital portions of the XR-1020A. It should be tied to the digital ground of the system, separate from the analog ground of Pin 9, AGND. The two grounds may connect at the supply.

As with the analog ground, a wide trace is needed to reduce any inductive components in the system.

23 S2

Digital input S2: This is address line 2 and controls the use of the 1kHz band-pass (phase jitter) filter. When latched high, the 1kHz band-pass filter is selected. When this input is latched low, the 1kHz band-pass filter is in the power down mode. Details on its operation are given in Figure 1. With split supply operation, all digital inputs are TTL compatible.

24 S7

Digital input S7: This input, along with the address lines S6 and S5, controls the selection of the eight filters obtained with the on-chip multiplexers. Details are given with the pin description for digital input S5.

5

25 S6

Digital Input S6: This input, with address lines S7 and S5, controls the input and output multiplexers. This is detailed with the pin description for S5, digital input S5 (Pin 27).

26 NC

No internal connection: Due to the closeness to the other digital inputs, it is recommended that this pin be tied to digital ground (DGND), Pin 22.

27 S5

Digitai input S5: This digital input, along with S7 and S6, controls which of eight filter functions will be selected using the on-chip multiplexers.

S7	S6	S5	Function
0	0	0	Peak-to-average filter is selected.
0	0	1	50 KBPS filter is selected.
0	1	0	3kHz low-pass filter is selected.
0	1	1	15kHz low-pass filter is selected.
1	0	0	Wire (direct from input multiplexer to output multiplexer).
1	0	1	Psophometric weighting filter (for CCITT noise measurements).
1	1	0	Program-weighting filter.
1	1	1	C-message weighting filter (for Bell noise measurements).

28 S4

Digital input S4: This digital input, along with S3 (Pin 1), selects which of the three inputs will be applied to the input multiplexer.

S4	S3	Function
0	X	Filter input. Note that when S4 is latched low, S3 is in the "don't care" mode.
1	0	1010 Hz (825 Hz) notch filter is the input selected, Note that if SO is latched low, then no usable signal would be applied to the filter bank since the notch filter would be in the power down mode.
1	1	When this combination is latched into the XR-1020A, the 1kHz band-pass (phase jitter) filter is selected. Note that S2, the 1kHZ band-pass filter enable, must be latched high, or no usable output will appear at the filter output.

Board Layout

The device is divided approximately in half with Pins 1 through 7, and Pins 19 through 28 having digital functions, and the rest having an analog function. It is best to use the XR-1020A at the dividing point between the analog and digital portions of the systems as would be done with an analog-to-digital converter.

An analog ground plane for the filter inputs and outputs is recommended, as long as the trace from the ground plane to the supply ground can be made wide enough to prevent the ground plane from acting as a capacitor or an antenna.

FILTER CHARACTERISTICS

1KHz Band-pass Filter (Phase Jitter), see Figure 6

Parameter	Min.	Typ.	Max.	Unit	Conditions
Output Offset Voltage–0.5	0	+0.5		V	V_{IN} = 0V
Input Frequency					
Less than 100Hz		–35		dB	V_{IN} = 1Vrms
150Hz			–28	dB	
250Hz			–20	dB	
300Hz	–15		–18	dB	
500Hz	–10		–8	dB	
600Hz	–5	–5		dB	
700Hz	–3	–3		dB	
1000Hz	–1	0	+1	dB	
2000Hz		–12		dB	
3000Hz		–20	–18	dB	
Greater than 3500Hz			–25	dB	

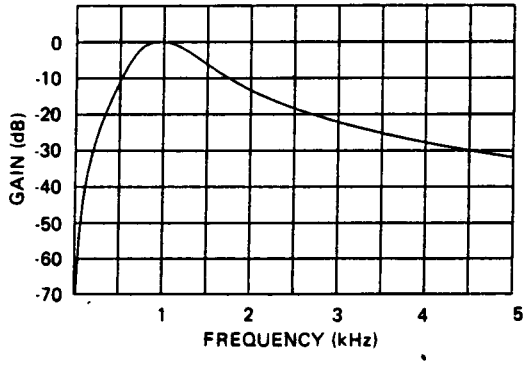


Figure 6. Amplitude Response: 1kHz Band-pass

FILTER CHARACTERISTICS

C-Message Weighting Filter, see Figure 7

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
100Hz		–42.5		dB	V_{IN} = Vrms
200Hz	–27.0	–25.1	–23.0	dB	
300Hz		–16.3		dB	
400Hz	–12.2	–11.2	–10.2	dB	
500Hz		–7.7		dB	
600Hz		–5.0		dB	
700Hz		–2.8		dB	
800Hz		–1.3		dB	
900Hz		–0.3		dB	
1000Hz	–1.0	0.0	+1.0	dB	
1200Hz		–0.4		dB	
1300Hz		–0.7		dB	
1500Hz		–1.2		dB	
1800Hz		–1.3		dB	
2000Hz		–1.1		dB	
2500Hz		–1.1		dB	
2800Hz		–2.0		dB	
3000Hz	–4.0	–3.0	–2.0	dB	
3300Hz		–5.1		dB	
3500Hz	–9.1	–7.1	–5.1	dB	
4000Hz		–14.6		dB	
4500Hz		–22.3		dB	
5000Hz	–31.7	–28.7	–25.7	dB	

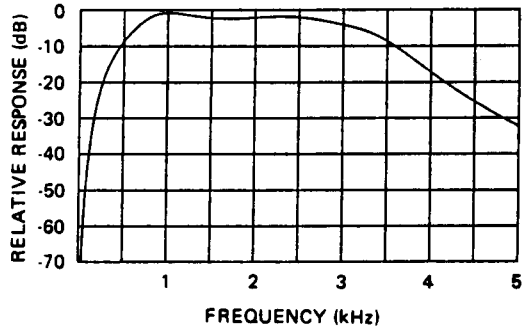


Figure 7. Amplitude Response: C-Message

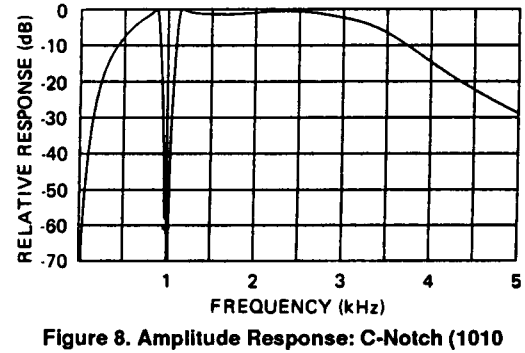


Figure 8. Amplitude Response: C-Notch (1010 Notch with C-Message Weighting Filter)

FILTER CHARACTERISTICS

Psophometric Weighting Filter, see Figure 9.

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
16.66Hz		–85		dB	V_{IN} = Vrms
50Hz		–63.0		dB	
100Hz		–41.0		dB	
200Hz	–23.0	–21.0	–19.0	dB	
300Hz		–10.6		dB	
400Hz	–7.3	–6.3	–5.3	dB	
500Hz		–3.6		dB	
600Hz		–2.0		dB	
700Hz		–0.9		dB	
800Hz	–1.0		+1.0	dB	
900Hz		+0.6		dB	
1000Hz		+1.0		dB	
1200Hz	–1.0	0.0	+1.0	dB	
1400Hz		–0.9		dB	
1600Hz		–1.7		dB	
1800Hz		–2.4		dB	
2000Hz		–3.0		dB	
2500Hz		–4.2		dB	
3000Hz	–6.6	–5.6	-4.6	dB	
3500Hz		–8.5		dB	
4000Hz		–15.0		dB	
4500Hz		–25.0		dB	
5000Hz		–36.0		dB	
6000Hz	–47	–43	–39	dB	

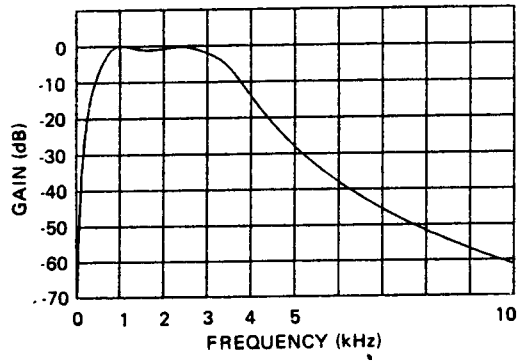


Figure 9. Amplitude Response: Psophometric Filter

FILTER CHARACTERISTICS

3kHz Low-Pass Filter, see Figure 10

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency					
30Hz		0		dB	V_{IN} = Vrms
60Hz		0		dB	
400Hz	–1	0	+1	dB	
1000Hz	–1	0	+1	dB	
2010Hz	–1.8	–0.2	+0.2	dB	
3000Hz	–4.8	–3.0	–1.2	dB	
6000Hz	–15.3	–12.3	–9.3	dB	

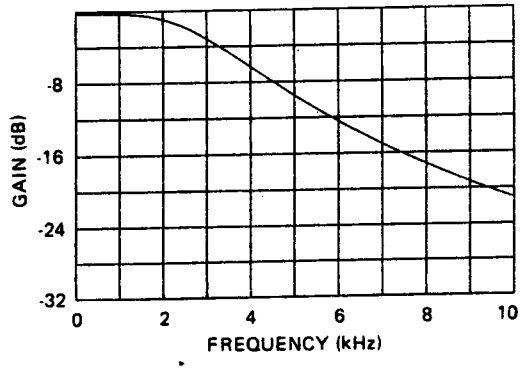


Figure 10. Amplitude Response: 3kHz Low-Pass Filter

FILTER CHARACTERISTICS

825Hz Notch, see Figure 11

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
325Hz	–1.5	0		dB	V_{IN} = Vrms
570Hz	–2.0	0		dB	
690Hz	–4	0		dB	
827Hz		–70	–50	dB	
855Hz		–70	–50	dB	
1000Hz	–4	0		dB	
1105Hz	–2	0		dB	
1360Hz	–1.5	5	0	dB	

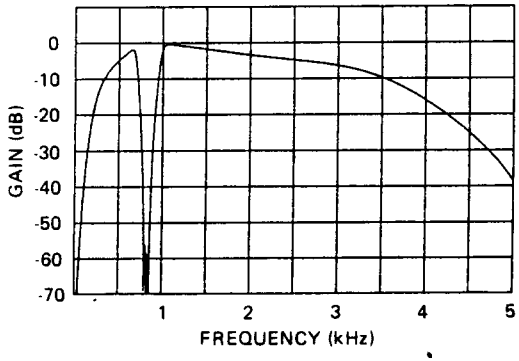


Figure 11. 825Hz Notch and Psophmetric Filter

FILTER CHARACTERISTICS

1010Hz Notch Filter, see Figure 12

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5	0.1	0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
400Hz	–1.5	0		dB	V_{IN} = Vrms
529Hz		0		dB	
700Hz	–2.0	0		dB	
860Hz	–4	–1		dB	
995Hz		–70	–50	dB	
1010Hz		–70	–50	dB	
1025Hz		–70	–50	dB	
1180Hz	–4.0	0		dB	
1330Hz	–2.0	0		dB	
1700Hz	–1.5	0		dB	

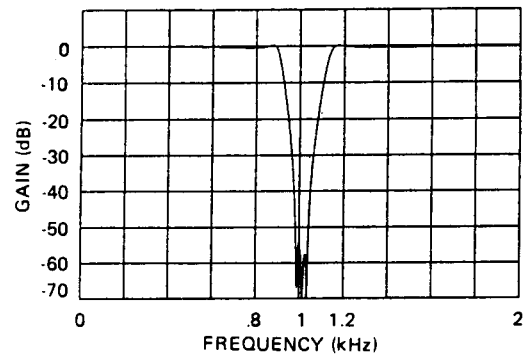


Figure 12. 1010Hz Notch Amplitude Response

FILTER CHARACTERISTICS

50 KBPS Weighting Filter Low-Pass Filter Section, see Figure 13

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output					
Offset Voltage	–0.5		+0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
50Hz		0		dB	V_{IN} = Vrms
200Hz		0		dB	
400Hz	–1	0	+1	dB	
1000Hz	–0.2	0.0	+0.2	dB	
5000Hz		0		dB	
10000Hz	–1.8	–0.1	+0.2	dB	
15000Hz	–4.8	–0.4	–0.2	dB	
20000Hz		–1.0		dB	
25000Hz	–3.1	–1.9	–1.1	dB	
30000Hz	–4.6	–3.1	–1.6	dB	
35000Hz		–4.7		dB	
40000Hz		–7.9		dB	
45000Hz		–14.0		dB	
55000Hz			–29.0	dB	
Greater than 550000Hz			–30.0	dB	

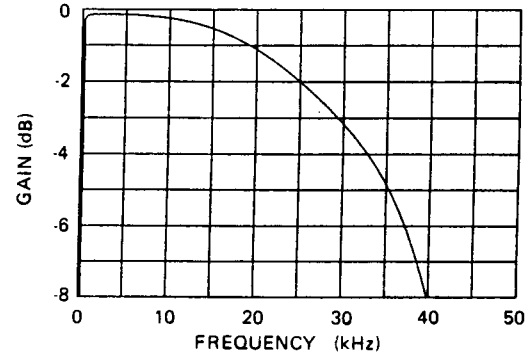


Figure 13. Amplitude Response: 50 kBPS Filter with 50Hz High-pass Filter

FILTER CHARACTERISTICS

Peak-to-Average Ratio (P/AR) Band-pass Filter, see Figure 14

Receiver Response

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency: f_o					
140Hz		–50.5		db	V_{IN} = Vrms
390Hz	–34.5	–31.5	–28.5	dB	
640Hz	–22.4	–20.4	–18.4	dB	
890Hz	–12.63	–10.6	–8.63	dB	
1140Hz		–2.1		dB	
1390Hz	–1.6	–0.6	+0.4	dB	
1640Hz		–5.5		dB	
1890Hz	–12.5	–10.5	–8.5	dB	
2140Hz		–14.5		dB	
2390Hz		–17.7		dB	
2640Hz	–22.4	–20.4	–18.4	dB	
2890Hz		–22.7		dB	
3140Hz		–24.6		dB	
3390Hz		–26.4		dB	
3640Hz		–27.9		dB	
3890Hz	–33.3	–29.3	–26.3	dB	

Receiver Phase

Includes removal of an approximate = cycle (at 56kHz) linear phase error (inherent in sample data devices) which can be subtracted out by normal system linear phase compensation networks.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Input Frequency: f_o					
140Hz		173.77		degree	
390Hz		161.2		degree	
640Hz		143.6		degree	
890Hz		114.0		degree	
1140Hz		55.2		degree	
1390Hz		–31.2		degree	
1640Hz		–87.2		degree	
1890Hz		–114.5		degree	
2140Hz		–129.6		degree	
2390Hz		–138.8		degree	
2640Hz		–145.1		degree	
2890Hz		–149.8		degree	
3140Hz		–153.3		degree	
3390Hz		–156.1		degree	

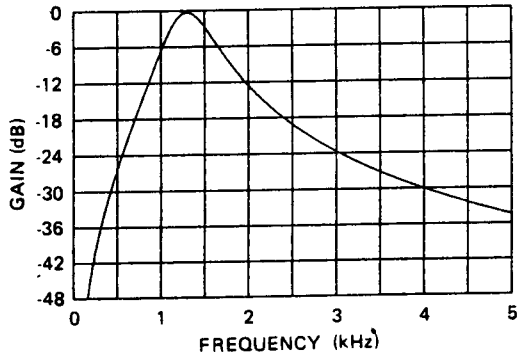


Figure 14. Amplitude Response: Peak-to-Average Ratio Band-pass Filter

FILTER CHARACTERISTICS

Program Weighting Filter, see Figure 15

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output Offset Voltage	–0.5	0.1	+0.5	VDC	V_{IN} = 0V
Input Frequency: f_o					
100 Hz		–26.3		dB	V_{IN} = Vrms
200 Hz	–19.3	–17.3	–15.3	dB	
300 Hz		–12.2		dB	
400 Hz		–9.0		dB	
500 Hz	–8.6	–6.6	–4.6	dB	
600 Hz		–4.7		dB	
700 Hz		–3.2		dB	
800 Hz		–2.0		dB	
900 Hz		–0.8		dB	
1000 Hz	–1.0		+1.0	dB	
1500 Hz	+2.2	+3.2	+4.2	dB	
2000 Hz	+3.5	+4.8	+5.5	dB	
2500 Hz		+5.6		dB	
3000 Hz		+6.0		dB	
4000 Hz		+6.5		dB	
5000 Hz	+3.5	+6.5	+9.5	dB	
6000 Hz		+6.4		dB	
7000 Hz		+5.8		dB	
8000 Hz	0.0	+4.0	+8.0	dB	
9000 Hz		+1.5		dB	
10000 Hz	–12.5	–8.5	–4.5	dB	

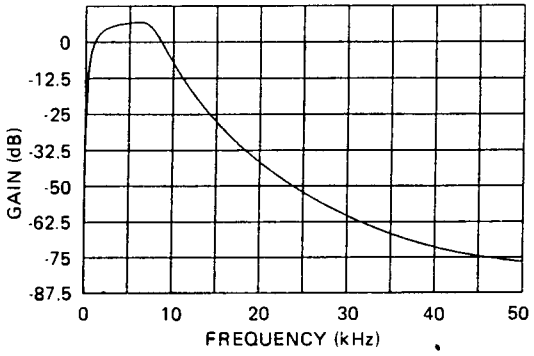


Figure 15. Amplitude Response: Program Weighting Filter

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FILTER CHARACTERISTICS

15kHz Low-Pass Filter, see Figure 16

Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OS} Output Offset Voltage	–0.5	0	+0.5	V	V_{IN} = 0V
Input Frequency: f_o					
30 Hz		0		dB	V_{IN} = Vrms
60 Hz		0		dB	
400 Hz	–1	0	+1	dB	
1000 Hz	–1	0	+1	dB	
10000 Hz	–1.8	-0.8	+0.2	dB	
15000 Hz	–4.8	–3.0	–1.2	dB	
30000 Hz	–15.3	–12.3	–9.3	dB	

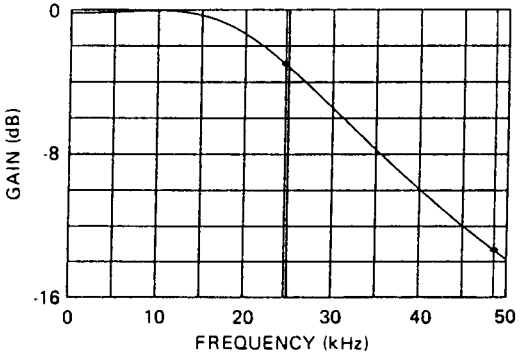

Figure 16. Amplitude Response: 15 kHz Low-pass Filter