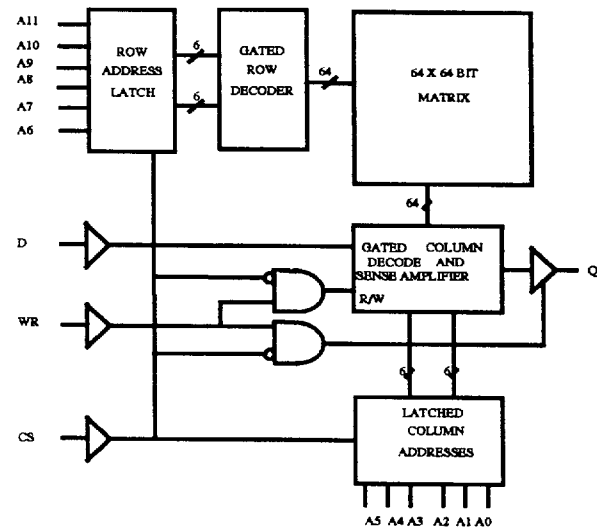


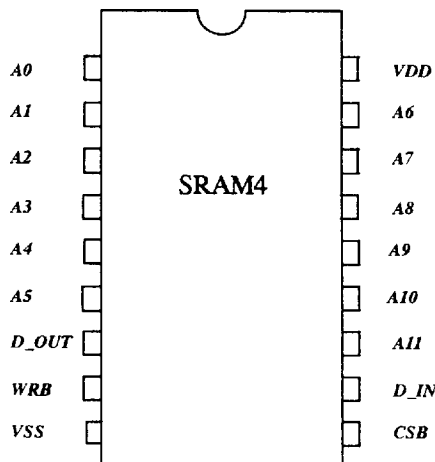
Features

- ▶ 1.2um Radiation Hardened SOI CMOS
Total Dose > 100k RAD (Si)
Transient 3×10^{10} RAD (Si)/s
Survivability > 1×10^{12} RAD (Si)/s
- ▶ Latch-Up Free
- ▶ Low Voltage Backup Mode
- ▶ Low Standby Current
- ▶ Fully Static Design
- ▶ Six Transistor Bit Cell
- ▶ TTL on all Inputs, CMOS Outputs
- ▶ 5 Volt Supply
- ▶ Standard JEDEC DIP Pinout
- ▶ Full Mil Temp (-55 to 125°C)

Functional Diagram



18 Pin Dip



Description

The AlliedSignal SRAM4 is a Radiation Hardened industry standard 4096 x 1 bit static random access memory. It is fabricated using AlliedSignal's proprietary 1.2um CMOS/SOI process which exhibits a high tolerance to radiation and temperature. The RAM operates as specified over full military temperature and requires a single 5 V(+/- 10%) supply and retains data down to 2.0 volts.

TRUTH TABLE

CSB	WRB	MODE	OUTPUT
H	X	NOT SELECTED	HIGH Z
L	L	WRITE	INPUT
L	H	READ	DATA OUT

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow I.C. handling procedures.

Specifications SRAM4

DC ELECTRICAL CHARACTERISTICS						
Test	Symbol	-55°C ≤ T _C ≤ 125°C 4.5 V ≤ V _{DD} ≤ 5.5 V unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Input Voltage Low	V _{IL}		1,2,3	V _{SS} - 0.7	0.8	V
Input Voltage High	V _{IH}		1,2,3	V _{DD} /2	V _{DD} + 0.7	V
Output Voltage Low	V _{OL}	V _{dd} = max, I _{ol} = 0.0 mA	1,2,3		V _{SS} + 0.1	V
Output Current Low	I _{OL}	V _{dd} =min, V _{ol} =0.4	1 2,3		3.5 2.5	ma
Output Voltage High	V _{OH}	V _{dd} = min, I _{ol} = 0.0 mA	1,2,3	V _{DD} - 0.1		V
Output Current High	I _{OH}	V _{dd} =min, V _{oh} =V _{dd} -0.4	1 2,3		-2.5 -2.0	
Input Leakage Current	I _L	V _{dd} = max, V _{in} = HI	1 2,3		+/- 2 +/- 10	ma
High Z State Output	I _{IZ}	V _{dd} = max, V _{in} = GND	1 2,3		+/- 5 +/- 10	ma
Quiescent Current	I _{DD}	CSB=HI, WRB=HI	1 2,3		0.1 1.0	ma
Operating Current	I _{OPRO}	CSB=HI, WRB=HI	1 2,3		0.15 1.0	ma
Operating Current	I _{OPR}	CSB=HI, WRB=HI	1,2,3		5.0	ma
Input Capacitance	C _I	Guaranteed but not tested	4		5	pf
Input Capacitance	C _O	Guaranteed but not tested	4		5	pf

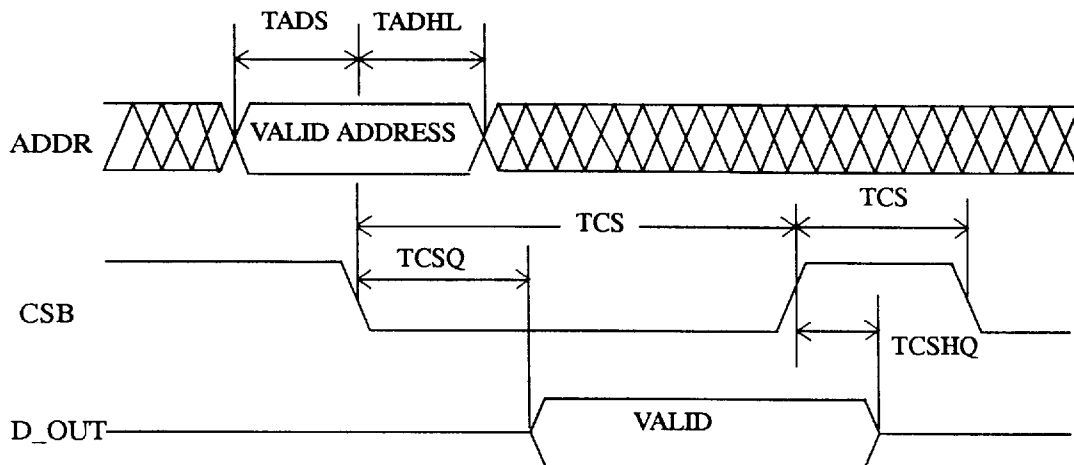
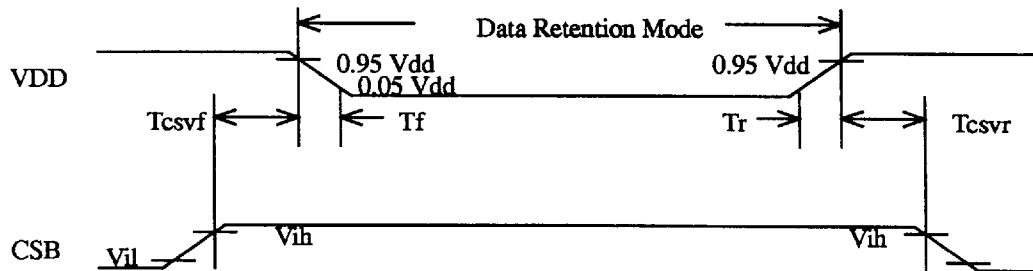
Notes: Notes: /1 Measured using a 1MHz cycle rate with the outputs loaded with 50pf.

AC ELECTRICAL CHARACTERISTICS						
Test	Symbol	-55°C ≤ T _C ≤ 125°C 4.5 V ≤ V _{DD} ≤ 5.5 V unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Read Access	TCSQV	Figure 1	9		70	ns
			10,11		80	
CS High to Q Hi Z	TCSHQZ	Figure 1	9		20	ns
			10,11		30	
CS High	TCSH	Figure 1	9	30		ns
			10,11	40		
Address Setup	TADSU	Figure 1.2	9	10		ns
			10,11	15		
CS Low	TCSL	Figure 2	9	85		ns
			10,11	95		
Address Hold	TADHLD	Figure 1.2	9	10		ns
			10,11	15		
Write Low to CS High	TWRLCSH	Figure 2	9	60		ns
			10,11	70		
Write Low	TWRM	Figure 2	9	60		ns
			10,11	70		
Data Setup	TDSU	Figure 2	9	50		ns
			10,11	60		
Data Hold From Write High	TDHLD	Figure 2	9	10		ns
			10,11	15		

Specifications SRAM4

CHARACTERISTICS (DATA RETENTION)

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{DD} ≤ 5.5 V unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Minimum data Retention Voltage	VDR		9		2.0	V
			10,11		2.5	
Data retention Quiescent Current	I _{DDDR}		9		40	µA
			10,11		70	
CSB to VDD Rise and Fall Time	T _{Tr} , T _F T _{CSVF} , T _{CSVR}		-55°C < T _A < +125°C	9,10,11	1	ns

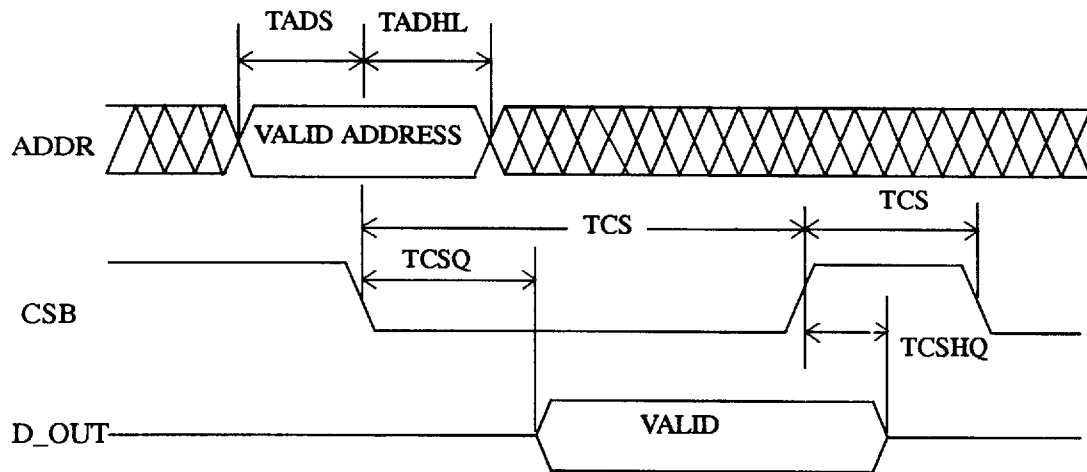


READ CYCLE

FIGURE 1

NOTE: ALL "AC" INPUT PARAMETERS MEASURED WITH RESPECT TO VDD/2.

Specifications SRAM4



READ CYCLE

FIGURE 2

NOTE: ALL "AC" INPUT PARAMETERS MEASURED WITH RESPECT TO VDD/2.