

SRM20100L_{70/85/10}

CMOS 1M-BIT STATIC RAM

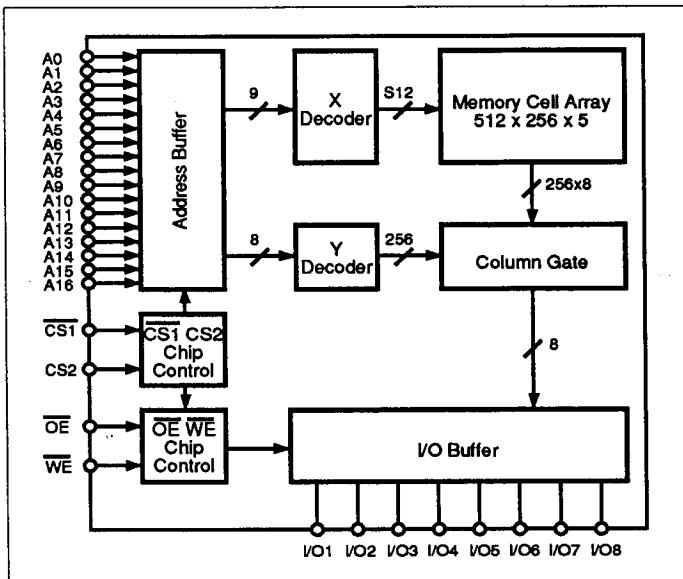
DESCRIPTION

The SRM20100L_{70/85/10} is a 131,072 words x 8 bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the three-state output allows easy expansion of memory capacity.

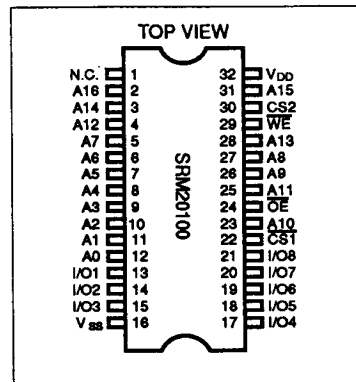
FEATURES

- Fast access time SRM20100L₇₀ 70ns (Max)*
SRM20100L₈₅ 85ns (Max)
SRM20100L₁₀ 100ns (Max)
- Low supply current Standby : 2μA (Typ)
Operation: 15mA (Typ)
- Completely static No clock required
- Single power supply 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capacity
- Non-volatile storage with battery back-up operation
- Package SRM20100LC_{70/85/10} 32-pin DIP (plastic)
SRM20100LM_{70/85/10} 32-pin SOP (plastic)
SRM20100LTM_{70/85/10} 32-pin TSOP (plastic)
SRM20100LRM_{70/85/10} 32-pin TSOPR (plastic)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

A0 to A16	Address Input
WE	Write Enable
OE	Output Enable
CS1	Chip Select 1
CS2	Chip Select 2
I/O1 to 8	Data Input/Output
VDD	Power Supply (+5V)
Vss	Power Supply (0V)
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage*	V _I	-0.5 to 7.0	V
I/O voltage*	V _{IO}	-0.5 to V _{DD} +0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s (at lead)	—

* V_I, V_{IO} (Min) = -3.0V (Pulse width is to 50 ns)

DC RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	—	4.5	5.0	5.5	V
	V _{SS}	—	0	0	0	V
Input Voltage	V _{IH}	—	2.2	3.5	V _{DD} + 0.3	V
	V _{IL}	—	-0.3*	0	0.8	V

* If pulse width is less than 50ns, it is -3.0V

ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20100L70/85/10			Unit
			Min	Typ*1	Max	
Input leakage current	I _{IL}	V _I = 0 to V _{DD}	-1	—	1	μA
Standby supply current	I _{DD}	CS1 = V _{IH} or CS2 = V _{IL}	—	1	3.0	mA
	I _{DD} 1	CS1 = CS2 ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V	—	2	100	μA
Average operating current	I _{DDA}	V _I = V _{IL} , V _{IH} I _{IO} = 0mA, t _{cyc} = Min	—	45	70	mA
Operating supply current	I _{DDO}	V _I = V _{IL} , V _{IH} I _{IO} = 0mA	—	15	35	mA
Output leakage	I _{LO}	CS1 = V _{IH} or CS2 = V _{IL} or WE = V _{IL} or OE = V _{IH} V _{IO} = 0 to V _{DD}	-1	—	1	μA
High level output voltage	V _{OH}	I _{OH} = -1.0 mA	2.4	V _{DD} -0.1	—	V
Low level output voltage	V _{OL}	I _{OL} = 2.1 mA	—	0.2	0.4	V

*1 Typical values are measured at T_a = 25°C and V_{DD} = 5.0V.

Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C _{ADD}	V _{ADD} = 0V	—	—	10	pF
Input capacitance	C _I	V _I = 0V	—	—	10	pF
I/O capacitance	C _{IO}	V _{IO} = 0V	—	—	10	pF

● AC ELECTRICAL CHARACTERISTIC ○ Read Cycle ($V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to $70^\circ C$)

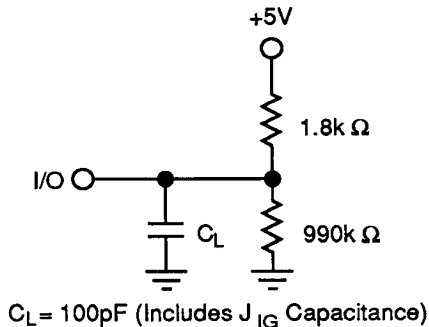
Parameter	Symbol	Conditions	SRM20100L70		SRM20100L85		SRM20100L10		Unit
			Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	70	—	85	—	100	—	ns
Address access time	t_{ACC}		—	70	—	85	—	100	ns
$\overline{CS1}$ access time	t_{ACS1}		—	70	—	85	—	100	ns
$CS2$ access time	t_{ACS2}		—	70	—	85	—	100	ns
OE access time	t_{OE}		—	40	—	45	—	50	ns
$\overline{CS1}$ output set time	t_{CLZ1}	*2	10	—	10	—	10	—	ns
$\overline{CS1}$ output floating	t_{CHZ1}		—	30	—	30	—	35	ns
$CS2$ output set time	t_{CLZ2}		10	—	10	—	10	—	ns
$CS2$ output floating	t_{CHZ2}		—	30	—	30	—	35	ns
OE output set time	t_{OLZ}		5	—	5	—	5	—	ns
OE output floating	t_{OHZ}		—	30	—	30	—	35	ns
Output hold time	t_{OH}	*1	10	—	10	—	10	—	ns

○ Write Cycle ($V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to $70^\circ C$)

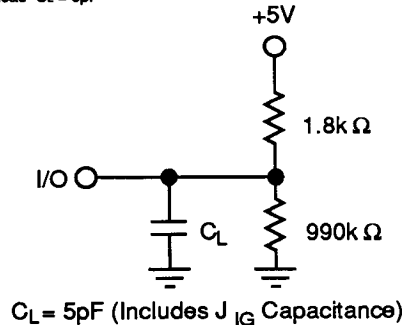
Parameter	Symbol	Conditions	SRM20100L70		SRM20100L85		SRM20100L10		Unit
			Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	70	—	85	—	100	—	ns
$CS1$ time	t_{CW1}		60	—	70	—	80	—	ns
$CS2$ time	t_{CW2}		60	—	70	—	80	—	ns
Address enable time	t_{AW}		60	—	70	—	80	—	ns
Address setup time	t_{AS}		0	—	0	—	0	—	ns
Write pulse width	t_{WP}		55	—	65	—	75	—	ns
Address hold time	t_{WR}		0	—	0	—	0	—	ns
Input data setup time	t_{DW}		30	—	35	—	40	—	ns
Input data hold time	t_{DH}		0	—	0	—	0	—	ns
$\overline{WE}$ output floating	t_{WHZ}	*2	—	30	—	30	—	35	ns
$\overline{WE}$ output setup time	t_{OW}		5	—	5	—	5	—	ns

***1 Test Conditions.**

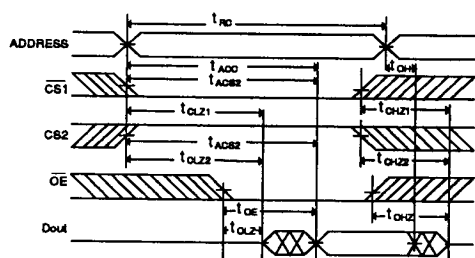
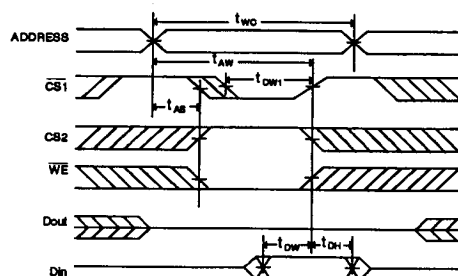
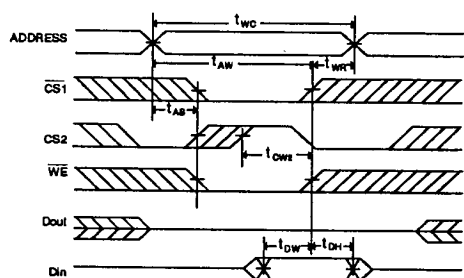
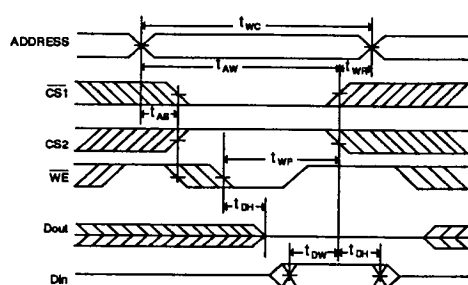
1. Input pulse level : 0.6V to 2.40V
2. $t_r = t_f = 5ns$
3. Input and output timing reference levels : 1.5V
4. Output load $C_L = 100pF$


***2 Test Conditions**

1. Input pulse level : 0.6V to 2.4V
2. $t_r = t_f = 5ns$
3. Input and output timing reference levels : 1.5V
4. Output timing reference levels: $\pm 200mV$
(the level displaced from stable output voltage level)
5. Output load $C_L = 5pF$



Read Cycle

Write Cycle (1) ($\overline{CS1}$ Control)Write Cycle (2) ($\overline{CS2}$ Control)Write Cycle (3) ($\overline{WE}$ Control)

Note:

1. During read cycle time, $\overline{WE}$ is to be "H" level.
2. During write cycle time that is controlled by $\overline{CS1}$ or $\overline{CS2}$, Output Buffer is in high impedance state, whether $\overline{OE}$ is "H" or "L".
3. During write cycle time that is controlled by $\overline{WE}$, Output Buffer is in high impedance state if $\overline{OE}$ is "H" level.

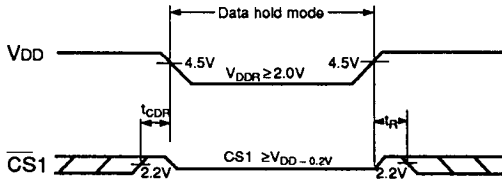
DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(Ta = 0 to 70°C)

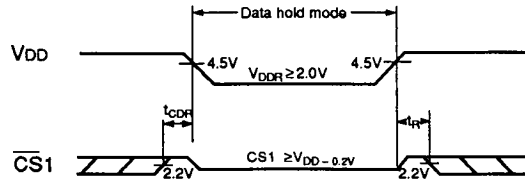
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V _{DDR}		2.0	—	5.5	V
Data retention current	I _{DDR}		—	1	50	μA
Chip select data hold time	t _{CDR}	V _{DO} = 3V CS1=CS2>V _{DO} -0.2V or CS2<0.2V	0	—	—	ns
Operation recovery time	t _R		t _{RC} *	—	—	ns

* t_{RC} = Read Cycle time

Data Retention Timing (CS1 Control)



Data Retention Timing (CS2 Control)



FUNCTIONS

Truth Table

CS1	CS2	OE	WE	DATA I/O	Mode	I _{DD}
H	X	—	—	Hi-Z	Unselected	I _{DDs} , I _{DDs1}
—	L	—	—	Hi-Z	Unselected	I _{DDs} , I _{DDs1}
L	H	X	L	Input data	Write	I _{DDO}
L	H	L	H	Output data	Read	I _{DDO}
L	H	H	H	Hi-Z	Output disable	I _{DDO}

Read Mode

Data is read by setting addresses while holding CS1 = "L", CS2 = "H", OE = "L" and WE = "H". Since data I/O terminals are in a high impedance state when OE = "H", the data bus line can be used for any other objective, then access time is able to be cut down.

Write Mode

There are 4 ways of writing data into the memory:

1. Hold CS2 = "H", WE = "L", set addresses and give "L" pulse to CS1.
2. Hold CS1 = "L", WE = "L", set addresses and give "H" pulse to CS2.
3. Hold CS1 = "L", CS2 = "H", set addresses and give "L" pulse to WE.
4. After setting addresses, give "L" pulse CS1, WE and give "H" pulse to CS2.

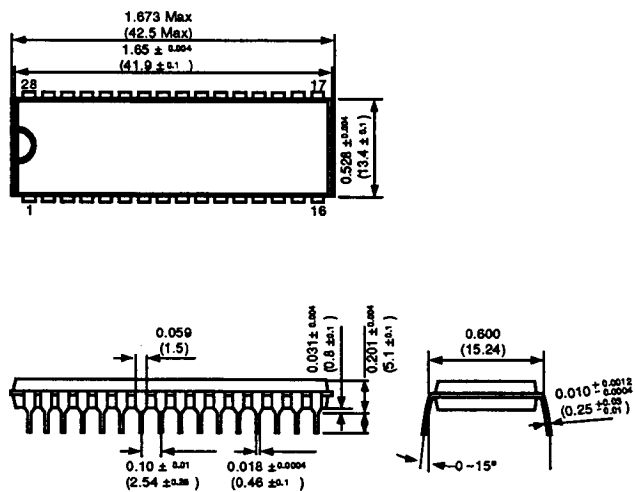
Data on the DATA I/O terminals are latched up into the SRM20100L70/85/10 at the end of the period that CS1, WE are "L", and CS2 is "H" level. As Data I/O terminals are in high impedance state when any of CS1, OE = "H", or CS2 = "L", the contention on the data bus can be avoided.

Standby Mode

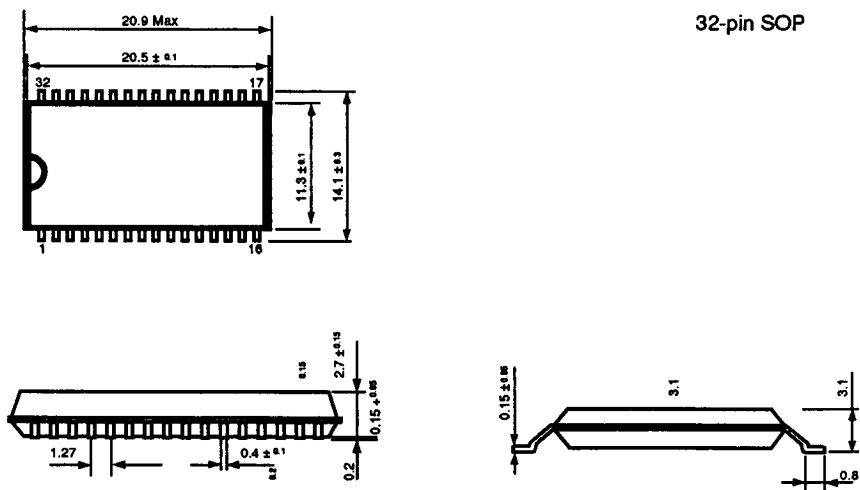
When CS1 is "H" or CS2 is "L" level, the SRM20100L70/85/10 is in the standby mode which has retaining data operation. In this case Data I/O terminals are Hi = -Z, and all inputs of addresses, WE and data can be any "H" or "L". When CS1 and CS2 level are in the range over V_{DD} - 0.2V, or CS2 level is in the range under 0.2V, in the SRM20100L70/85/10 there is almost no current flow except through the high resistance parts of the memory.

C32

32-pin DIP

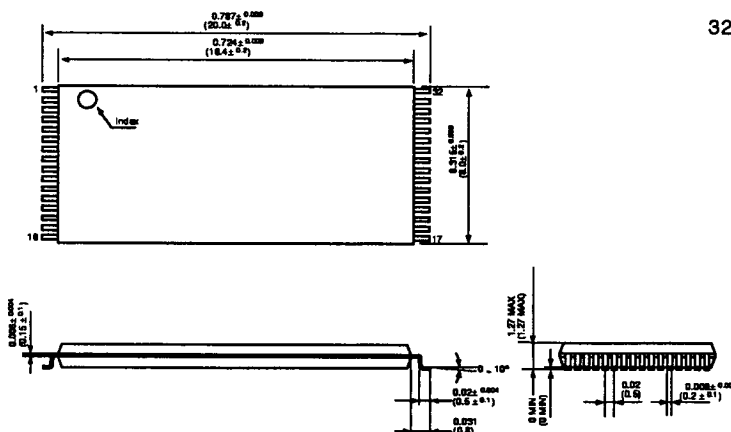
**M32**

32-pin SOP



TM32

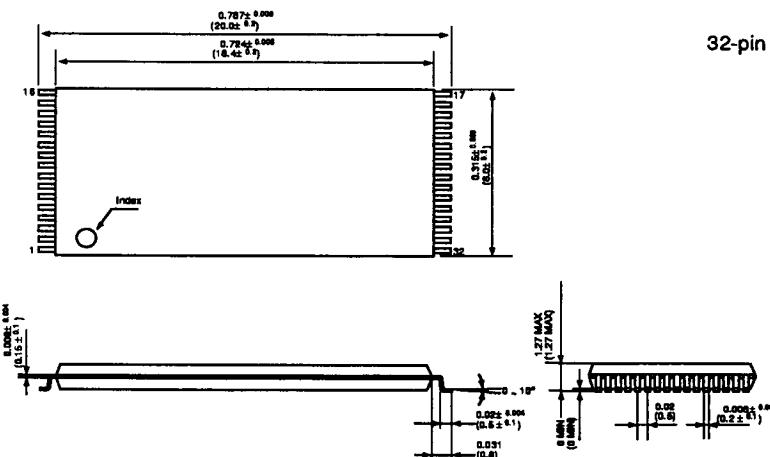
32-pin TSOP*1



*1 SRM20100LTM70/85/100 has the same characteristics as SRM20100LC70/85/10.

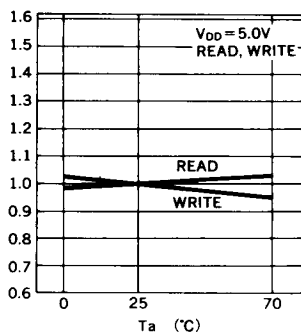
RM32

32-pin TSOPR

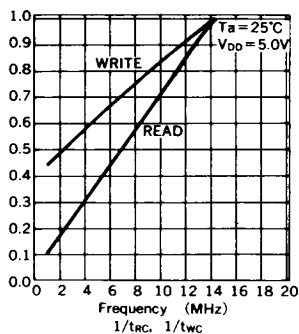


CHARACTERISTICS CURVES

Normalized I_{DDA} — T_a



Normalized I_{DDA} —Frequency



Normalized I_{DDA} — V_{DD}

