CMOS 16K-BIT STATIC RAM

DESCRIPTION

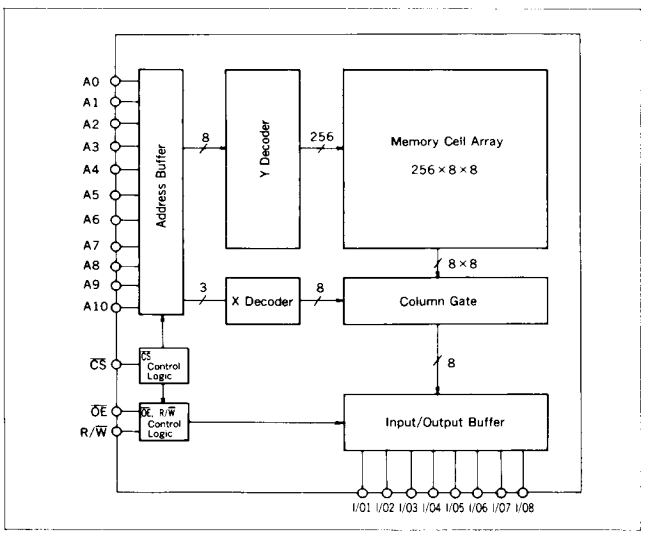
The SRM2016$_{10/12}$ is a 2,048 words x 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the three-state output allows easy expansion of memory capacity.

FEATURES

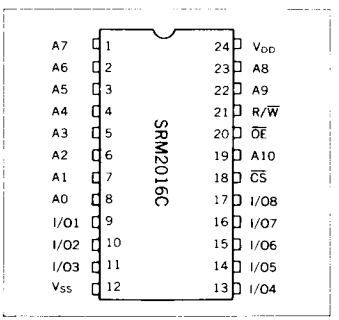
- Access time ..... SRM2016$_{10}$ 100ns (Max)
  SRM2016$_{12}$ 120ns (Max)
- Low supply current .... Standby : 1μA (Typ)
  Operation: SRM2016$_{10}$ 30mA (Typ)
  SRM2016$_{12}$ 25mA (Typ)

- Completely static operation
- Single power supply .. 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package ..... SRM2016C$_{10/12}$ 24-pin DIP(plastic)
  SRM2016M$_{10/12}$ 24-pin SOP (plastic)
  SRM2016N$_{10/12}$ 24-pin Skinny DIP (plastic)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

A0 to A10	Address Input
R/$\overline{W}$	Read/Write
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply (+ 5V)
V_{SS}	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage*	V_I	−0.5 to 7.0	V
Input/output voltage*	$V_{I/O}$	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temp. & time	T_{sol}	260°C, 10s (at lead)	—

*V_I, $V_{I/O}$ = −1.0V when pulse width is 50 ns

■RECOMMENDED OPERATING CONDITIONS

(Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	3.5	V_{DD}+0.3	V
	V_{IL}		−0.3*	—	0.8	V

*V_{IL}(Min)= −1.0V when pulse width is 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM2016$_{10}$			SRM2016$_{12}$			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I_{LI}	V_{DD}=5.5V, V_I=0 to V_{DD}	−1	—	1	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{DD}	−1	—	1	−1	—	1	μA
Operating supply current	I_{DDO}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	30	60	—	25	50	mA
	I_{DDO1}	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	16	—	—	16	—	mA
Average operating current	I_{DDA}	Min. cycle, duty=100%, $I_{I/O}$=0mA	—	30	60	—	25	50	mA
Standby supply current	I_{DDS}	$\overline{CS}$=V_{IH}	—	1.5	3.0	—	1.5	3.0	mA
	I_{DDS1}	$\overline{CS}$=V_{DD}−0.2V	—	1	50	—	1	50	μA
Output voltage	V_{OL}	I_{OL}=4.0mA	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* Typical values are for reference, with V_{DD}=5V and Ta=25°C assumed

●Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	V_I=0V	—	4	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	6	8	pF

●AC Electrical Characteristics

○Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM2016$_{10}$		SRM2016$_{12}$		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CS}$ access time	t_{ACS}		—	100	—	120	ns
$\overline{CS}$ output setup time	t_{CLZ}	*2	10	—	10	—	ns
$\overline{OE}$ access time	t_{OE}	*1	—	55	—	60	ns
$\overline{OE}$ output setup time	t_{OLZ}	*2	5	—	10	—	ns
$\overline{CS}$ output floating	t_{CHZ}		0	40	0	40	ns
$\overline{OE}$ output floating	t_{OHZ}		0	40	0	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

○ **Write Cycle**

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

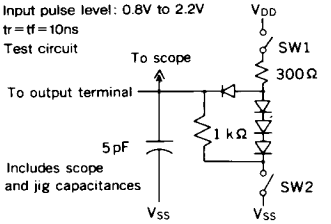
Parameter	Symbol	Conditions	SRM2016-10		SRM2016-12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time ($\overline{CS}$)	t_{CW}		80	—	85	—	ns
Address enable time	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		65	—	70	—	ns
$\overline{OE}$ output floating	t_{OHZ}	*2	0	40	0	40	ns
R/$\overline{W}$ output floating	t_{WHZ}	*3	0	45	0	50	ns
Input data setup time	t_{DW}	*1	45	—	50	—	ns
Address hold time	t_{WR}		5	—	5	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
R/$\overline{W}$ output setup time	t_{OW}	*3	5	—	10	—	ns

*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Input/output timing reference level: 1.5V
4. Output load: I_{TTL} + C_L = 100pF

*2 Test conditions.

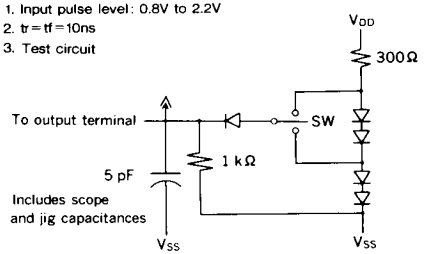
1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Test circuit



○ Both SW1 and SW2 are closed when measuring t_{OHZ} or t_{OHZ}.
○ SW1 is open and SW2 is closed when measuring Hi-z-high of t_{OLZ} or t_{OLZ}.
○ SW1 is closed and SW2 is open when measuring Hi-z-low of t_{OLZ} or t_{OLZ}.

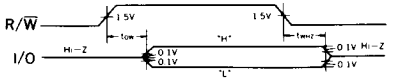
*3 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Test circuit

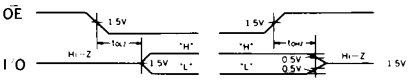


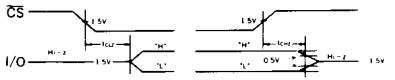
○ SW is set to the V_{DD} side when measuring Hi-z-high and high-Hi-z of t_{OW} or t_{WHZ}.
○ SW is set to the V_{SS} side when measuring Hi-z-low and low-Hi-z of t_{OW} or t_{WHZ}.

Output turn-on turn-off times



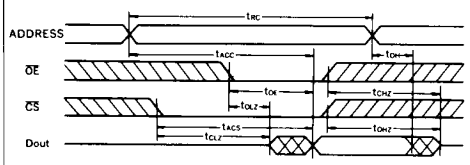
Output turn-on turn-off times



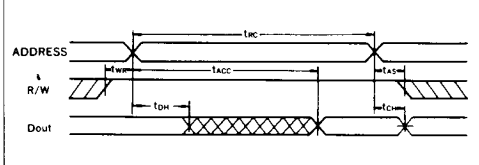


● Timing Chart

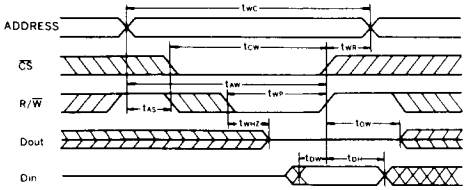
○ Read cycle 1 ($\overline{OE}$, $\overline{CS}$ control, R/$\overline{W}$ = high)



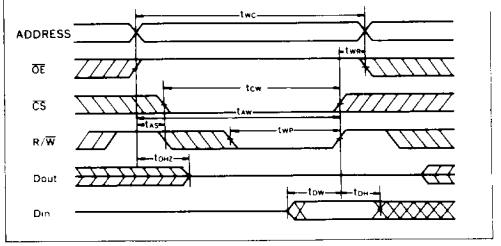
○ Read cycle 2 (R/$\overline{W}$ control, $\overline{OE}$ = low, $\overline{CS}$ = low)



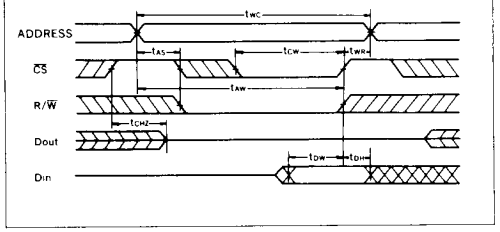
○Write cycle 1 (R/$\overline{W}$ control, OE=low)



○Write cycle 2 (R/$\overline{W}$ control)



○Write cycle 3 (CS control, OE=low)



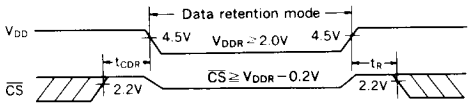
■DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

(Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{CS} \geq V_{DDR} - 0.2V$	2.0	–	5.5	V
Data retention current	I_{DDR}	V_{DD}=3.0V, $\overline{CS} \geq 2.8V$	–	–	25	μA
Chip select data hold time	t_{CDR}	Refer to the figure below.	0	–	–	ns
Operation recovery time	t_R		t_{RC}*	–	–	ns

* t_{RC} : read cycle time

Data retention timing



Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

■FUNCTIONS

●Truth Table

$\overline{CS}$	$\overline{OE}$	R/$\overline{W}$	A0 to A10	DATA I/O	Mode	I_{DD}
H	–	–	–	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	L	H	Stable	Output data	Read	I_{DDO}
L	H	L	Stable	Input data	Write	I_{DDO}
L	L	L	Stable	Input data	Write	I_{DDO}

X : "H" or "L" –: "H", "L" or "Hi

●Reading Data

Data can be read out if an address is set while $\overline{CS}$ and $\overline{OE}$ are held low, and R/$\overline{W}$ is held high.

● **Writing Data**

There are the following three ways of writing data into the memory.

(1) Hold $\overline{CS}$ low, set the address, and apply a low pulse to R/$\overline{W}$.

(2) Hold R/$\overline{W}$ low, set the address, and apply a low pulse to $\overline{CS}$.

(3) Set the address, then apply low pulses to both $\overline{CS}$ and R/$\overline{W}$.

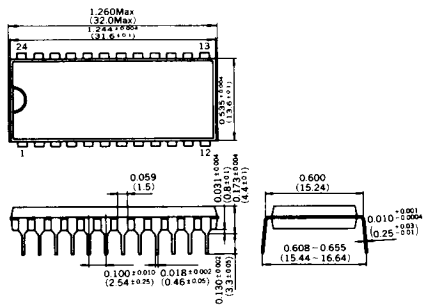
In each case, data from the DATA I/O terminal is fetched into the SRM2016$_{10/12}$ at the last transition of a section in which both $\overline{CS}$ and R/$\overline{W}$ are low. Because the DATA I/O terminal is in high-impedance state when $\overline{CS}$ or $\overline{OE}$ is high, or R/$\overline{W}$ is low, contention of the data driver on the bus and memory output is avoided.

● **Standby Mode**

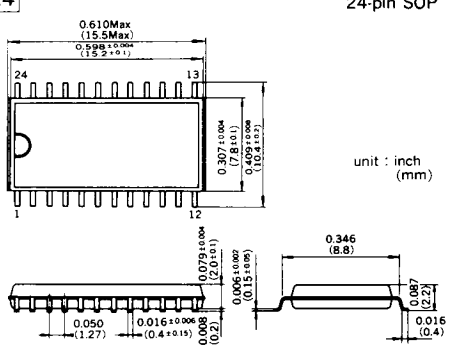
When $\overline{CS}$ is high, SRM2016$_{10/12}$ is in the stand-by mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state, and input of an address, R/$\overline{W}$ signal, or data is prohibited. When $\overline{CS}$ is above V_{DD}—0.2V, current flowing within the SRM2016$_{10/12}$ chip is only that in the high-resistance portion of the memory cells and leakage current.

■**PACKAGE DIMENSIONS**

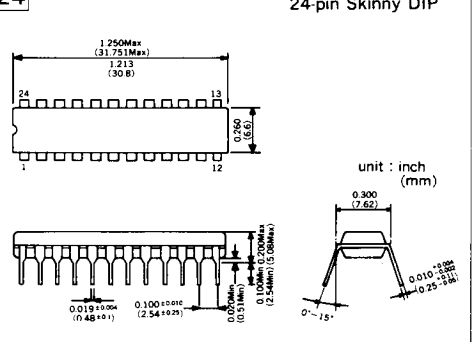
C24 — 24-pin DIP



M24 *1 — 24-pin SOP



N24 *2 — 24-pin Skinny DIP



* 1 Represents model SRM2016M$_{10/12}$ that has the same electrical characteristics as model SRM2016C$_{10/12}$.

* 2 Represents model SRM2016N$_{10/12}$ that has the same electrical characteristics as model SRM2016C$_{10/12}$.

■CHARACTERISTICS CURVES