SRM2114$_{25}$

CMOS 4K-BIT STATIC RAM

■DESCRIPTION

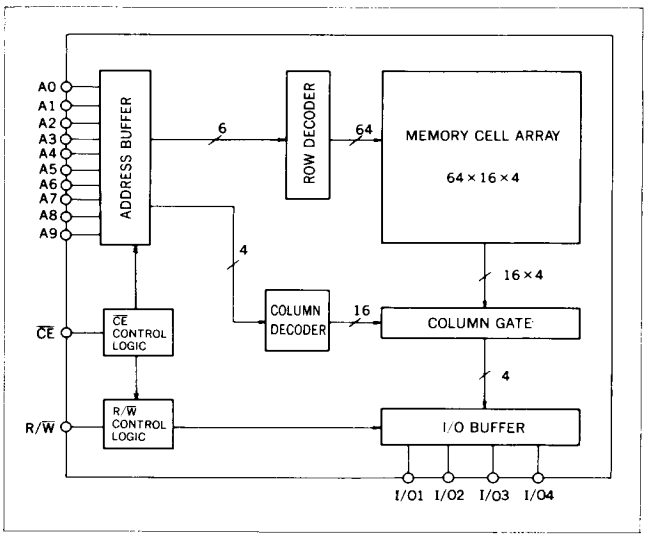
The SRM2114$_{25}$ is a 1,024 words x 4 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby current consumption makes it ideal for applications requiring non-volatile storage with back-up batteries. The static nature of the memory requires no external clock or refreshing circuit.

Both the input and output ports are TTL compatible; and the three-state output allows easy expansion of memory capacity. These features make the SRM2114$_{25}$ usable for a wide range of applications from microprocessor systems to terminal devices.

■FEATURES

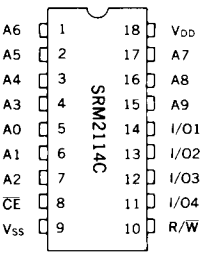
- Access time ..... 250ns (Max)
- Single power supply .. 5V±10%/3 to 5V
- Low supply current .... Standby : 0.1μA (Typ)/0.1μA (Typ)
  Operation: 14mA(Typ)/9mA (Typ)
- Completely static operation
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Operation with back-up batteries
- Package ..... 18-pin DIP(plastic)
  24-pin SOP (plastic)

■BLOCK DIAGRAM

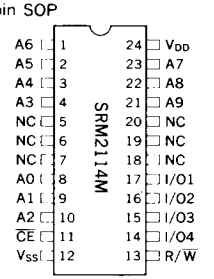


■PIN CONFIGURATION

● 18-pin DIP



● 24-pin SOP



NC : no connection

■PIN DESCRIPTION

A0 to A9	Address Input
R/W	Read/Write
CE	Chip Enable
I/O1 to 4	Data Input/Output
V_{DD}	Power Supply (+)
V_{SS}	Power Supply (−)

■ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage	V_I	-0.5 to 7.0	V
I/O voltage	$V_{I/O}$	-0.5 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	-40 to 85	°C
Storage temperature	T_{stg}	-65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	SRM2114 25			Unit
		Min	Typ	Max	
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
	V_{SS}	—	0	—	
Input Voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	-0.3	—	0.8	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($SRM2114_{25}$ . . . . V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = -40 to 85°C)

Parameter	Symbol	SRM2114 25				Unit
		Conditions	Min	Typ	Max	
Input leakage current	I_{LI}	V_I = 0 to V_{DD}	-1.0	—	1.0	μA
Standby supply current	I_{DDS}	$\overline{CE}$ = V_{DD} - 0.2V	—	0.1	5	μA
Operating supply current	I_{DDO}	$\overline{CE}$ = V_{IL} *C_L = 100pF	—	*14	*35	mA
Output leakage current	I_{LO}	V_O = 0 to V_{DD}	- 1.0	—	1.0	μA
High level output voltage	V_{OH}	I_{OH} = - 1.0mA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 2.0 mA	—	—	0.4	V

*C_L = 0pF Typ7 Max 25

● Terminal Capacitance

(f = 1MHz, $SRM2114_{25}$ . . . . V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = -40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	V_I = 0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

● AC Electrical Characteristics

O Read Cycle

($SRM2114_{25}$ . . . . V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = -40 to 85°C)

Parameter	Symbol	Conditions	SRM2114 25		Unit
			Min	Max	
Read cycle time	t_{RC}	*1	250	—	ns
Address access time	t_{ACC}		—	250	ns
$\overline{CE}$ access time	t_{ACE}		—	250	ns
$\overline{CE}$ output set time	t_{CLZ}	*2	0	—	ns
$\overline{CE}$ output floating	t_{CHZ}		—	120	ns
Output hold time	t_{OH}	*1	10	—	ns

O Write Cycle

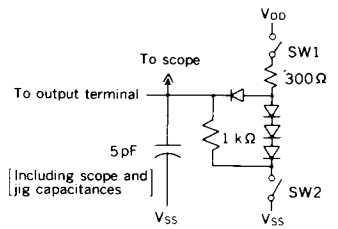
Parameter	Symbol	Conditions	SRM211425		Unit
			Min	Max	
Write cycle time	tWC	*1	250	—	ns
Address setup time	tAS		0	—	ns
Write pulse width	tWP		150	—	ns
Address hold time	tWR		0	—	ns
Input data setup time	tDW		100	—	ns
Input data hold time	tDH		0	—	ns
R/$\overline{W}$ output floating	tWHZ	*3	—	120	ns

*1 Test Conditions.

1. Input pulse level : 0.8 to 2.2V
2. tr = tf = 10ns
3. Output load : I_{TTL} + CL= 100pF (including scope and jig capacitances)
4. Timing reference level : 1.5V

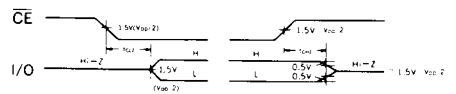
*2 Test Conditions

1. Input pulse level : 0.8 to 2.2V
2. tr = tf = 10ns
3. Test circuit



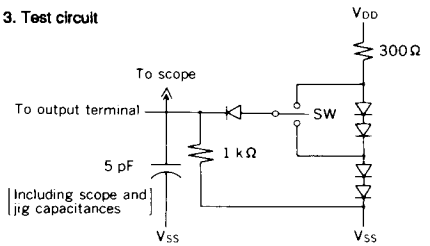
○SW1, SW2 are closed when measuring t_{CHZ}.
○SW1 is open, SW2 is closed when measuring Hi-Z→"High" of t_{CLZ}.
○SW1 is closed, SW2 is open when measuring Hi-Z→"Low" of t_{CLZ}.

Output turn-on turn-off times



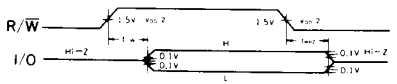
*3 Test Conditions

1. Input pulse level : 0.8 to 2.2V
2. tr = tf = 10ns
3. Test circuit



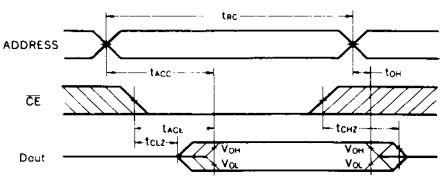
○SW is set to the V_{DD} side when measuring Hi-Z→"High" and "High"→Hi-Z of t_{OW} or t_{WHZ}.
○SW is set to the V_{SS} side when measuring Hi-Z→"Low" and "Low"→Hi-Z of t_{OW} or t_{WHZ}.

Output turn-on turn-off times



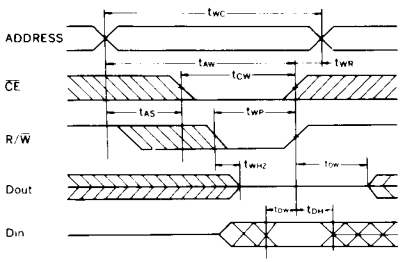
●Timing Chart

○Read Cycle



* R/$\overline{W}$ is "High" during read cycle.

○ Write Cycle

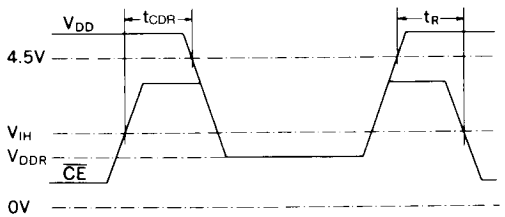


■ DATA RETENTION CHARACTERISTICS WITH LOW SUPPLY VOLTAGE

(SRM2114 25 . . . .Ta = -40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	V_I = 0 or V_{DD}, $\overline{CE}$ = V_{DD}	2.0	—	5.5	V
Data retention supply current	I_{DDR}	V_{DD} = 2.0V, 25°C	—	—	2	μA
$\overline{CE}$ setup time	t_{CDR}	Refer to the Figure Below	0	—	—	ns
$\overline{CE}$ recovery time	t_R		t_{RC}*	—	—	ns

Data retention timing



* When retaining data in standby mode, supply voltage can be lowered within a certain range. But read or write cycle cannot be performed while the supply voltage is low.

■ FUNCTIONS

● Truth Table

$\overline{CE}$	R/$\overline{W}$	A0 to A9	DATA I/O	MODE
H	X	X	Hi-Z	Unselected
L	L	Stable	Input data	Write
L	H	Stable	Output data	Read

X : "H" or "L"

● Reading Data

Data can be read out if an address is set while $\overline{CE}$ is "Low", and R/$\overline{W}$ is "High".

● Writing Data

There are the following two ways of writing data into the memory.

(1) Hold $\overline{CE}$ "L", set the address, and apply low level pulse to R/$\overline{W}$.

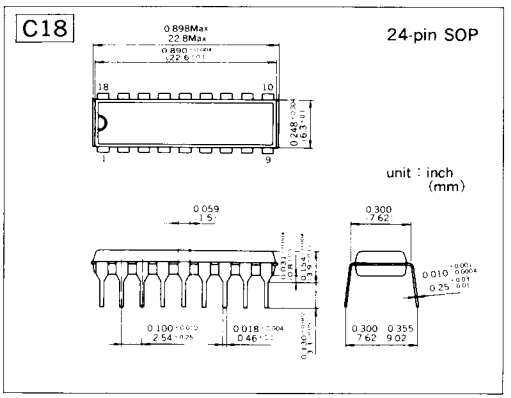
(2) Set the address and apply Low level pulse to $\overline{CE}$ and R/$\overline{W}$.

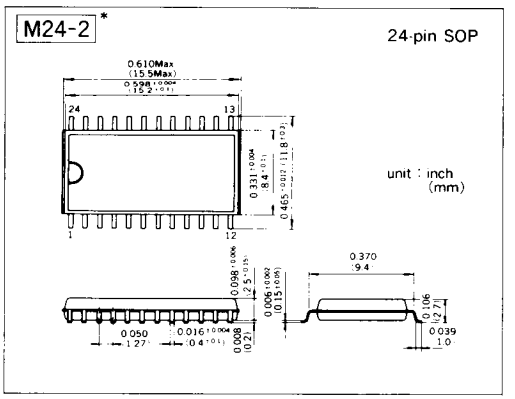
In each case, data from the DATA I/O terminal is latched at the positive transition of "L" pulse of $\overline{CE}$ or R/$\overline{W}$. The DATA I/O terminal is in high-impedance state when $\overline{CE}$ is "H" or R/$\overline{W}$ is "L", so competition of data driver and memory output can be avoided.

● Standby Mode

When $\overline{CE}$ is "H" SRM2114$_{25}$ is in standby mode and only retains the data. In this mode, DATA I/O terminals are in high-impedance state, and all inputs of addresses, R/$\overline{W}$, or data can be any "H" or "L". The current flowing in the SRM2114$_{25}$ is only leakage current.

■PACKAGE DIMENSIONS





*Represents model SRM2114M$_{25/L7}$ that has the same electrical characteristics as model SRM2114C$_{25/L7}$.

■CHARACTERISTICS CURVES