EPSON

SRM2B257SLC70/10

256K-Bit Static RAM

- Low Supply Current
- Access Time 100/120nS
- 32,768 Words×8-bit Asynchronous
- Two Chip Select Terminals

■ DESCRIPTION

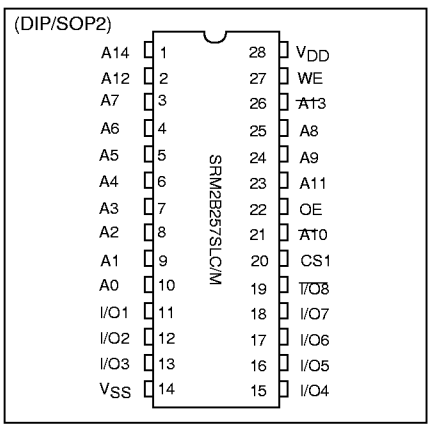
The SRM2B257SLC70/10 is a 32,768 word×8-bit asynchronous, static, random access memory fabricated using advanced CMOS technology. (memory cells are NMOS and outskirt circuits are CMOS.) Its very low standby power requir makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity. The inclusion of two chip select terminals simplifies the design of peripheral circuits for the memories.

■ FEATURES

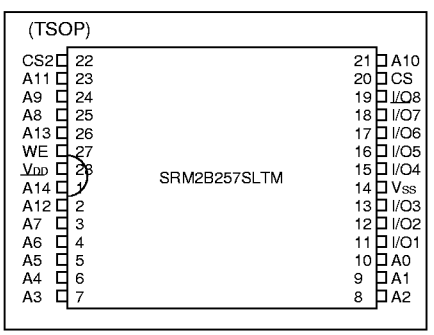
- Fast access time ..... SRM2B257SLC70 70ns (Max.)
  SRM2B257SLC10 100ns (Max.)
- Low supply current ..... stadby :0.5μA (Typ.)
  operation:10mA/1MHz (Typ.)
- Completely static ..... no clock required
- Single power supply ..... 5v±10%
- TTL compatible inputs and outputs
- 3-state output
- Battery back-up operation
- Package ..... SRM2B257SLC70/10 Plastic DIP-28pin
  SRM2B257SLM70/10 Plastic SOP2-28pin
  SRM2B257SLTM70/10 Plastic TSOP (I)-28pin
  SRM2B257SLRM70/10 Plastic TSOP (I)-28pin-R1

■ PIN CONFIGURATION

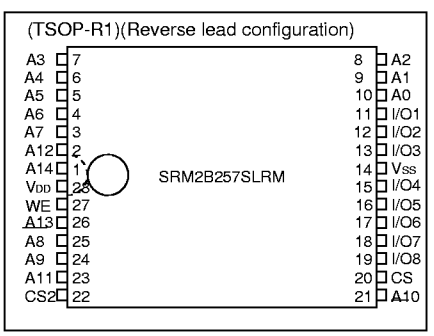
(DIP/SOP2)



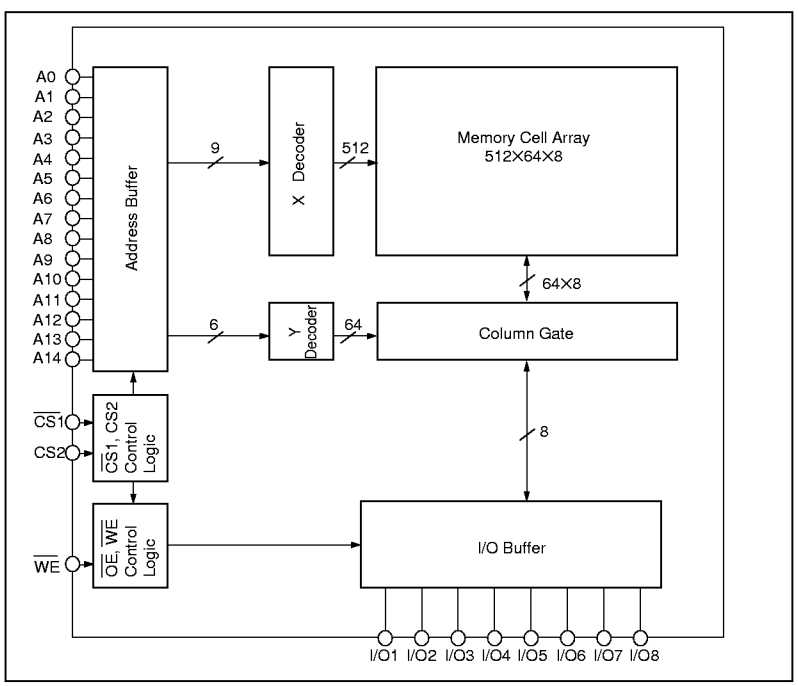
(TSOP)



(TSOP-R1)(Reverse lead configuration)



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

A0 to A14	Address Input
$\overline{WE}$	Write Enable
$\overline{CS1}$	Chip Select1
CS2	Chip Select2
I/O1 to 8	Data Input/Output
V_{DD}	Power Supplyy (+5V)
V_{SS}	Power Supply (0V)

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to 7.0	V
Input voltage	V_I	–0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	–0.5* to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (Lead only)	–

*V_I, $V_{I/O}$ (Min)=–3.0V when pulse width is less or equal to 50ns

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	–	V_{DD}+0.3	V
	V_{IL}		–0.3*	–	0.8	V

*V_{IL} (Min)=–1.0V when pulse width is less or equal to 50ns

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM2B257SLC70			SRM2B257SLC10			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input leakage	I_{LI}	V_I=0 to V_{DD}	–1	–	1	–1	–	1	µA
Standby supply current	I_{DDS}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	–	–	3.0	–	–	3.0	mA
	I_{DDS1}	$\overline{CS1}$=CS2≥V_{DD}–0.2V or CS2≤0.2V	–	0.5	20	–	0.5	20	µA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA, t_{cyc}=Min.	–	30	45	–	30	45	mA
	I_{DDA1}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA, t_{cyc}=1µs	–	–	10	–	–	10	mA
Operating supply current (DC)	I_{DDO}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA	–	–	10	–	–	10	mA
Output leakage	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{DD}	–1	–	1	–1	–	1	µA
High level output voltage	V_{OH}	I_{OH}=–1.0mA	2.4	–	–	2.4	–	–	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	–	–	0.4	V

Typical values are measured at Ta=25°C and V_{DD}=5.0V

● Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C_{ADD}	V_{ADD}=0V	–	–	8	pF
Input Capacitance	C_I	V_I=0V	–	–	8	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	10	pF

● AC Electrical Characteristics

❍ Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM2B257SLC70		SRM2B257SLC10		Unit
			Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	*1	70	–	100	–	ns
Address access time	t_{ACC}		–	70	–	100	ns
$\overline{CS1}$ access time	t_{ACS1}		–	70	–	100	ns
CS2 access time	t_{ACS2}		–	70	–	100	ns
$\overline{CS1}$ output set time	t_{CLZ1}	*2	10	–	10	–	ns
$\overline{CS1}$ output floating	t_{CHZ1}		–	25	–	35	ns
CS2 output set time	t_{CLZ2}		10	–	10	–	ns
CS2 output floating	t_{OHZ2}		–	25	–	35	ns
Output hold time	t_{OH}	*1	10	–	10	–	ns

❍ Write Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

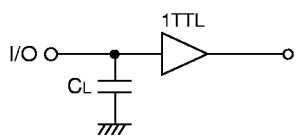
Parameter	Symbol	Conditions	SRM2B257SLC70		SRM2B257SLC10		Unit
			Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	*1	70	–	100	–	ns
Chip select time ($\overline{CS1}$)	t_{CW1}		60	–	80	–	ns
Chip select time (CS2)	t_{CW2}		60	–	80	–	ns
Address valid to end of write	t_{AW}		60	–	80	–	ns
Address setup time	t_{AS}		0	–	0	–	ns
Write pulse width	t_{WP}		45	–	60	–	ns
Address hold time	t_{WR}		0	–	0	–	ns
Input data set time	t_{DW}		30	–	40	–	ns
Input data hold time	t_{DH}		0	–	0	–	ns
Write to Output floating	t_{WHZ}	*2	–	25	–	35	ns
Output Active from end to wirte	t_{OW}		5	–	5	–	ns

*1 Test Conditions

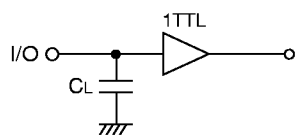
1. Input pulse level: 0.6V to 2.4V
2. t_r=t_f=5ns
3. Input and output timing reference levels : 1.5V
4. Output load C_L=100pF

*2 Test Conditions

1. Input pulse level : 0.6V to 2.4V
2. t_r=t_f=5ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200mV
   (the level displaced from stable output voltage level)
5. Output load C_L=5pF



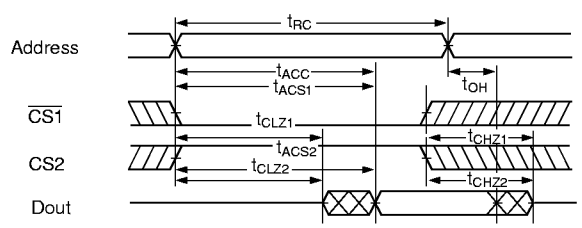
C_L=100pF (Includes Jig Capacitance)



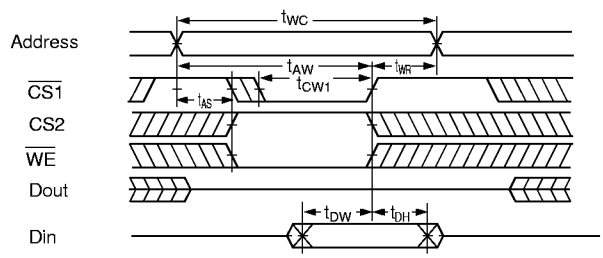
C_L=5pF (Includes Jig Capacitance)

● Timing chart

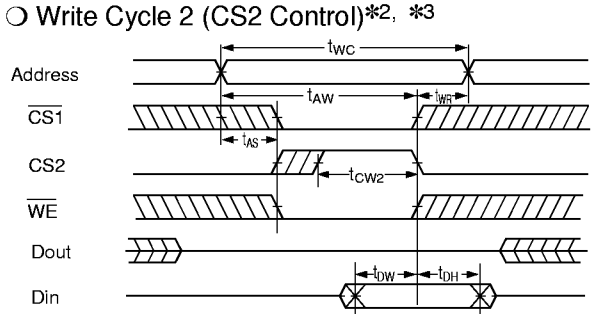
❍ Read Cycle*1



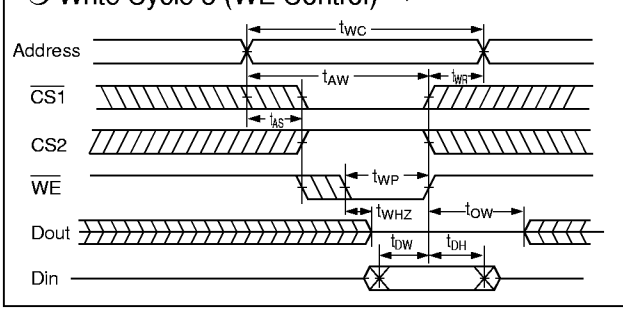
❍ Write Cycle 1 ($\overline{CS1}$ Control)*2, *3



❍ Write Cycle 2 (CS2 Control)*2, *3



❍ Write Cycle 3 ($\overline{WE}$ Control)*2, *3



Note : *1 During read cycle time, $\overline{WE}$ should be "H" level.

*2 During write cycle time that is controlled by $\overline{CS1}$ or CS2 Output Buffer is in high impedance.

*3 When I/O terminals are in output mode, be careful that opposite signals are not given to the I/O terminals.

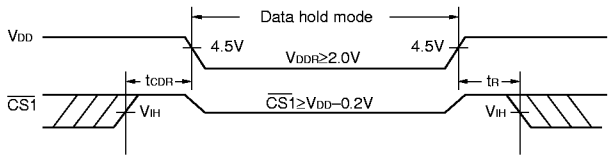
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(V_{SS}=0V, Ta=–40 to 40°C)

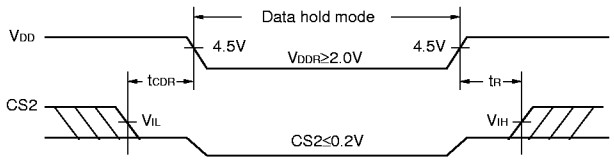
Parameter	Symbol	Conditions		Min.	Typ.*1	Max.	Unit
Data retention Supply voltage	V_{DDR}			2.0	–	5.5	V
Data retention current	I_{DDR}	V_{DDR}=3V, CS2≤0.2V or $\overline{CS1}$=CS2≥V_{DD}–0.2V	0 to 70°C	–	0.25	10	µA
			0 to 40°C	–	0.25	2	
Chip select data hold time	t_{CDR}			0	–	–	ns
Operation recovery time	t_R			5	–	–	ms

*1 Typical values are measured at 25°C

❍ **Data retention timing 1 (Controlling with $\overline{CS1}$)**



❍ **Data retention timing 2 (Controlling with CS2)**



Note: During standby mode in which the data is retentive, the supply voltage (V_{DD}) can be in low voltage until V_{DD}=V_{DDR}.
At this mode data reading and writing are impossible.

■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{WE}$	A0 to A14	DATA I/O	Mode	I_{DD}
H	X	X	X	Hi-Z	Standby	I_{DDS}, I_{DDS1}
X	L	X	X	Hi-Z	Standby	I_{DDS}, I_{DDS1}
L	H	L	Stable	D_{in}	Write	I_{DDA}, I_{DDA1}
L	H	H	Stable	D_{out}	Read	I_{DDA}, I_{DDA1}

X : "H" or "L"

● Read Mode

Data is read with setting addresses while holding $\overline{CS1}$ ="L", CS2 ="H" and $\overline{WE}$ ="H".

● Write Mode

There are following 4 ways of writing data into memory.

(1) Hold $\overline{CS1}$ ="L", $\overline{WE}$ ="L", set address, and give "H" pulse to CS2.

(2) Hold $\overline{CS2}$ ="H",$\overline{WE}$ ="L", set address, and give "L" pulse to $\overline{CS1}$.

(3) Hold $\overline{CS1}$ ="L", CS2 ="H", set address, and give "L" pulse to $\overline{WE}$.

(4) After setting addresses, give "L" pulse to both $\overline{CS1}$ and $\overline{WE}$, and also give "H" pulse to CS2.

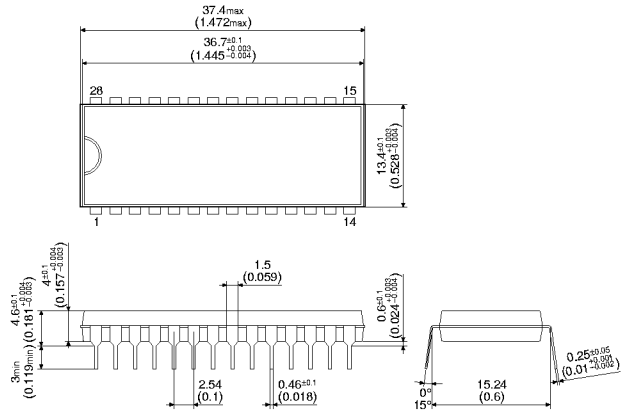
In the above cases, the data on the DATA I/O terminals are latched up into the SRM2B257SLC$_{70/10}$ when $\overline{CS1}$ and or $\overline{WE}$ are in positive-going of "L" pulse of CS2 are in the negative-going of "H" pulse. Since DATA I/O terminals are in high impedance, when $\overline{CS1}$ ="H" or CS2 ="L", bus contention between data driver and memory outputs can be avoided.

● Standby Mode

When $\overline{CS1}$ is"H", or CS2 is "L", the SRM2B257SLC$_{70/10}$ is in the standby mode. In this case data I/O terminals are in Hi-Z, so that all inputs of addresses. $\overline{WE}$ and all input data are inhibited. When $\overline{CS1}$ and CS2 ≥V_{DD}-0.2V, CS2 ≤0.2V, there is a small current in the SRM2B257SLC$_{70/10}$ which flow through the high resistances of the memory cells only.

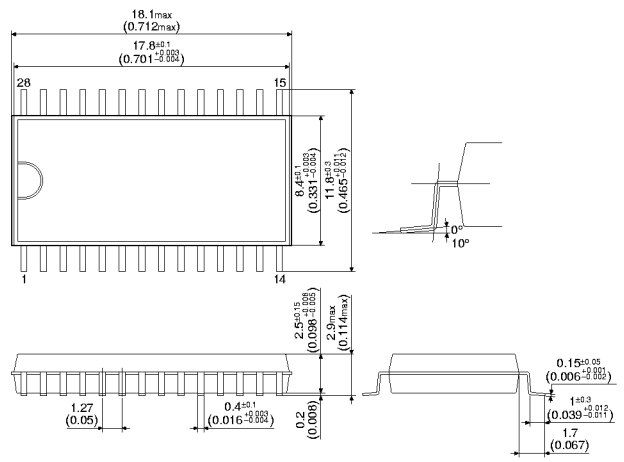
■ PACKAGE DIMENSIONS

Plastic DIP-28pin (600mil)



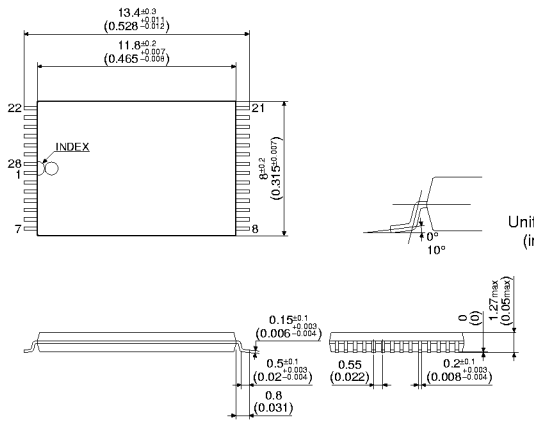
Unit : mm
(inch)

Plastic SOP2-28pin (450mil)



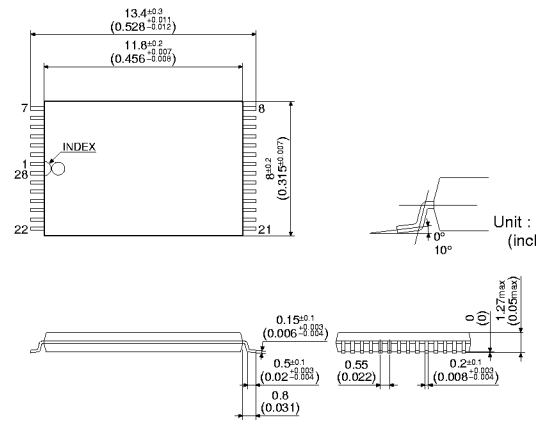
Unit : mm
(inch)

Plastic TSOP(I)-28pin



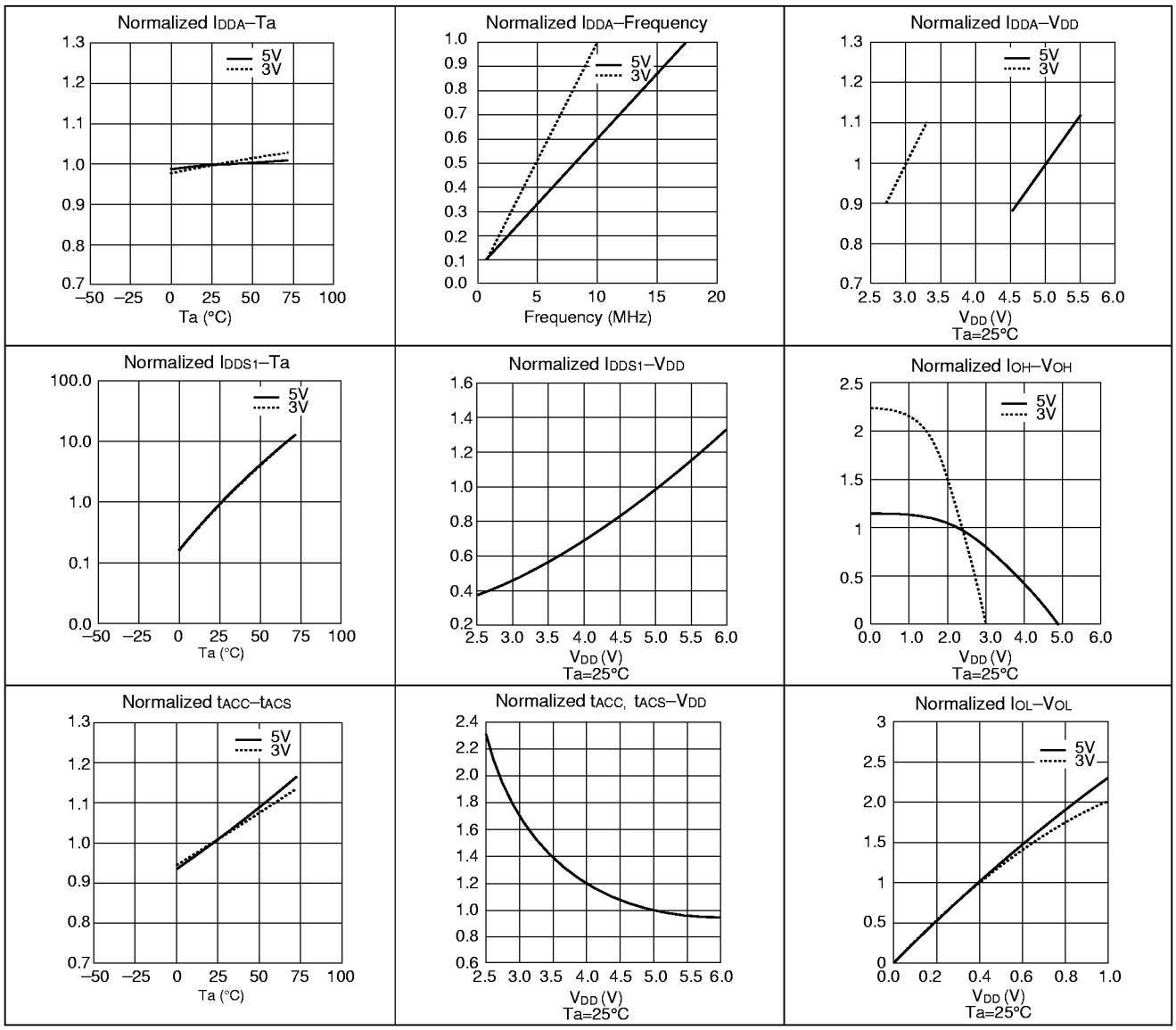
Unit : mm
(inch)

Plastic TSOP(I)-28pin-R1



Unit : mm
(inch)

■ CHARACTERISTICS CURVES



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