R/W Preamplifier for 3 Terminal Recording Heads, 2, 4, or 6, Channels

GENERAL DESCRIPTION

The XR-510A is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-510A is compatible with 2" to 14" single and multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring from two to six center-tapped read/write heads Multiple devices are easily cascaded for drives with more heads.

The XR-510AR option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-510A, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

Complete Head Interfacing Functions, Read and Write
Low Noise Preamplifier
High Dynamic Range and Bandwidth
Available in Two, Four and Six Head Versions
Easily Cascaded for Larger Systems
Full Featured Power Monitor
TTL Compatible Control Inputs
Optional Internal Damping Resistors
Fast Settling Time

APPLICATIONS

Hard Disk Drives with MIG, ferrite, or composite heads

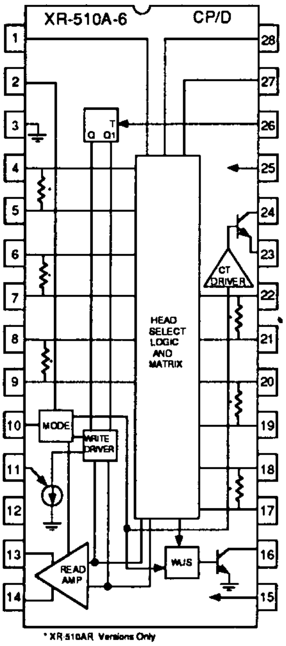
ABSOLUTE MAXIMUM RATINGS

V_{DD}	15 V
V_{CC}	6 V
Digital Inputs	-0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

SYSTEM DESCRIPTION

The XR-510A consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of six heads, and associated control and monitoring functions.

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-510A-2CP	18 Pin Plastic DIP	0°C to 70°C
XR-510A-2D	18 Pin SO	0°C to 70°C
XR-510A-4CP	22 Pin Plastic DIP	0°C to 70°C
XR-510A-4D	24 Pin SO	0°C to 70°C
XR-510A-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-510A-6CJ	28 Pin PLCC	0°C to 70°C
XR-510A-6D	28 Pin SO	0°C to 70°C
XR-510AR-2CP	18 Pin Plastic DIP	0°C to 70°C
XR-510AR-2D	18 Pin SO	0°C to 70°C
XR-510AR-4CP	22 Pin Plastic DIP	0°C to 70°C
XR-510AR-4D	24 Pin SO	0°C to 70°C
XR-510AR-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-510AR-6CJ	28 Pin PLCC	0°C to 70°C
XR-510AR-6D	28 Pin SO	0°C to 70°C

Less than 1.0 nV/ Hz (nominal) noise allows error free operation with small input signals. Over 40 mA of write current output (user adjustable) is available. Preamplifier offset voltages are low, aiding use in "wedge" servo drives and in other applications where rapid system settling times are needed.

ELECTRICAL SPECIFICATIONS
Test Conditions: $T_A = 25°C$, $V_{CC} = 5$ V, $V_{DD} = 12$ V, $I_W = 40$ mA, $R_D = 750\Omega$, $C_L (R_{D+}, R_{D-}) \leq 20$ pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	Min	TYP	MAX	UNIT	CONDITION
I_{CC}	Supply Current			35	mA	$V_{CC} = 5.5$ V, Read or Idle Mode
				30	mA	$V_{CC} = 5.5$ V, Write Mode
I_{DD}	Supply Current			20	mA	$V_{DD} = 13.2$ V, Idle Mode
				40	mA	$V_{DD} = 13.2$ V, Read Mode
				20	mA	$V_{DD} = 13.2$ V, Write Mode, $I_W = 0$ mA
PD	Power Dissipation			400	mW	Idle Mode - $V_{CC} = 5.5$ V, $V_{DD} = 13.2$ V
				600	mW	Read Mode - $V_{CC} = 5.5$ V, $V_{DD} = 13.2$ V
				670	mW	$I_W = 40$ mA, $R_{CT} = 160\Omega$
				800	mW	$I_W = 40$ mA, $R_{CT} = 0\Omega$
V_{CT}	Center Tap Voltage		5.0		V	Read Mode
			7.0		V	Write Mode
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
		8.5	9.6	10.5	V	V_{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	$I_{OL} = 8$ mA
I_{OH}	Leakage Current			100	µA	$V_{OH} = 5$ V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current	-0.4			mA	$V_{IL} = 0.8$ V
I_{IH}	Input High Current			100	µA	$V_{IH} = 2.0$ V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-5		5	%	Error from $I_W = \frac{2.5V}{R_W}$
	Recommended Write Current Range	10		40	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak (Inductive Load)
	Unselected Differential Head Current			85	µA	Peak
	Unselected Transient Current			2	mA	Peak

SYMBOL	PARAMETER	Min	TYP	MAX	UNIT	CONDITION
	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10			KΩ	XR-510A
		635	750	865	Ω	XR-510AR
	WD Rate/Transistion Freq.	250	500		kHz	
K_I	Current Source Factor		1			$K_I = I_W$/(Current through R_W)
K	Write Current Constant	2.375	2.50	2.625	V	$K = I_W \cdot R_W$
	Write Protection Leakage Current	-200		200	µA	Per Side, $V_{CC} \leq 3.7$ V and/or $V_{DD} \leq 8.5$ V
V_{OS}	Preamplifier Output Offset Voltage	-20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	-100		100	µA	Write or Idle Mode, RD += R_{D-} = 6 V
READ MODE						
A_V	Differential Voltage Gain	85		115	V/V	V_{IN} = 1 mVp-p at 300 kHz, $R_L+ = R_L- = 1K\Omega$
	Dynamic Range	-3		+3	mV	DC input voltage where gain drops 10%. $V_{in} = V_i + 0.5$ mVp-p at 300 KHz.
R_{IN}	Differential Input Resistance	2			KΩ	XR-510
		500	650	850	Ω	XR-510AR
C_{IN}	Differential Input Capacitance			20	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	$nV/\sqrt{HZ}$	$L_h = 0$, $R_h = 0$, B_W = 15 MHz
BW	Bandwidth	30	60		MHz	-3 dB Point, $\lvert Z_s \rvert \leq 5\Omega$, V_{in} = 1 mVp-p
I_B	Input Bias Current		10	45	µA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Super-imposed on V_{DD1},V_{DD2} or V_{CC}

SYMBOL	PARAMETER	Min	TYP	MAX	UNIT	CONDITION
READ MODE (cont.)						
	Channel Separation	45	60		dB	Unselected Channel: V_{IN} - 100 mVp-p at 5 MHz. Selected Channel V_{IN} - 0 V
V_{OS} Out	Output Offset Voltage	-440	-+50	440	mV	
ΔV_{OS}	Output Offset Voltage Change		-+20		mV	Switching between any two heads
V_{CM}	Common Mode Output Voltage	4.5	5.5	6.5	V	
ΔV_{CM}	V_{CM} Change from Write to Read		500		mV	Common Mode Output Voltage Change from Write to Read or Read to Write
	Head Current Leakage	-200		200	µA	Per Side
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/$\overline{W}$	Read to Write		0.1	1	µs	Note 1
	Write to Read		0.1	1	µs	Notes 2,3
$\overline{CS}$	Start-up Delay		0.1	1	µs	Notes 1,2
	Inhibit Delay		0.1	1	µs	Note 3
	Head Switching Delay		0.1	1	µs	Note 2, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6	2	8.0	µs	I_W = 35 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µs	I_W = 35 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay		2	25	ns	Note 4, See Figure 1, TD3
	Asymmetry		0.1	2	ns	Note 5
	Rise or Fall Time		1	20	ns	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.
Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.
Note 3: Delay to 90% Decay of I_W.
Note 4: From 50% Points. L_h = 0µH, R_h = 0Ω.
Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

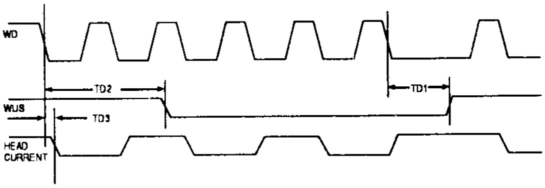


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity. Improved write stability over 117-type devices is achieved by employing a unity gain write current constant.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/$\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude IW, set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (WUS) signals the disk oontroller whenever one of six error conditions exist and writing should be discontinued. The six faults are: -open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/W high enables the data readback mode. The head read signal is amplified by the low noise differential stage and is output by low impedance drivers for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency. high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-510A is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-510AR option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-510AR option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-510A lead to a certain degree of electrostatic discharge (ESD) suseptability, so static reducing precautions should be taken.

Write Mode Design Considertions

Write current, I_W. typically between 20 mA and 40 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{2500}{I_W}$$

where I_W is in mA and R_{IW} is in Ohms.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 150 \frac{(40)}{Iw}$$

where R_{CT} is in Ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. If RCT is not used, VDD2 is directly conneded to VDD1.

Write Unsafe Indicator (WUS)

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exists. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS This output is for indication only, intended for signaling a controller, and does not stop the write operation. A pull-up resistor of from 2K Ω to 10KΩ is necessary for operation of this open collector output.

Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V and/or V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable.

Device operation at standard voltages (V_{CC} = 5 V ±10%, V_{DD1} = 12 V ± 10%) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

Read Mode Design Considerations

The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (1.0nV/√Hz typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.3 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100μA.

The XR-510A read preamplifier is specifically designed to minimize output common mode voltage changes between write mode and read mode, thus reducing switching transients that slow write to read recovery time. DC shifts are typically held under 500mV from the 5.3V nominal bias level.

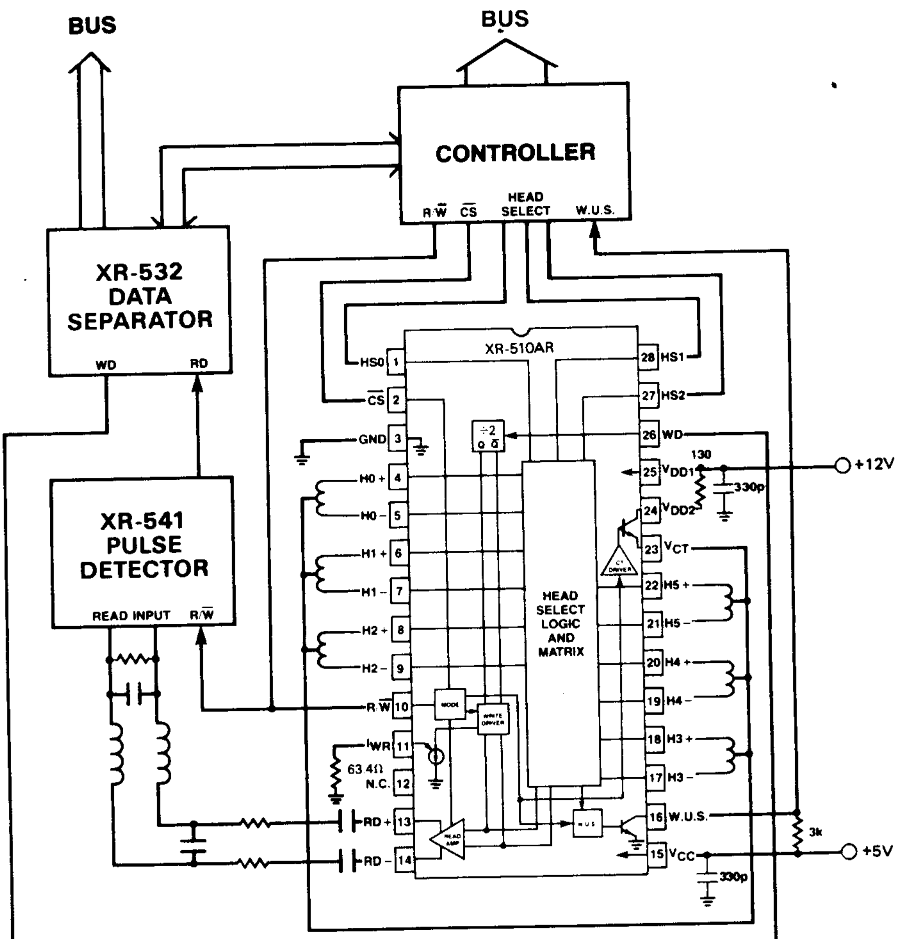


Figure 2. Hard Disk Read/Write Applications Circuit
Note: Circuit shown for XR-510AR. Non-R versions require damping resistors across each head.

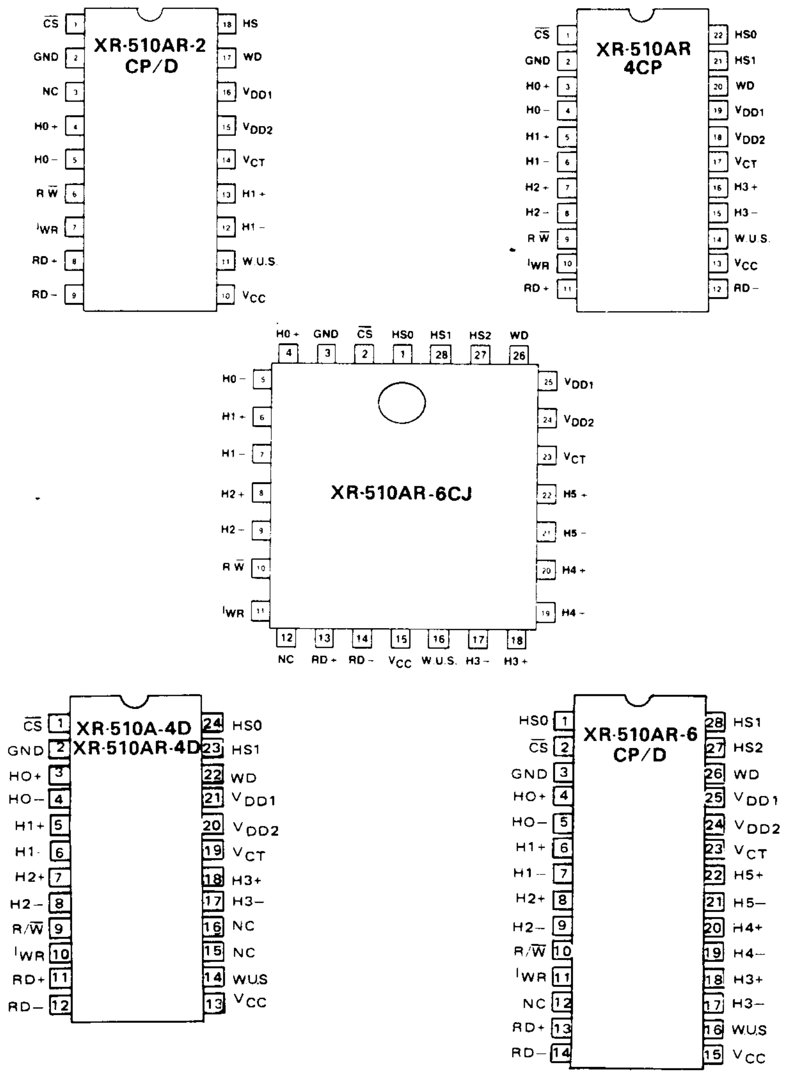


Figure 3. Additional Packages for XR-510A