SSI 32F8020/8022
Low-Power Programmable Electronic Filter

December 1991

T-64-05

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DESCRIPTION

The SSI 32F8020/8022 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, .05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation makes the SSI 32F8020/8022 ideal for use in constant density recording applications. Double differentiation pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

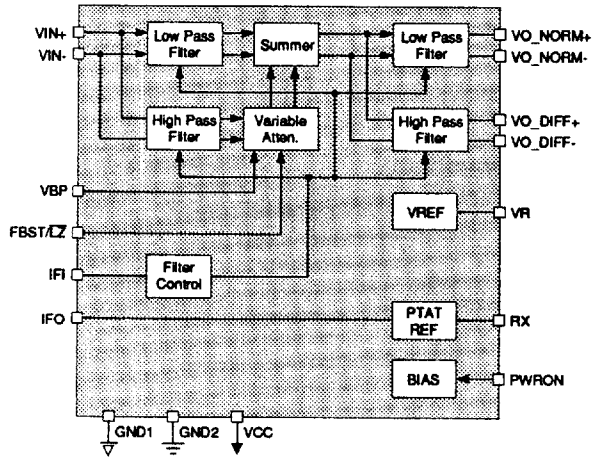
The SSI 32F8020/8022 programmable equalization and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 time base generator. Fixed characteristics are easily accomplished with three external resistors. For the SSI 32F8020, equalization can be switched in or out by a logic signal. The input impedance of the SSI 32F8022 can be clamped low for fast recovery from input overload.

The SSI 32F8020/8022 requires only a +5V supply and is available in 16-pin DIP, SON, and SOL packages.

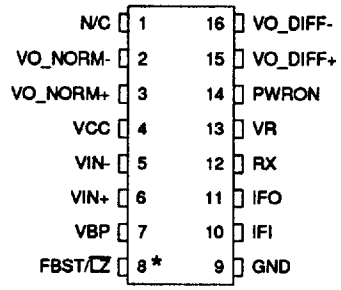
FEATURES

- **Ideal for constant density recording applications**
- **Programmable filter cutoff frequency (f_c = 1.5 to 8 MHz)**
- **Programmable pulse slimming equalization (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 1.5 - 8 MHz**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-pin DIP, SON, and SOL package**

BLOCK DIAGRAM



PIN DIAGRAM



* Pin 8 = FBST - SSI 32F8020
LZ - SSI 32F8022

CAUTION: Use handling procedures necessary for a static sensitive component.

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FUNCTIONAL DESCRIPTION

The SSI 32F8020/8022 is a high performance programmable electronic filter. It features a 7-pole 0.05° phase equiripple filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54X family pulse detectors, and the SSI 32P4622 combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, of the SSI 32F8020/8022 is defined as the -3dB filter bandwidth with no magnitude equalization applied, and is programmable from 1.5 MHz to 8 MHz.

The cutoff frequency is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{RX} \text{ at } T = 27°C$$

IFI should be made proportional to IFO for temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as follows:

$$fc(MHz) = 8x\frac{IFI}{IFO}x\frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 8x\frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. The IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current from its reference to full scale output is used, a 5-kΩ RX is used. The fc is then given as follows:

$$fc(MHz) = 8x\frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit digital input for the DACF.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 9 dB boost is applied, the magnitude response peaks up 6 dB above the DC gain.

The magnitude equalization is programmable with two pins: VR and VBP. The VR is a bandgap reference voltage, 2.2 V typically. The voltage at the VBP pin determines the amount of high frequency boost. The boost function is as follows:

$$Boost(dB) = 20\log_{10}[1.884(\frac{VBP}{VR}) + 1]$$

For a fixed boost setting, a resistor divider between VR to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VR should be the reference voltage to the DAC. The DAC output voltage is then proportional to VR. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters. When DACS is used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}[1.884(\frac{S\_Code}{127}) + 1]$$

where S_Code is the decimal code equivalent to the 7-bit digital input for the DACS.

For the SSI 32F8020, the equalization function can be disabled when FBST is pulled to logic 0. For the SSI 32F8022, the VBP pin should be grounded to achieve 0 dB boost.

LOW INPUT IMPEDANCE (SSI 32F8022 only)

When the $\overline{LZ}$ is at logic 1 or left open, the SSI 32F8022 input is at high impedance state. When the $\overline{LZ}$ is pulled to logic 0, the SSI 32F8022 input is clamped to a low impedance state, 200 Ω typical.

POWER ON/OFF

The SSI 32F8020/8022 supports a power down mode for minimal idle dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

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PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to load.
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to load.
RX	PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pin.
IFO	PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFI.
IFI	FREQUENCY PROGRAM INPUT. The filter cutoff frequency fc, is set by an external current IFI, injected into this pin. IFI must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO.
VBP	FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST (32F8020 only)	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. No boost is applied if the FBST pin is grounded, or at logic low.
$\overline{LZ}$ (32F8022 only)	LOW IMPEDANCE MODE. With a low logic level, the analog input impedance is switched low for fast recovery from input overload. With a high logic level or left open, the input is at high impedance state.
PWRON	POWER ON. A high logic level circuit enables the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC	+5 VOLT SUPPLY.
GND	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC	V
Maximum Power Dissipation, fc = 8 MHz, Vcc = 5.5V	226	mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC	4.50 < VCC < 5.50	V
Ambient Temperature	0 < Ta < 70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Characteristics						
ICC	Power Supply Current	PWRON = 0.8V			3	mA
ICC	Power Supply Current	PWRON ≥ 2.2V		35	41	mA
PD	Power Dissipation	PWRON ≥ 2.2V, VCC = 5.0V		175	205	mW
		PWRON ≥ 2.2V, VCC = 5.5V		193	226	mW
DC Characteristics						
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V			−1.5	mA
Filter Characteristics						
fc	Filter Cutoff Frequency	Rx = 5kΩ $fc = (\text{ideal})\,8\text{MHz} \cdot \frac{\text{IFI}}{4\text{IFO}}$	1.5		8.0	MHz
FCA	Filter *fc* Accuracy	*fc* (nominal) = 8 MHz	−10		+10	%
AO	VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.8	0.9	1.0	V/V
AD	VO_DIFF Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.8AO		1.2AO	V/V
FB	Frequency Boost at *fc*	$\text{FB(db)} = 20 \log \left[1.884 \left(\frac{\text{VBP}}{\text{VR}} \right) + 1 \right]$ VBP = VR		9.2		dB
FBA	Frequency Boost Accuracy	FB (ideal) = 9.0 dB	−1		+1	dB
TGD0	Group Delay Variation Without Boost	*fc* = 8 MHz, VBP = 0V F = 0.2 *fc* to *fc*	−1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 *fc* to *fc*, VBP = 0V	−2		+2	%
TGDB	Group Delay Variation With Boost	*fc* = 8 MHz, VBP = VR F = 0.2 *fc* to *fc*	−1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 *fc* to *fc*, VBP = VR	−2		+2	%

ELECTRICAL CHARACTERISTICS (Continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Filter Characteristics, continued						
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
VIF	Filter Input Dynamic Range	THD = 3% max, F = 0.67 *fc*	2.0			Vpp
VOF	Filter Output Dynamic Range	THD = 3% max, F = 0.67 *fc*	2.0			Vpp
RIN	Filter Diff Input Resistance	32F8020 32F8022 $\overline{LZ}$ = 1	3.0			kΩ
		32F8022 $\overline{LZ}$ = 0		200		Ω
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = 0.0V		6.3	7.5	mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = 0.0V		2.7	4.0	mVRms
EOUT	Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = VR		9.4	11.0	mVRms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = VR		3.7	4.5	mVRms
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance (Single ended)	IO+ = 1.0 mA			60	Ω
Filter Control Characteristics						
VR	Reference Voltage		2.0		2.40	V
VBP	Frequency Boost Control Voltage Range	VR = 2.2V FBOOST = 0 to 9.2 dB	0		2.2	V
VRX	PTAT Reference Current Set Output Voltage	TA = 25°C IRX = 0 - 0.6 mA Rx > 1.25 kΩ		750		mV
IFO	PTAT Reference Current, Output Current Range	TA = 25°C 1.25 kΩ < Rx < 6.8 kΩ IFO = VRX/Rx VRX = 750 mV	0.11		0.6	mA
RIFO	IFO Output Impedance		50			kΩ
VIFO	IFO Voltage Compliance		0		Vcc -1	V

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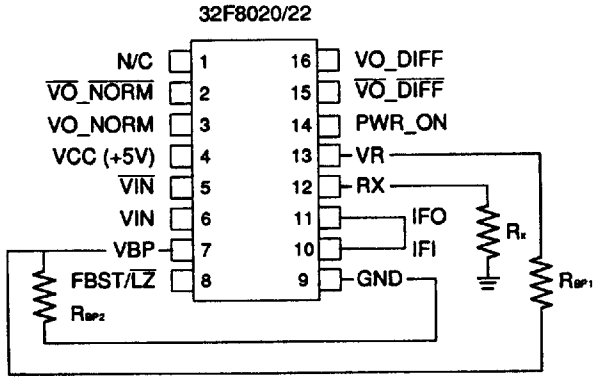
ELECTRICAL CHARACTERISTICS, (Continued)

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Filter Control Characteristics (continued)						
IFI	PTAT Programming Current Range	TA = 25°C, VRX = 750 mV	0.11		0.6	mA
RIFI	IFI Input Impedance		1.0		2.5	kΩ
VIFI	IFI Voltage Compliance		0.5		2.5	V



VR = 2.2V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

Fixed frequency programming is accomplished as shown in the drawing above. In this case IFI (programming current) is equivalent to IFO (reference current). Programming current is then set by VRX/Rx.

where: fc = 8.0 MHz then

IFI = IFO = 0.60 mA @25°C

Rx = 750 mV/0.60 mA = 1.25 kΩ

FIGURE 1: 32F8020/8022 Applications Setup

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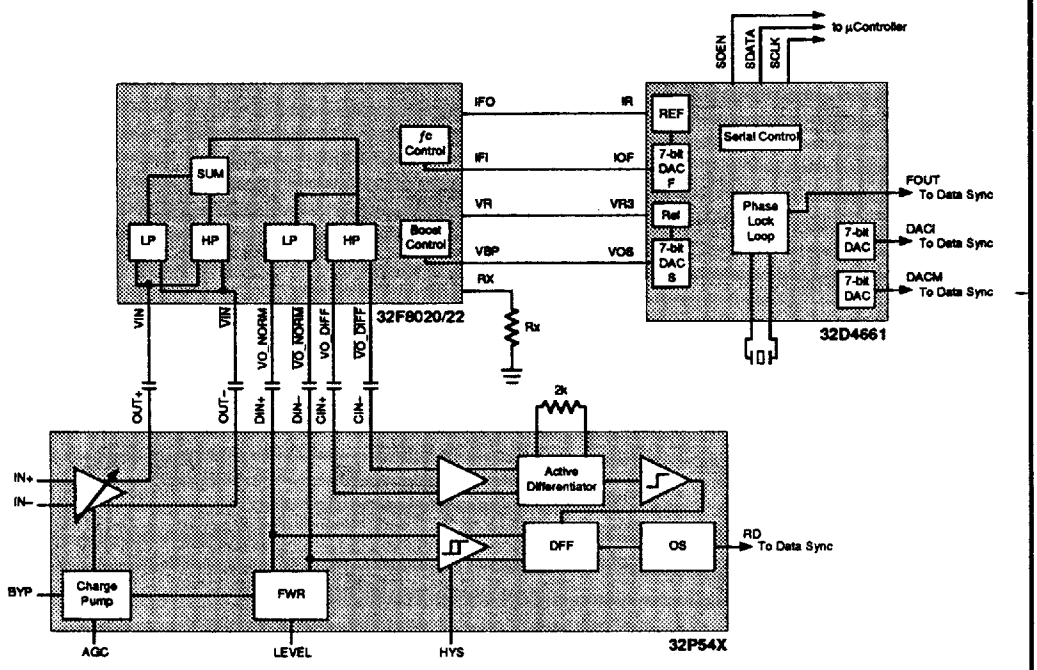

VR = 2.2V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

In this case the IFI (programming current) is scaled from IFO (reference current) through DACF on the 32D4661. DACF has a current gain of 4; therefore, the reference current should be set to 25% of the maximum desired IFI (programming current).

where: f_C (max) = 8.0 MHZ then

IFI (max) = 0.60 mA @25°C

IFO (max) = 0.15 mA

therefore Rx = 750 mV/0.15 mA = 5 kΩ

FIGURE 2: Applications Setup, Constant Density Recording 32F8020/8022, 32P54X, 32D4661

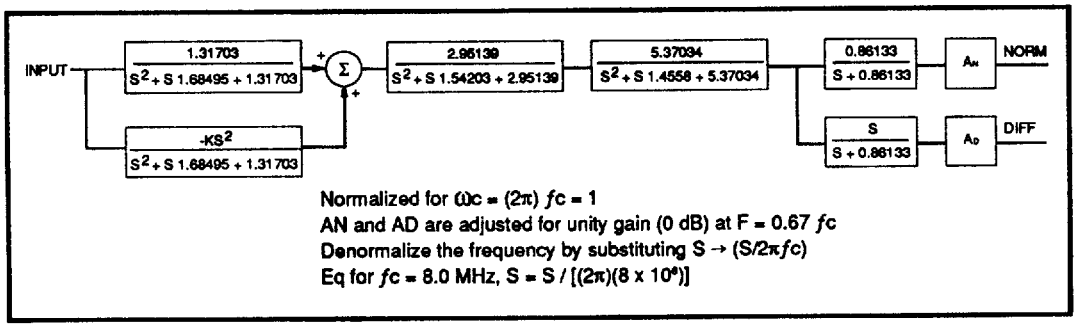

FIGURE 3: 32F8020/8022 Normalized Block Diagram

TABLE 1: 32F8020/8022 Frequency Boost Calculations

Assuming 9.2 dB boost for **VBP = VR**

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

Boost	VBP/VR
1 dB	0.065
2 dB	0.137
3 dB	0.219
4 dB	0.310
5 dB	0.413
6 dB	0.528
7 dB	0.658
8 dB	0.802
9 dB	0.965

or,

$$\text{boost in dB} \cong 20 \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$$

VBP/VR	Boost
0.1	1.499 dB
0.2	2.777 dB
0.3	3.891 dB
0.4	4.879 dB
0.5	5.765 dB
0.6	6.569 dB
0.7	7.305 dB
0.8	7.984 dB
0.9	8.613 dB
1.0	9.200 dB

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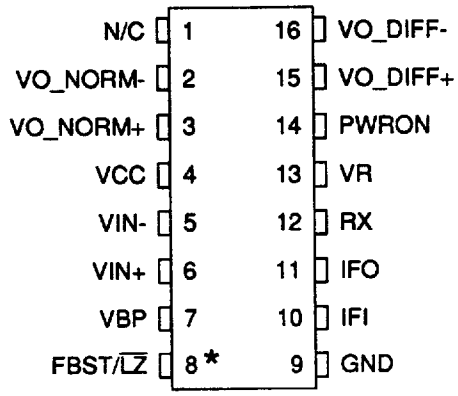
PACKAGE PIN DESIGNATIONS

(Top View)



* Pin 8 = FBST - SSI 32F8020
LZ - SSI 32F8022

32F8020/8022
16-pin DIP, SON, SOL

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8020		
Standard Width 16-Pin Plastic Dip	32F8020-CP	32F8020-CP
Narrow Width (150 Mil.) Small Outline	32F8020-CN	32F8020-CN
Large Width (300 Mil.) Small Outline	32F8020-CL	32F8020-CL
SSI 32F8022		
Standard Width 16-Pin Plastic Dip	32F8022-CP	32F8022-CP
Narrow Width (150 Mil.) Small Outline	32F8022-CN	32F8022-CN
Large Width (300 Mil.) Small Outline	32F8022-CL	32F8022-CL

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