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SSI 32H6840
Advanced Servo and Spindle Predriver with DSP
Advance Information

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DESCRIPTION

The SSI 32H6840 Advanced Servo and Spindle Predriver with DSP is a CMOS monolithic integrated circuit housed in a 128-lead QFP package, operates at five volts, provides control signals for external MOSFETs operating at twelve volts, and includes all key functionality necessary to implement the control of a hard disk drive spindle motor and head positioning servo. The device includes an industry standard compatible DSP core, data acquisition and conversion, predriver control of brushless, three-phase spindle motors without sensors using Silicon Systems' SilentSpin™ technology, predriver control of voice coil positioning motor, and power fault detection circuits. The integrated DSP is code compatible with the TMS320C25™ and includes internal program and data RAM.

FEATURES

- **Integrated TMS320C25™ code compatible 15 MIPS DSP core**
- **1568 words of configurable internal program and data memory**
- **Full external DSP bus for peripherals**
- **Relocatable on-chip peripheral paging**
- **Automatic wait state generation for external ROM, RAM, and peripherals**
- **1 µs, 10-bit A/D with 8 input MUX**
- **Two 10-bit voltage D/As with references**
- **16-bit D/A in cascade mode**
- **Auto and manual A/D convert modes**
- **SilentSpin™ spindle predriver**
- **12-bit pulse density PWM spindle D/A**
- **Spindle speed period counter**
- **Synchronized spindle master speed and phase counters**
- **Programmable brake delay**
- **Class B VCM predriver**
- **Error summing amplifier saturation detector**
- **Dual level retract for VCM**
- **Compatible with Silicon Systems' PRML Read Channel 32P49xx family**
- **Precision low voltage +5V and +12V monitors with velocity limited retract**
- **Extensive power saving modes**

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BLOCK DIAGRAM

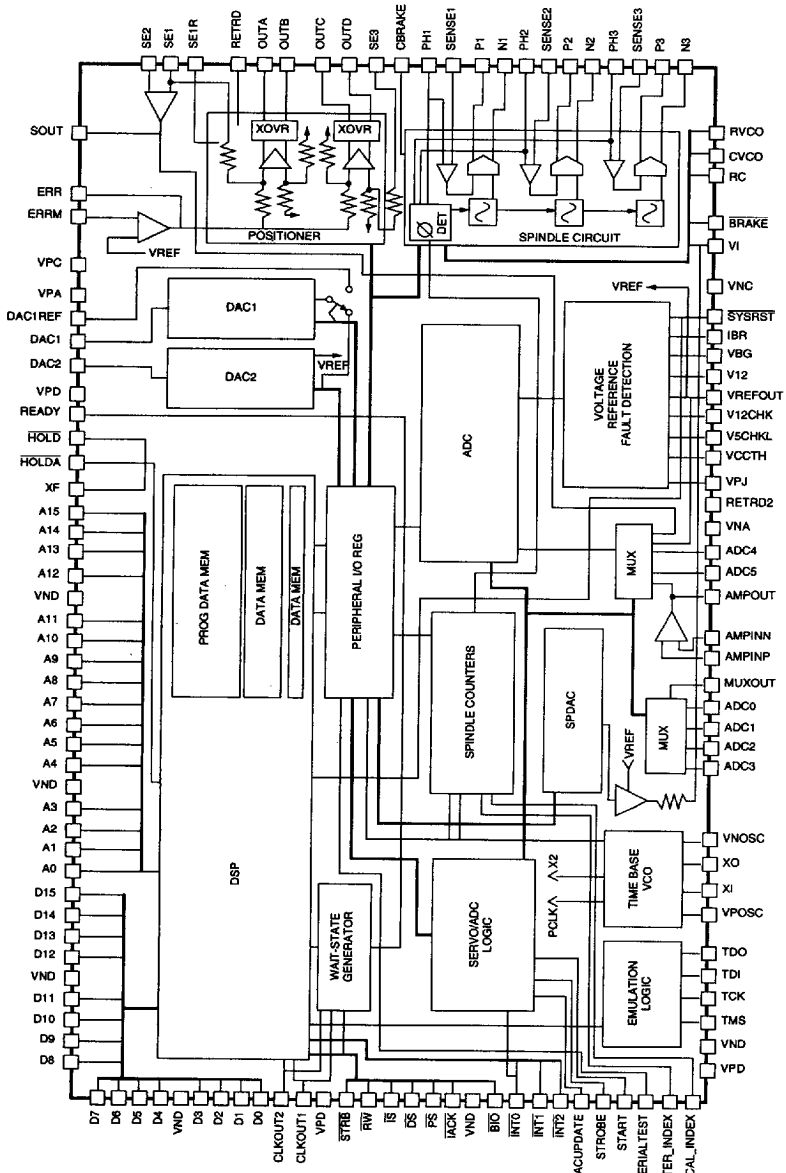

TABLE 1: Interrupt Sources

SOURCE	LEVEL	DESCRIPTION
RSB	1	External Reset Signal
INT0	2	External User Interrupt #0
INT1	3	External User Interrupt #1
INT2	4	External User Interrupt #2
TINT	5	Interval Timer Interrupt
TRAP	N/A	Software Interrupt

FUNCTIONAL DESCRIPTION

The SSI 32H6840 functional block diagram contains five major sections. These sections are Logic Functions (DSP core, DSP memory, wait-state generator, Peripheral I/O, servo logic, spindle timers, time base, emulation logic, and spindle DAC), ADC and DACs, Actuator Predriver, Spindle Predriver, Voltage Reference and Power Fault Detection.

DSP CORE

The DSP core is code compatible with the industry standard TMS32C025™. This high-speed, 15 MIPS core internally includes 1568 words of configurable program and data RAM. An internal wait state generator simplifies attachment of external peripherals. The on-chip peripheral page address is programmable and may be overlaid with internal data RAM for maximum algorithm performance.

EXTERNAL CONNECTIONS

An on-chip frequency synthesizer generates a 60 MHz system clock from an external 10 MHz crystal or clock source. This system clock operates a 4 stage instruction pipeline thereby determining the maximum instruction rate of 15 MIPS. The full address, data, and control bus is accessible so that external peripherals including program memory, data memory, and IO devices may be attached. Internal wait state generation is configurable for external bus transfers by type, address range, and duration. Hardware interrupt sources include three external pins and one internal timer interval interrupt as shown in Table 1.

DEVELOPMENT TOOLS

Development support for the 32H6840 includes JTAG Emulation Port, (compatible with IEEE 1149.1 standard), and a C source level debugger. Source code may be written in assembly or C languages. The 32H6840 debugger is compatible with many third party software tools as well.

PERIPHERAL IO PAGE

The DSP communicates with on-chip peripherals through the peripheral IO registers. These registers are accessible as data memory space. The page in data memory of these registers is programmed by the DSP by writing to the peripheral IO page bits 8..0 in memory mapped register PPWSC. The peripheral IO addresses always occupy the highest 16 words in their programmed data page. The peripheral IO page can be placed anywhere including the pages of internal RAM blocks B0 and B1. By programming the peripheral IO page to share the same data page as the most frequently used data memory, the peripheral IO registers may be accessed without the need to reload the data page pointer thereby significantly reducing instruction overhead.

WAIT STATE GENERATION

An on-chip programmable wait state generator simplifies the attachment of external program and data memory. The memory wait state generator register MEMWSG defined in Table 2 partitions the two memory spaces into four address segments each. Each memory segment can be assigned a different number of automatically inserted wait states as determined by the two-bit code. A two-bit code is further translated by values in the wait state control register PPWSC, (bits 14 and 15), into one of four values corresponding from zero to seven wait states.

TABLE 2: MEMWSG Definition

2-BIT WAIT STATE CODE	MEMORY SPACE	ADDRESS SEGMENT
0..1	program	0000H..3FFFH
2..3	program	4000H..7FFFH
4..5	program	8000H..BFFFH
6..7	program	C000H..FFFFH
8..9	data	0000H..3FFFH
10..11	data	4000H..7FFFH
12..13	data	8000H..BFFFH
14..15	data	C000H..FFFFH

TABLE 3: PPWSC Definition

BIT	DESCRIPTION
0..8	Peripheral IO Page Pointer
9..10	Not Used
11	Program wait state control
12	Data wait state control
13	IO wait state control
14..15	IO wait state code

TABLE 4: Memory Mapped Registers

NAME	ADDRESS	DESCRIPTION
MEMWSG	0	Memory Wait State
PPWSC	1	PIOREG page pointer (8-0) and Wait State Control
TIM	2	Timer
PRD	3	Period
IMR	4	Interrupt mask (5-0)
GREG	5	Global memory (7-0)

TABLE 5: IMR Definition

BIT	NAME	DESCRIPTION
0	INT0	External Interrupt 0
1	INT1	External Interrupt 1
2	INT2	External Interrupt 2
3	TINT	Timer Interrupt
4		Unused
5		Unused
15..6		Unused

TABLE 6: Interrupt Vectors

SOURCE	LOCATION	DESCRIPTION
RSB	0000H	Reset
INT0B	0002H	External Interrupt 0
INT1B	0004H	External Interrupt 1
INT2B	0006H	External Interrupt 2
TINT	0018H	Timer
TRAP	001EH	Software

WAIT STATE GENERATION (continued)

Table 4 describes the memory mapped special function registers located in data memory page zero. Register MEMWSG is located in the first word of page 0 while PPWSC is located in the second word.

Wait states may be automatically inserted for IO space accesses as well. IO wait states are programmed in the wait state control register PPWSC. The definition of the PPWSC register is found in Table 3. Program, data, and IO spaces each have a control bit which when "0" translates the two-bit wait state code into zero, one, two, or three wait states. When the wait control bit is a "1", then the translation of the two-bit wait state code is zero, one, three, or seven. When the device is reset, the default wait state timing for all spaces is preset for seven.

INTERRUPTS

Interrupts can be selectively enabled by writing a "1" or disabled by writing a "0" to the corresponding IMR register bit. Enabled interrupts are serviced by jumping to interrupt vectors in program memory. Table 5 shows the definition of the IMR register and Table 6 identifies the interrupt service vectors.

PERIPHERAL IO

The peripheral IO block consists of peripheral IO functions and registers. The registers are accessible by the DSP core in data memory with zero wait states. The data page of the peripheral IO registers is programmable in the peripheral IO page bits in the PPWSC register. The peripheral page may be programmed to overlay internal or external data memory. When overlaying internal data memory, the peripheral registers are accessible without intermediate data pointer loads and internal memory will not be affected by PIOREG writes. When overlaying external data memory, a write to PIOREG will overwrite both the PIOREG and the external memory. Internal data RAM, undisturbed by register accesses, may be recovered by programming the peripheral page to another location.

Each PIOREG register is 16 bits wide and the DSP communicates through the peripheral IO registers with the programmable digital functions such as A/D, D/As, spindle speed and phase counters, pulse density PWM-type DAC, and mode or control bits. See Figure 1 for PIOREG MAP definitions.

Data Acquisition

The A/D can be programmed to operate in different conversion modes which differ in the method of starting the A/D conversion, the number of conversions performed, and the input source. Table 7 lists these A/D conversion modes and the timing diagrams of Figure 13 and Figure 14 show two typical modes of operation. The method of starting the conversions is programmable and includes both external and DSP triggering. In a typical application, five conversions are performed corresponding to four position bursts from a quadrature servo demodulator and a fifth representing VCM motor current. Conversion status is indicated by use of the ADCBUSY and ADC(3:0) DONE status bits which are polled to monitor conversion progress and which registers have been updated. The result registers hold the left justified 10-bit result of 2's complement A/D conversions.

Data Conversion

Two 1 µs, 2's complement, 10-bit D/As identified as DAC1 and DAC2 are written left justified in the PIOREG register. Depending on the mode of operation selected, the DACs can be configured for independent writes, cascaded 16-bit DAC or FIFO pipelining of input data words. When configured as 16-bit cascaded DAC, the conversion of PIOREG 6 is as follows: bit 15 is the sign bit for both DACs, bits 14..6 are sent to DAC1, bits 5..0 are sent to DAC2 (corresponding to bits 8..3 of DAC2), and bits 2..0 of DAC2 are set to "100".

For spindle motor current control, a 12-bit pulse density DAC provides a PWM-type output through a 50 kΩ resistor to the VI pin of the spindle control circuit. A single capacitor to ground from the VI pin will provide adequate filtering. The SPDAC output is pulse density because it utilizes a technique illustrated in the timing diagram of Figure 2. Pulse density modulation redistributes the output signal's energy spectrum upward in frequency when compared to traditional PWM methods. With this technique, modulation ripple is significantly reduced.

Spindle Speed and Phase Counters

Spindle speed and phase control is implemented using three dedicated counters. Three counters provide sufficient resources to robustly implement synchronized spindle applications in both MASTER and SLAVE modes. Figure 3 shows these speed and phase counters. Counter 1 is dedicated to measuring the period of the local spindle. The spindle mode bits can be programmed so that the measurement periodcan be based on the commutation of the spindle motor itself or from an external source through the

TABLE 7: A/D Conversion Modes

MODE	ADC MODE CONTROL BIT VALUES			OPERATION
Normal	0	0	0	The START signal is asserted and each STROBE will convert ADC0-3 in sequence. After START is de-asserted, SOUT will be converted. There may be up to four STROBE signals during the START interval depending upon the number of bursts utilized. SOUT is converted on the fall of START after any active conversion is complete.
Normal-auto	0	0	1	After the assertion of START, a single STROBE signal will initiate the sequential conversion of ADC0-3 and SOUT. The conversions will complete at the rate of PCLK/13 in accordance with the PCLK clock being used. SOUT is converted after the de-assertion of start and any active conversion is complete.
Direct ADC0	0	1	0	This mode allows direct external control of the servo ADC to convert input ADC0 for use with external sample and hold and MUX circuits. The input is converted upon assertion of the STROBE signal.
Direct ADC4	0	1	1	This mode allows direct external control of the servo ADC to convert input ADC4 via the STROBE signal. For use with external level conditioning and sampling circuits.
External Calibration	1	0	0	The inputs ADC4, ADC5, SOUT, and VREF are converted when DSP sets the ADC START bit.
Manual Conversion	1	0	1	The inputs ADC0-3, and SOUT are converted under DSP control by asserting the ADC START bit.
SOUT Conversion	1	1	0	The DSP can initiate a conversion of SOUT by asserting ADC START bit.
Internal Calibration	1	1	1	The DSP initiates a sequence of conversions by setting ADC START. The outputs of DAC1, DAC2, VREF, and SOUT are converted and loaded into PIOREG.

Address-NAME	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0 SERVO CONTROL	FIFO MODE	DAC WRITE MODE	ADC3 DONE	ADC2 DONE	ADC1 DONE	ADC0 DONE	ADC MODE 3	ADC MODE 2	ADC MODE 1	MARGIN	DAC1 VREF	RE-TRACT	SAT	VCM ENABLE	ADC START	ADC BUSY
1 ADC0/4 (READ)	BIT 9	ADC0/ADC4/DAC1								BIT 0						
1 SP PARAM (WRITE)					VHYST3	VHYST2	VHYST1	VHYST0	ISLEW3	ISLEW2	ISLEW1	ISLEW0	IPH3	IPH2	IPH1	IPH0
2 ADC1/5	BIT 9	ADC1/ADC5/DAC2								BIT 0						
3 ADC2/ VREF	BIT 9	ADC2/VREF								BIT 0						
4 ADC3	BIT 9	ADC3								BIT 0						
5 SOUT	BIT 9	SOUT								BIT 0						
6 DAC1	BIT 9 SIGN	DAC1								BIT 0	Refer to bit definitions in data conversion section					
7 DAC2	BIT 9 SIGN	DAC2								BIT 0						
8 CLOCK CONTROL							SLEEP 1	SLEEP 0	SLEEP 0	PCLK DIV 3	PCLK DIV 2	PCLK DIV 1	PCLK DIV 0	CNTR3 FLAG	CNTR2 FLAG	CNTR2 FLAG
9 TEST	BIT 15	TEST WORD (READ BACK IS ALWAYS 0)														
A SPIN. CONTROL	SPMUX MODE1	SPMUX MODE0	SPCNTR MODE1	SPCNTR MODE0	SPDIV MODE3	SPDIV MODE2	SPDIV MODE1	SPDIV MODE0	SPCLK SEL3	SPCLK SEL2	SPCLK SEL1	SP RESET	ENABLE	DIS PWR	GAIN	AD-VANCE
B SPDAC	0	BIT 11 MSB	SPINDLE DAC										BIT 0 LSB			
C SPIN. COUNT1	0	BIT 14	SPINDLE COUNTER 1													BIT 0
D SPIN. COUNT2	0	BIT 14	SPINDLE COUNTER 2													BIT 0
E SPIN. COUNT3	BIT 15 SIGN	SPINDLE COUNTER 3														BIT 0
F SPCNT3 PRESET	BIT 15 SIGN	SPINDLE COUNTER 3 PRE-LOAD														BIT 0

FIGURE 1: Peripheral I/O Register Map - PIOREG

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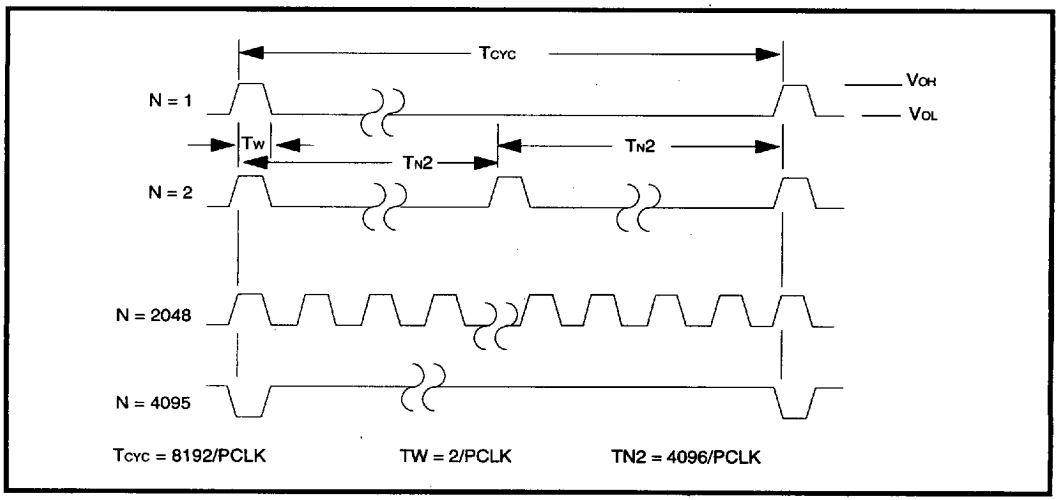

FIGURE 2: Spindle Pulse-Density PWM Timing Diagram (Internal signal, for reference only)

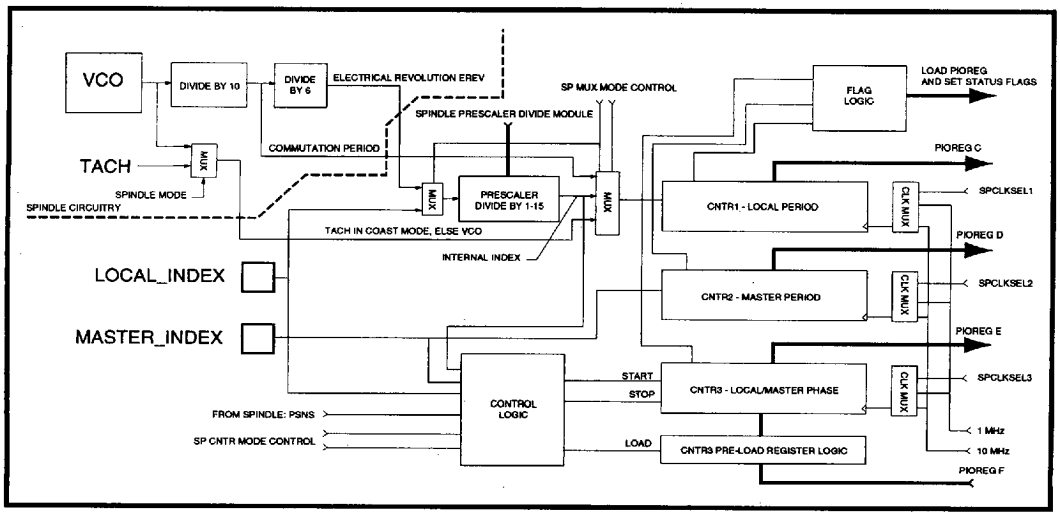

FIGURE 3: Spindle Counter Functional Blocks

Spindle Speed and Phase Counters (continued)

LOCAL pin. Programmable counters are included which can divide the measurement source down in frequency. Typically, the counters are programmed to account for the number of motor poles so that the period measurement is exactly one revolution. When the period measurement is complete, the count will be saved in the PIOREG and signal the DSP by setting the associated flag bit.

Synchronized spindle operation is supported with counters 2 and 3. Counter 2 is intended to measure the period of the master spindle through the MASTER pin. Counter 3 is a relative phase counter which is started by the master and stopped by the local spindle. Phase can be determined by reading counter 3. To assist measuring phase for all angles, counter 3 may be preloaded with a number such that a 2's complement value centered at zero corresponds to the desired phase.

Each spindle counter can be configured to count at a rate of 1 MHz or 10 MHz depending on the resolution required and the expected period to be measured. Counters 1 and 2 are up-counters which start at zero and count to 7FFFH where they saturate. Counter 3 is a presetable down counter (2's complement) ranging from 7FFFH to 8000H where it saturates.

Spindle Startup

Spindle motor startup is readily implemented by the DSP. The DSP asserts the ADVANCE bit in the spindle control register which in turn advances the commutation counter 1/10th of a commutation. The role of the DSP during startup is to provide an increasing frequency of ADVANCE pulses which will accelerate the motor. Once the motor has reached sufficient speed, the DSP enables normal mode. Once in normal mode, all further commutation is handled entirely by the spindle predriver block.

Capability for closed-loop, position sense and go, starting is provided in the spindle drivers and spindle timers. Refer to applications notes for details.

Time Base Prescaler

A Time Base prescaler is provided for the generation of internal clock signals. The signal X2 is generated by a PLL and is 6 times the frequency of the crystal or external clock referenced at X1, and is used to generate the DSP core clocks. A DSP cycle uses four X2 cycles. Outputs CLK1 and CLK2 are derived from X2 and are used for DSP interface timing. The clock for the peripheral circuits is referred to as PCLK and is generated from X2 divided by the value of bits PCLK (3-0) in the PIOREG register. In general, the peripherals require a clock rate of 10 MHz to 12.5 MHz (maximum), which is set by dividing X2 by the appropriate value. The PCLK register is preset to divide X2 by 6 on reset. The timing signals for the spindle counters are X2 divided by 6, or X2 divided by 60.

ACTUATOR PREDRIVER

Figure 4 details the actuator predriver, spindle predriver, and voltage reference and power fault blocks. The actuator block consists of amplifiers A1 through A4, saturation detector, and cross-over protection. The actuator predriver serves as a transconductance amplifier by driving four external MOSFETs in an H-bridge configuration. It has two modes of operation which are linear and retract. The retract mode is activated by a power supply failure or assertion of the RETRACT pin. Otherwise, the actuator operates in linear or normal mode.

Loop Compensation Amplifier

During linear operation, the acceleration signal is applied through amplifier A1 with three connections all available externally. RC components may be used to provide loop compensation at this stage. The saturation detector monitors amplifier A1 for saturation. Whenever amplifier A1 is in saturation, the current flowing through the summing node at ERRM will be detected and the SAT bit in the peripheral IO status register will be asserted.

MOSFET Drivers

ERR is the output signal of A1 and it drives two precision amplifiers each with a gain of 8.5. The first of these two amplifiers is inverting and it is formed from opamp A3, an on-chip resistor divider, and an off-chip complementary MOSFET pair. The second amplifier is non-inverting and it is formed in a similar manner as opamp A4. Feedback from the MOSFET drains on sense inputs SE1 and SE3 allow the amplifier gains to be established precisely. The voice coil motor and a current sense resistor is connected in series between SE1 and SE3.

ACTUATOR PREDRIVER (continued)

Crossover Protection Blocks

Crossover protection circuitry between the outputs of A3 and A4 and the external MOSFETs ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also apply a constant voltage across the motor to retract the heads at a constant velocity.

Current Sense Amplifier

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 is fixed gain with internal resistors) through inputs SE1 and SE2. SOUT is referenced to VREF.

Retract Function

The 6840 incorporates a dual level retract scheme. When retract is initiated, a fixed voltage (level 1) is applied across the actuator to force a constant retract velocity. After an externally adjustable amount of time, a higher voltage (level 2) is briefly applied to the actuator. At the end of level 2, the actuator is floated (i.e., zero current).

The timing and amplitude of the level 2 phase can be adjusted with external components. RRTR, CRTR, and an internal discharge resistor which is activated during level 2 control the retract timing. When $\overline{\text{RETRACT}}$ is first lowered, RRTR discharges CRTR until the RETRD pin reaches the level 2 trigger threshold (nominally 0.85V). At this time, the level 2 tract amplitude is applied to the actuator and the internal discharge resistor (nominally 32 kΩ) quickly discharges CRTR. When CRTR has been discharged to half of the trigger voltage, all retract current is turned off and the actuator is floated. The level 1 retract amplitude is internally fixed (0.85V nominal). During level 2, SE1R is fed back to the retract amplifier instead of SE1. Thus the level 2 amplitude will be increased by the factor $(1 + R_{R1}/R_{R2})$.

A second external RC delay is used between $\overline{\text{RETRACT}}$ and $\overline{\text{BRAKE}}$ to program the brake delay and ensure the actuator has enough time to retract before the spindle is braked.

SPINDLE PREDRIVER

Figure 4 provides a detailed block diagram of the spindle predriver block. The spindle block includes spindle motor current shaping, a phase error circuit and phase locked loop, MOSFET predrivers, and a delayed spindle brake circuit. The current shaping circuit employs Silicon Systems' SilentSpin™ technology which shapes the spindle motor current to minimize acoustic noise.

SilentSpin™ Waveform Generator

The SilentSpin™ wave generator drives the spindle motor windings with properly phased current waveforms. In run mode, the generator is clocked by the VCO output. During start mode, the generator is clocked by the ADVANCE bit in the spindle control register.

The analog signal at pin VI controls the peak amplitude of the current waveform. With the spindle control register bit GAIN programmed as "0", the peak current occurring when the voltage at VI is equal to VREFOUT corresponds to 294 mV dropped across each sense resistor. Programming GAIN to "1" configures the peak current to correspond to 79 mV across each sense resistor.

Phase Error Circuit and PLL

The phase error circuit determines the phase error between the current and voltage in each winding. Depending on the result of the comparison and the phase of the commutator, a positive or negative pump current is applied to the RC pin.

The magnitude of the pump current at RC is the sum of a constant current (IPH) and a current proportional to the VCO frequency. The constant current value for IPH is set by the value of the bits IPH(3:0) in the PIOREG word 1. (see PIOREG definition.) The default value is 8h (10 μA), otherwise IPH = 1.25 μA • N, for N = 0 to 15. The proportional current is set by RVCO, the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on VCO is nominally 2.0 volts. When the VCO is reset, the VCO output is forced low. The first VCO clock will occur immediately after the VCO exits reset.

MOSFET Predrivers

The N and P outputs drive the gates of the external N and P channel power MOSFETs. Except during brake, both the N and P drivers are switched with PWM. During brake, the N channel MOSFETs are turned on and the P channel MOSFETs are turned off. To minimize electrical switching noise, the charge and discharge currents at N and P can be adjusted with the ISLEW DAC. The output current is 100 times the value of ISLEW (ISLEW = 6.8 μA • (N+1)).

Delayed Spindle Brake

Brake mode is invoked whenever the $\overline{\text{BRAKE}}$ pin or the BRAKE bit in the spindle mode register is asserted. A delayed spindle brake resulting from power failure is implemented with and external resistor and capacitor. The brake resistor tied between $\overline{\text{BRAKE}}$ and $\overline{\text{SYSRST}}$. The brake delay capacitor is connected from $\overline{\text{BRAKE}}$ to ground. The time constant of the two discrete components determines the delay from system reset assertion to dynamic braking.

A second capacitor is required to provide the voltage necessary to assert the brake condition during power failure. This capacitor is connected at the CBRAKE pin to ground.

Voltage Reference and Fault

The voltage reference circuit generates VRETRACT, VIDLE, and several other internal voltage and current references. It also generates an precise 1.200 volt reference at pin VBG for use with the fault detection comparators. VBG is internally multiplied by 1.875 and output as VREFOUT.

The voltage fault detector contains sensing for under-voltage on the twelve volt supply through the V12CHK pin and on the five volt supply with the VCCHKL pin. An internal resistor divider monitoring the five volt supply is available at the VCCTH pin. If VCCTH is the correct voltage and tolerance, it can be connected directly to VCCHKL; otherwise, an external resistor divider can be used with VCCHKL.

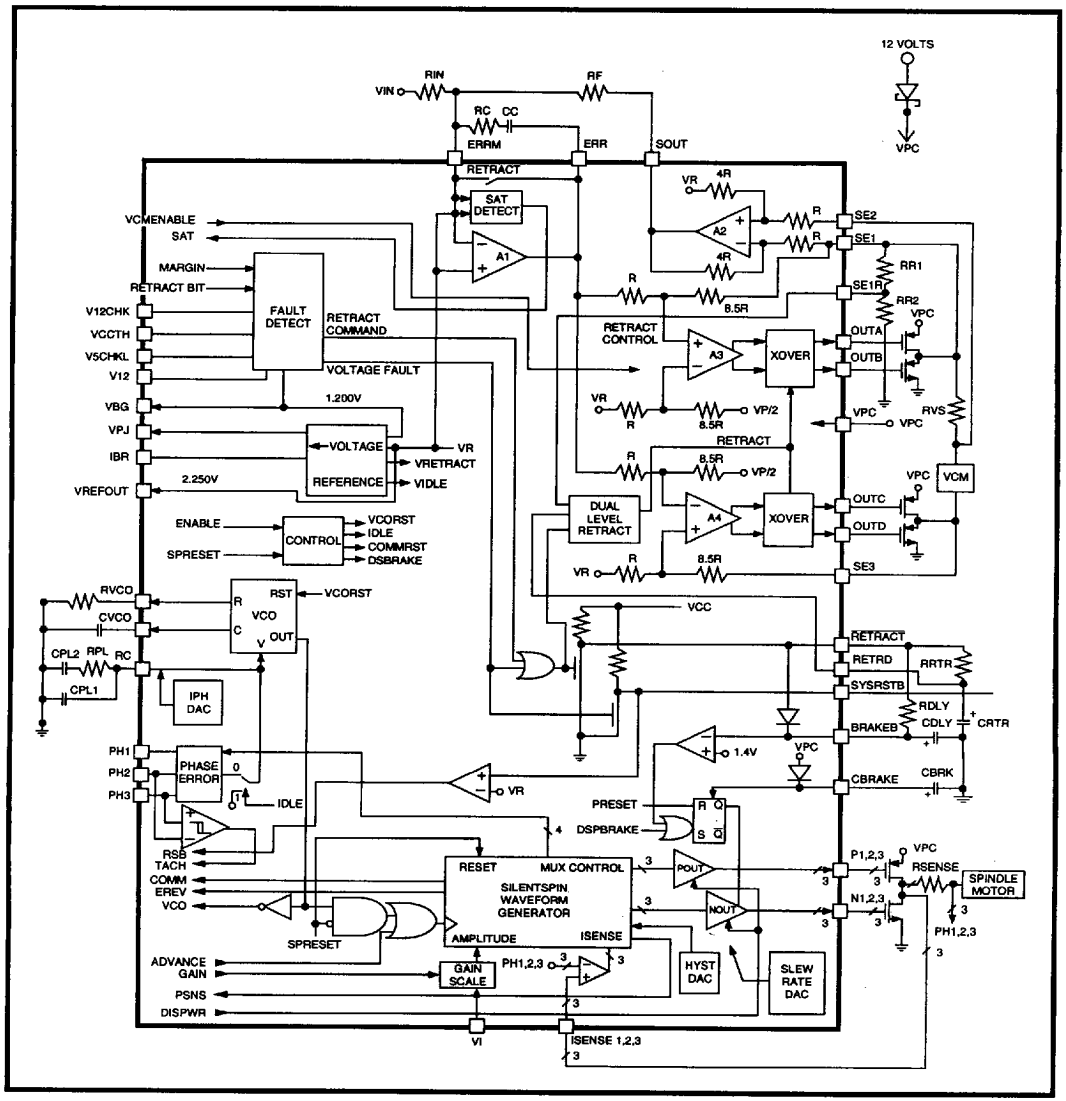

FIGURE 4: Spindle and Positioner Circuitry

PIN DESCRIPTION

Note abbreviations: C = Component, AI = Analog Input, I = Digital Input, AO = Analog Output, O = Digital Output, Z = Tri-State Output, OC = Open Collector Output.

SUPPLIES

NAME	TYPE	DESCRIPTION
VNA, VND	GROUND	Analog and Digital grounds. These pins are internally connected.
VDD	POWER	Digital +5V supply
VPO	POWER	+5V supply for internal crystal oscillator
VNO	GROUND	Internal crystal oscillator ground
VPC	POWER	The +12V supply. Diode protected from system +12V. This is also the bridge supply for the spindle and actuator FETs.

DSP CORE

D(15:0)	I/O/Z	Data input/output pins. Pin is high impedance state in hold mode.
READY	I	Data ready input, allows cycle extension for external devices if the internal wait-state generator is not utilized. Ready is sampled when $\overline{DS}$, $\overline{IS}$, or $\overline{PS}$ go low, if READY is high, the internal wait-state is used, if low, the external wait-state generator is used.
$\overline{HOLD}$	I	When this input is asserted, the DSP core places all its control lines and buses in a high impedance state.
$\overline{BIO}$	I	Branch control input. If low, the DSP core will branch on a BIOZ instruction.
$\overline{INT}$(2:0)	I	Three external user interrupts. $\overline{INT0}$ must be used as servo interrupt when DAC FIFO mode is being used.
A(15:0)	O/Z	Address bus outputs. Pin is high impedance state in hold mode.
$\overline{DS}$	O/Z	Data memory select signal. Pin is in high impedance state in hold mode.
$\overline{PS}$	O/Z	Program memory select signal. Pin is in high impedance state in hold mode.
$\overline{IS}$	O/Z	Input/Output select signal.Pin is in high impedance state in hold mode.
R/$\overline{W}$	O/Z	Read/Write signal for communication with external devices. Pin is high impedance state in hold mode.
$\overline{STRB}$	O/Z	Strobe signal for external bus cycles. Pin is in high impedance state in hold mode.
$\overline{HOLDA}$	O	Hold Acknowledge signal, asserted when in hold mode
$\overline{IACK}$	O	Interrupt acknowledge signal. Asserted when CLKOUT1 is low, and the program is branching to address on A(15:0).
XF	O	External flag
CLKOUT1	O	Instruction cycle phase indicator. Rises at start of Q3, falls at start of Q1.
CLKOUT2	O	Instruction cycle phase indicator. Rises at start of Q2, falls at start of Q4.
XO	AO	Output pin of the internal crystal oscillator. Leave unconnected if oscillator function is not used.

DSP CORE (continued)

NAME	TYPE	DESCRIPTION
XI	AI	Input pin for externally supplied clock, or connection to crystal for internal oscillator
SERIALTEST	O	Serial test port. DSP writes to special PIOREG location will result in contents shifted out on this pin.
DACUPDATE	I	Outputs data from DACFIFO to the DACs when DAC FIFO mode is selected
TDI	I	Emulator serial input port
TDO	O	Emulator serial output port
TCK	I	Emulator serial port clock
TMS	I	Emulator serial port mode select
LOCALINDEX	I	Signal from local spindle indicating rate of revolution
MASTERINDEX	I	Signal from (remote) master spindle in synchronized spindle applications

DATA CONVERSION

DAC1	AO	Output of DAC1
DAC2	AO	Output of DAC2
DAC1VREF	AI	Provides reference voltage to DAC1 if appropriate mode is selected.
ADC(5:0)	AI	Inputs to ADC multiplexer
MUXOUT	AO	Output of the first level multiplexer which selects ADC(3:0)
AMPINN	AI	Level and gain conditioning amplifier negative input
AMPINP	AI	Level and gain conditioning amplifier positive input
AMPOUT	AO	Level and gain conditioning amplifier output signal
START	I	This pin causes a sequence of A/D conversions in conjunction with STROBE
STROBE	I	Initiates a conversion by the ADC per the defined operating mode

ACTUATOR

NAME	TYPE	DESCRIPTION
ERR	AO	POSITION ERROR - The loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge as follows: SE3 - SE1 = 17 • (ERR - VREFOUT)
ERRM	AI	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier
SOUT	AO	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external sense resistor, as follows: SOUT - VREFOUT = 4 • (SE2 - SE1)
SAT	O	SATURATION DETECT - Monitors the error amplifier and is high when the amplifier has saturated (ERR is no longer proportional to the VCM voltage).
SE2	AI	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the actuator. The inverting input of the differential amplifier is connected internally to SE1.
SE1	AI	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier and to the current sense amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point from ERR is: SE1 - VREFOUT = -8.5 • (ERR - VERFOUT)
SE3	AI	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point from ERR is: SE3 - VREFOUT = 8.5 • (ERR - VREFOUT)
SE1R	AI	Alternate SE1 connection to the retract amplifier. This input is selected during the "pulse" phase of retract. An external resistor divider connected to this pin programs the retract amplitude during the "pulse" phase.
$\overline{\text{RETRACT}}$	OC	A retract command from the DSP or a voltage fault will cause this pin to go low, initiating a retract. This pin is open drain with internal pull-up resistor and may be activated internally.
RETRD	AI	A resistor from pin $\overline{\text{RETRACT}}$ and a capacitor to GND will set the timing for the dual-level retract operation. When the voltage on this pin falls below the trigger level, the "pulse" phase of the retract occurs (an internal pull-down resistor is activated also). When the voltage falls to 50% of the trigger value, the "pulse" phase is terminated.
OUTA OUTC	AO	P-FET DRIVE - Drive signal for a P-channel MOSFET connected between one side of the motor and VPC
OUTB OUTD	AO	N-FET DRIVE - Drive signal for an N-channel MOSFET connected between one side of the motor and GND. Crossover protection circuitry ensures that the P and N channel devices connected to the same side of the motor are never enabled simultaneously.

PIN DESCRIPTION (continued)

SPINDLE

NAME	TYPE	DESCRIPTION
P1, P2, P3	AO	P-CHANNEL SPINDLE DRIVERS - These pins are connected to the gates of three P channel power MOSFETs in the spindle motor power bridge.
N1, N2, N3	AO	N-CHANNEL SPINDLE DRIVERS - These pins are connected to the gates of three N channel power MOSFETs in the spindle motor power bridge.
VI	AO, C	SPINDLE CURRENT CONTROL VOLTAGE - Determines the peak amplitude of the spindle motor drive currents. External capacitor at this pin forms low-pass filter.
ISENSE1 ISENSE2 ISENSE3	AI	SPINDLE CURRENT SENSE - Connects to the spindle current sense resistors. The motor current in each winding is calculated by subtracting that winding's PH from its ISENSE.
RVCO	C	VCO RESISTOR - Sets the speed range of the VCO. The voltage at RVCO is forced to track RC.
CVCO	C	VCO CAPACITOR - Sets the speed range of VCO.
RC	C	PLL LOOP FILTER - Sets the time constant for the PLL in run mode. In all other modes, it is connected to a DC voltage, VIDLE. VIDLE determines the VCO frequency at which crossover from startup to run should occur (by setting the ENABLE bit).
PH1 PH2 PH3	AI	SPINDLE MOTOR TERMINALS - These pins are used to calculate the phase error in the PLL. They are also used, in conjunction with ISENSE1,2,3 to calculate winding current.

VOLTAGE REFERENCE AND FAULT DETECT

NAME	TYPE	DESCRIPTION
V12	AI	The 12V supply reference to the 12V fault detector.
V12CHK	AI	12V RESET COMPARATOR INPUT - The input to the 12V reset comparator and the connection to an optional external bypass capacitor. V12 is divided down at this pin by an on-chip resistor divider and then compared to VBG. If V12CHK falls below VBG, a forced retract occurs.
V5CHKL	AI	The 5V low voltage detect pin. May be connected to a bypass capacitor. When this pin falls below VBG, $\overline{\text{SYSRST}}$ is active and retract is initiated.
VCCTH	AI	The 5V divider output. Normally left open. The VCC low voltage check level can be modified by biasing this pin with an external resistor divider.
IBR	C	BIAS RESISTOR - This resistor sets the internal bias currents of the analog circuitry.
$\overline{\text{SYSRST}}$	OC	SYSTEM RESET - Active low, this open-collector output is asserted when a low condition is detected on either 5V or 12V. Provides reset signal to internal logic, including $\overline{\text{RS}}$ signal in DSP.
$\overline{\text{BRAKE}}$	AI	BRAKE - Active low, this input is pulled low by an external RC to perform a delayed brake. Note that when $\overline{\text{BRAKE}}$ is asserted, it sets a latch that is cleared in the Preset mode.
CBRAKE	C	BRAKE CAPACITOR - A storage capacitor is connected to CBRAKE to supply the charge necessary to turn on the NMOS device during brake.
VREFOUT	AO	VREFOUT is equal to 1.875 • VBG and represents the reference potential for the actuator, data converters, and spindle analog circuits.
VBG	AO	Output voltage of the band-gap voltage reference generator.
VPJ	AO, C	Internally generated 5V power supply for spindle and positioner logic and analog circuits. VPJ will hold its value as long as VPC maintains due to back-EMF from the spindle motor. Attach bypass capacitor as required.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
V12, VPC	0 to 14V
VPA, VCC	0 to 7V
SE1, SE2, SE3, N1, N2, N3, $\overline{\text{BRAKE}}$, CBRAKE	0 to 15V
PH1, PH2, PH3, ISENSE1, ISENSE2, ISENSE3	-2 to 15V
$\overline{\text{SYSRST}}$, RETRD, $\overline{\text{RETRACT}}$	0 to VCC
All other pins	0 to VCC
Storage Temperature	-45 to 165°C
Soldering Temperature, 10 seconds duration	260°C

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, the following conditions are valid through this document.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
V12	Normal Mode	9	12	13.2	V
	Retract Mode	3.5		14.0	V
VPC	Normal Mode	9	V12-V_D	14	V
	Retract Mode (back-emf)	3.5		14	V
VPA, VCC		4.5	5.0	5.5	V
VBG bypass capacitor			0.1		µF
VPJ bypass capacitor			0.1		µF
VREFOUT bypass capacitor			0.1		µF
IBR Resistor		11.8	12.0	12.2	kΩ
RVCO Resistor		24	25	26	kΩ
Operating Temperature		0		70	°C

DC CHARACTERISTICS

VPC Current	Normal Operation			35	mA
VCC Current	Normal Operation			100	mA
VPA Current	Normal Mode			15	mA

A1, LOOP COMPENSATION AMPLIFIER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Bias Current	Pin ERRM	-100		100	nA
Input Offset Voltage	w.r.t. VREFOUT	-10		10	mV
Voltage Swing V_{OL} V_{OH}, wrt VREFOUT	R_L = 10 kΩ to VREFOUT	 1		-1	 V V
Load Capacitance	Maximum Load			100	pF
Gain		60			dB
Unity Gain Bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB
Retract Switch Resistance	Retract Mode, VPC > 9V			1	kΩ
SAT threshold (IERR-VREFOUTI)		0.8	0.9	1.0	V
Hysteresis			40		mV

A2, CURRENT SENSE AMPLIFIER

Input Impedance, Resistive	SE2 = VREFOUT	2.6	4.3	100	kΩ
	SE1 = VREFOUT	3.2	5.4		kΩ
Input Offset Voltage	SE1 = SE2 = VREFOUT			20	mV
Output Voltage Swing V_{OL}	R_L = 20 kΩ to VREFOUT			-1	V
V_{OH}	wrt VREFOUT	1			V
Common Mode Range V_{OL}		 -0.2			 V
V_{OH}				V12+0.2	V
Load Capacitance	Maximum Load			100	pF
Load Resistance	to VREFOUT	20			kΩ
Output Impedance				20	Ω
Gain (SOUT-VREFOUT)/(SE1-SE2)		3.9	4.0	4.1	V/V
Unity Gain Bandwidth		0.5			MHz
CMRR		52			dB
PSRR		60			dB

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ELECTRICAL SPECIFICATIONS (continued)

ACTUATOR MOSFET DRIVERS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SE3 Input Impedance	to VREFOUT	10	25		kΩ
OUTA, OUTC voltage swing	IIOUTI<1 mA	1.5		VP-1	V
OUTB, OUTD voltage swing	IIOUTI<1 mA	1		VP-1.5	V
VTH, crossover separation threshold				1.6	V
Slew Rate, OUTA...D	CL ≤ 1000 pF	0.5			V/µs
Crossover Time	±300 mV step at ERR CL ≤ 1000 pF			4	µs
Output impedance, OUTA...D			20		kΩ
Transconductance I(OUTA...D)/(ERR-VREFOUT)			8		mA/V
Gain - (SE1-VREFOUT)/(ERR-VREFOUT) or (SE3-VREFOUT)/(ERR-VREFOUT)		8	8.5	9	V/V
Retract Motor Voltage	VP.5V	0.7	0.82	1.0	V

VCO

Unless otherwise specified, C_{VCO} = 1.0 µF, R_{VCO} = 25 kΩ

Typical Frequency		$F_{VCO} = V_{RC}/(4 \cdot R_{VCO}C_{VCO})$			Hz
Run Frequency	RC = 2.0V	17.5	19.75	22.0	kHz
Idle Frequency	Mode = Reset	700	1100	1500	Hz
Reset Phase Error	RC = V_{IDLE}			18	°

RETRACT CIRCUITS

Retract Voltage	VP>5V, level 1	0.7	0.82	1.0	V
RETRD Discharge Resistor	VP>5V, level 2	22	32	42	kΩ
RETRD Trigger Voltages VT1: level 1 to level 2 VT2: level 2 to float (% of VT1)	 VP>5V, level 1 VP>5V, level 2	 0.75 45	 0.85 50	 0.95 55	 V %
$\overline{\text{RETRACT}}$ Output Level V_{OL}	I_{SINK} = 8 mA			0.4	V
$\overline{\text{RETRACT}}$ Output Voltage V_{OH}	I_{SOURCE} = 0.1 mA	VCC-2.0			V
$\overline{\text{RETRACT}}$ Input Threshold V_{IL}		0.8			V
$\overline{\text{RETRACT}}$ Input Threshold V_{IH}				2.0	V
RETRD Input Bias Current	level 1			100	nA
SE1R Input Bias Current				100	nA

PHASE ERROR AMPLIFIER
Unless otherwise specified, RVCO = 25 kΩ, IPH = 0

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
V_{RC} (V_{IDLE})	Mode = Reset		100		mV
Pump Current at RC					
Start Mode	$V_{RC} = V_{IDLE}$		7		µA
Run Mode, at speed	V_{RC} = 2V		82		µA
Source/Sink Current Mismatch	V_{RC} = 2V			5	%
PH1 Input Offset, State B	PH2 = V12, PH3 = 0	-60		60	mV
PH1 Input Offset, State E	PH2 = 0, PH3 = V12	-60		60	mV
PH2 Input Offset, State A	PH1 = V12, PH3 = 0	-60		60	mV
PH2 Input Offset, State D	PH1 = 0, PH3 = V12	-60		60	mV
PH1 Input Offset, State B	PH1 = V12, PH2 = 0	-60		60	mV
PH1 Input Offset, State E	PH1 = 0, PH2 = V12	-60		60	mV

BRAKING CIRCUITS

CBRAKE Input Current - RUN	Run mode, VC_{BRAKE} = VP			2	µA
CBRAKE Input Current - BRAKE	Brake mode, VC_{BRAKE} = 10V			0.2	µA
$\overline{BRAKE}$ Threshold	T_A = 25°C, VP = 4V	1.1	1.25	1.4	V
$\overline{BRAKE}$ VP Threshold	$\overline{BRAKE}$ = 1.5V			3.8	V
$\overline{BRAKE}$ Bias Current				0.1	mA

VOLTAGE FAULT CIRCUIT

VCC Low Trip Point	VCC falling, MARGIN = 0 VCCTH = open	4.26	4.35	4.44	V
VCC Low Hysteresis		30	40	50	mV
VCC Low Trip Point	VCC falling, MARGIN = 0 VCCTH = 0	4.635	4.74	4.843	V
VCC Low Trip Point	VCC falling, MARGIN = 0 VCCTH = VCC	3.49	3.57	3.65	V
VCC Low Trip Change	MARGIN = 0 MARGIN = 1	-10	-14	-16	%
VCCTH Input Range	normal operation	0		2.9	V
VCCTH Input Resistance		90	140	250	kΩ
VREFOUT Fail Threshold	VREFOUT falling	1.4	1.55	1.7	V
VREFOUT Check Hysteresis			85		mV
V12 Low Trip Point	V12 falling	9.2	9.5	9.8	V
V12 Low Hysteresis		60	80	100	mV
V12CHK Impedance			14K		Ω
V5CHKL Bias Current				0.1	µA

ELECTRICAL SPECIFICATIONS (continued)

NMOS MOTOR DRIVER OUTPUTS (N1, N2, N3)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Source Current	V_{OUT} = 4V, ISLEW = 8h		5.8		mA
Sink Current	V_{OUT} = 4V, ISLEW = 8h		5.8		mA
Output High On Resistance				TBD	Ω
Output Low On Resistance				TBD	Ω

PMOS MOTOR DRIVER OUTPUTS (P1, P2, P3)

Source Current	V_{OUT} = VP-4, ISLEW = 8h		5.8		mA
Sink Current	V_{OUT} = VP-4, ISLEW = 8h		5.8		mA
Output High On Resistance				TBD	Ω
Output Low On Resistance				TBD	Ω
V_{OL}	I_{IN} =1 mA		0.4		V
V_{OH}	I_{OUT} =1 mA	VCC-0.4			V

TACH COMPARATOR

SENSOR Rising Edge Threshold	PH3-PH2	60	140	200	mV
SENSOR Falling Edge Threshold	PH2-PH3	60	140	200	mV

ISENSE1,2,3 (WITH RESPECT TO PH1,2,3)

OffsetVP (ISENSE-PH)	PH = VP, HYST = TBD, VI = 0	3	5.2	7.5	mV
Offset0 (ISENSE-PH)	PH = 0, HYST = TBD, VI = 0	-7.5	-5.2	-3	mV
Offset (OffsetVP - Offset0)	HYST = TBD, VI = 0	-2		2	mV
Hysteresis (OffsetVP-Offset0)	HYST = TBD, VI = 0	9		12	mV
V57Degrees (Average of PH=VP and PH=0 measurements)	VI = 2.4V, HIGHI = 1, HYST = TBD	113		138	mV

VBG OUTPUT

Output Voltage	No DC Load		1.20		V
Load Capacitance				0.1	µF

VREFOUT

Output Voltage	No DC Load	2.14	2.25	2.36	V
Output Impedance	$I_{SOURCE} \leq 1.0$ mA $I_{SINK} \leq 1.0$ mA			20	Ω

VPJ

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Voltage	VPC ≥ 6V	4.5	5.0	5.5	V
Bypass Capacitor Value			1		µF

SYSRST

Output Level	V_{OL}	I_{SINK} ≤ 8 mA			0.4	V
Output Voltage	V_{OH}	I_{SOURCE} ≤ 0.1 mA	VCC-2.0			V
Input Threshold	V_{IL}	Input rising	2.10		2.37	V
Input Hysteresis			120			mV

CLOCK TIMING

$\overline{SYNC}$ Hold Time	THS					ns
$\overline{SYNC}$ Setup Time	TSUS					ns
CLKOUT1/CLKOUT2 Cycle Time	TCC		67			ns
CLKOUT1/CLKOUT2 Low Pulse Duration	TWCL		26		36	ns
CLKOUT1/CLKOUT2 High Pulse Duration	TWCH		30		40	ns
CLKOUT1 Edge to CLKOUT2 Edge	TDC1C2		11.66		21.66	ns

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ELECTRICAL SPECIFICATIONS (continued)

MEMORY AND I/O READ AND WRITE TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{STRB}$ from CLKOUT1	TDC1S		15		19	ns
CLKOUT2 to $\overline{STRB}$	TDC2S		0		5	ns
$\overline{STRB}$ Low Pulse Duration	TWSL		32		35	ns
$\overline{STRB}$ High Pulse Duration	TWSH		32		35	ns
Address Setup Time before $\overline{STRB}$ Low	TSUA		8			ns
Address Hold Time after $\overline{STRB}$ High	THA		15			ns
Read Data Access Time from Address	TAA				19	ns
Data Read Setup Time before $\overline{STRB}$ High	TSUDR		15			ns
Data Read Hold Time after $\overline{STRB}$ High	THDR		0			ns
Data Bus Starts Being Driven after $\overline{STRB}$ Low	TEND		0			ns
Data Write Setup Time before $\overline{STRB}$ High	TSUDW		22			ns
Data Write Hold Time from $\overline{STRB}$ High	THDW		12			ns
Data Bus Tri-state after $\overline{STRB}$ High	TDISD		30			ns
READY Hold Time after $\overline{STRB}$ Low	THSLR		16			ns
READY Valid after $\overline{STRB}$ Low	TDSLR				-5	ns

EXTERNAL WAIT-STATE MEMORY AND I/O READ AND WRITE TIMING

READY Hold after CLKOUT2 High	THC2HR		16.66			ns
RREADY Valid after CLKOUT2 High	TDC2HR				-4.34	ns

$\overline{\text{SYSRST}}$ TIMING

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
$\overline{\text{SYSRST}}$ Setup before CLKOUT1 High	TSUIN		TBD		ns
$\overline{\text{SYSRST}}$ Hold after CLKOUT1 High	THIN		TBD		ns
CLKOUT1 Low to Reset State Entered	TDRS		TBD		ns
$\overline{\text{SYSRST}}$ Low Pulse Duration TWRS			TBD		ns

INTERRUPT, $\overline{\text{BIO}}$ AND XF TIMING

$\overline{\text{INT}}/\overline{\text{BIO}}$ Low Pulse Duration TWIN		66			ns
CLKOUT1 to $\overline{\text{IACK}}$ Valid TDIACK		-2			ns
XF Valid before Falling Edge of $\overline{\text{STRB}}$ TDXF		9			
$\overline{\text{INT}}/\overline{\text{BIO}}$ Setup before CLKOUT1 High TSUIN		15			
$\overline{\text{INT}}/\overline{\text{BIO}}$ Hold after CLKOUT1 High THIN		0			

HOLD CONDITION ENTRY TIMING

$\overline{\text{HOLD}}$ valid after CLKOUT2 High TDC2HH				-2	ns
Address tri-state after CLKOUT1 Low TDISC1LA				14	ns
$\overline{\text{HOLDA}}$ low to address tri-state TDISALA				8	ns
$\overline{\text{HOLDA}}$ Low after CLKOUT1 Low TDC1LAL				6	ns

HOLD CONDITION EXIT TIMING

Address Driven before CLKOUT1 Low TENAC1L				15	ns
$\overline{\text{HOLD}}$ Valid after CLKOUT2 High TDC2HH				-2	ns
$\overline{\text{HOLD}}$ High to $\overline{\text{HOLDA}}$ High TDHHAH				15	

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ELECTRICAL SPECIFICATIONS (continued)

ADC CONTROL TIMING

Tpclk is multiples of TCCL and is configured by the value of bits PCLK(3:0)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
STROBE Cycle Time	TSTRBCL		14 • Tpclk			ns
STROBE High Pulse Duration	TSTRBW		2 • Tpclk			ns
START Setup Time before STROBE High	TSTRTSU		0			ns
STROBE High to Valid SOUT	TSTRTSO	Normal mode, Figure 13	13 • Tpclk			ns
START Hold Time after SOUT Strobe	TSTRTH		4 • Tpclk		8 • Tpclk	ns
START Low Pulse Duration	TSTSRTL		16 • Tpclk			ns
ADC Signal Setup Time before STROBE High	TADCSU		0			ns
SOUT Hold Time after SOUT Valid	TSOUTH		4 • Tpclk			ns
ADC Signal Hold Time after STROBE High	TADCH		4 • Tpclk			ns
SOUT Hold Time	TSOUTSU		Tpclk			ns
ADC Valid Signal Cycle Time (auto mode)	TSTRCL		13 • Tpclk			ns
SOUT Setup Time (auto mode)	TSOSU		Tpclk			ns
SOUT Hold Time (auto mode)	TSOH		4 • Tpclk			ns

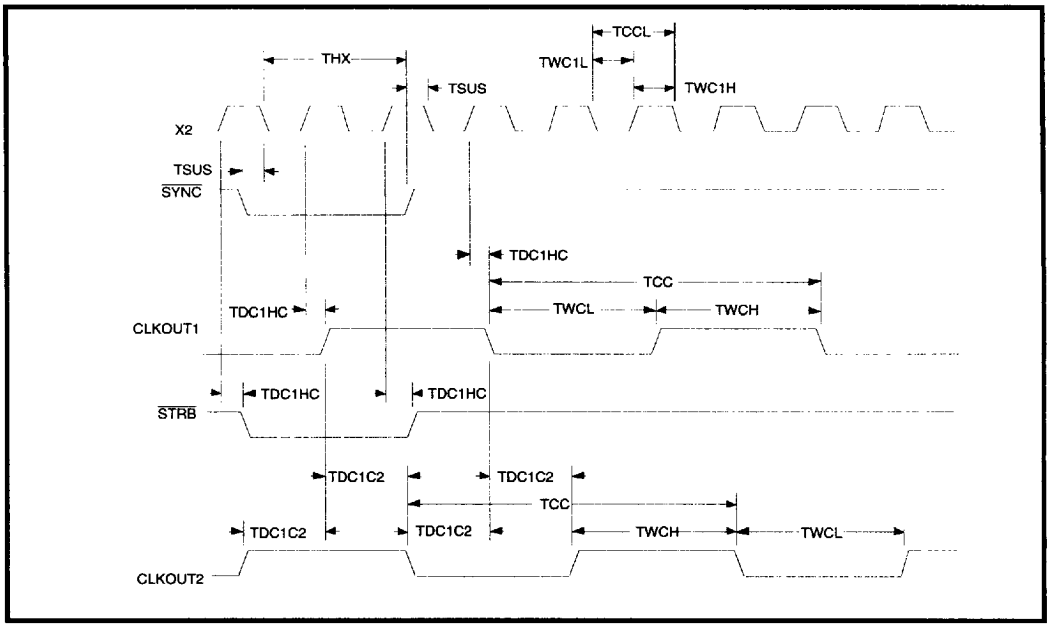

FIGURE 5: Clock Timing Diagram

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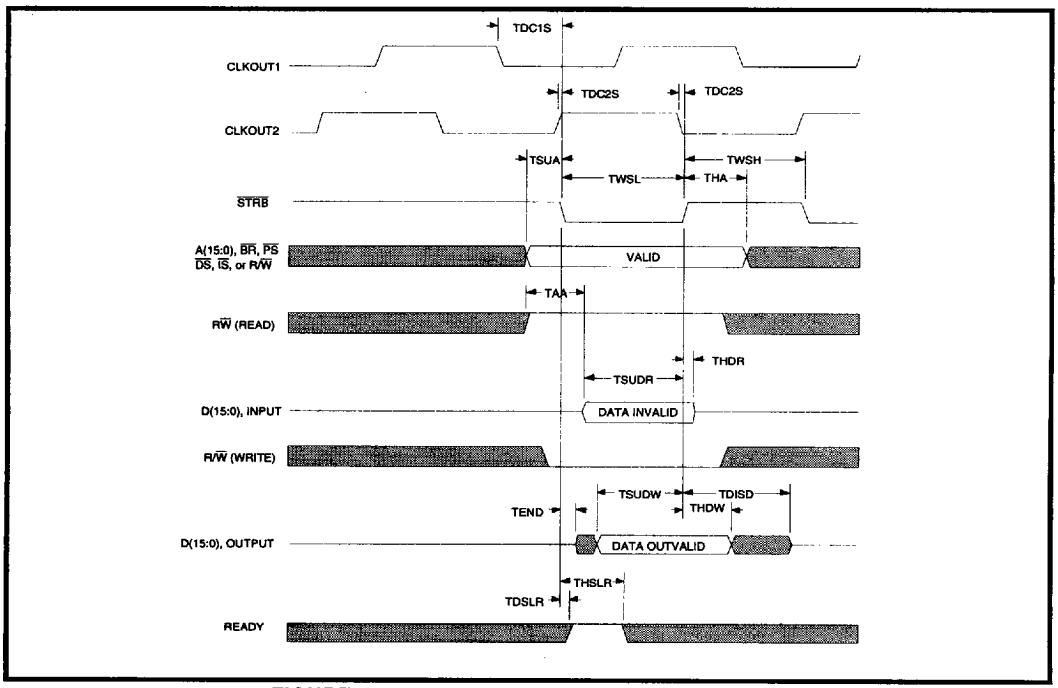

FIGURE 6: Memory and I/O Read and Write Timing

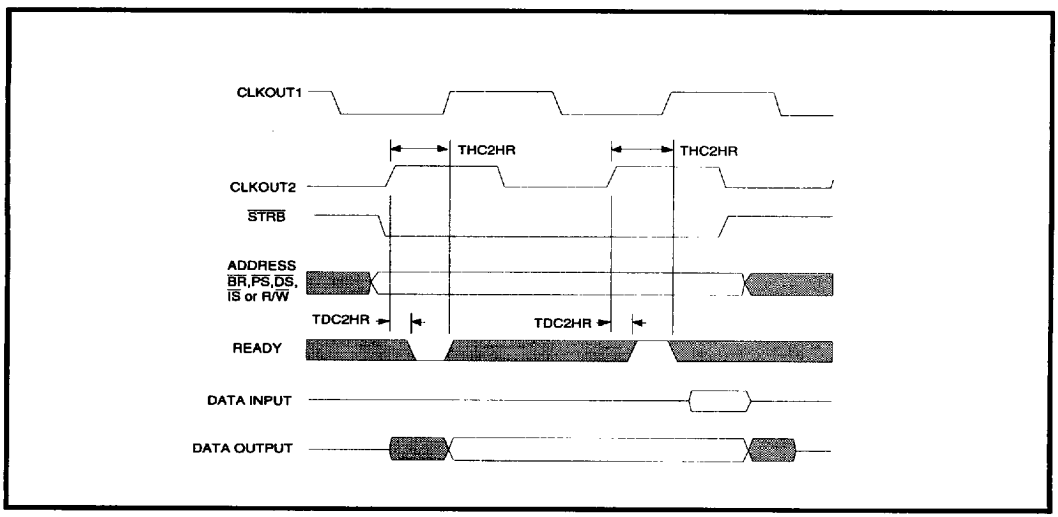

FIGURE 7: One External Wait-State Memory Access Timing

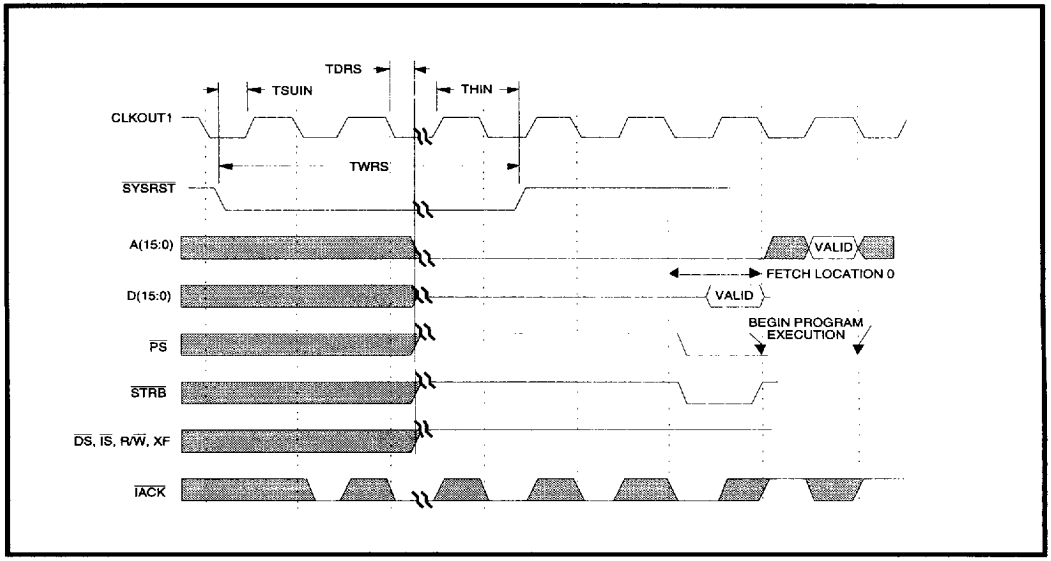

FIGURE 8: Reset Timing

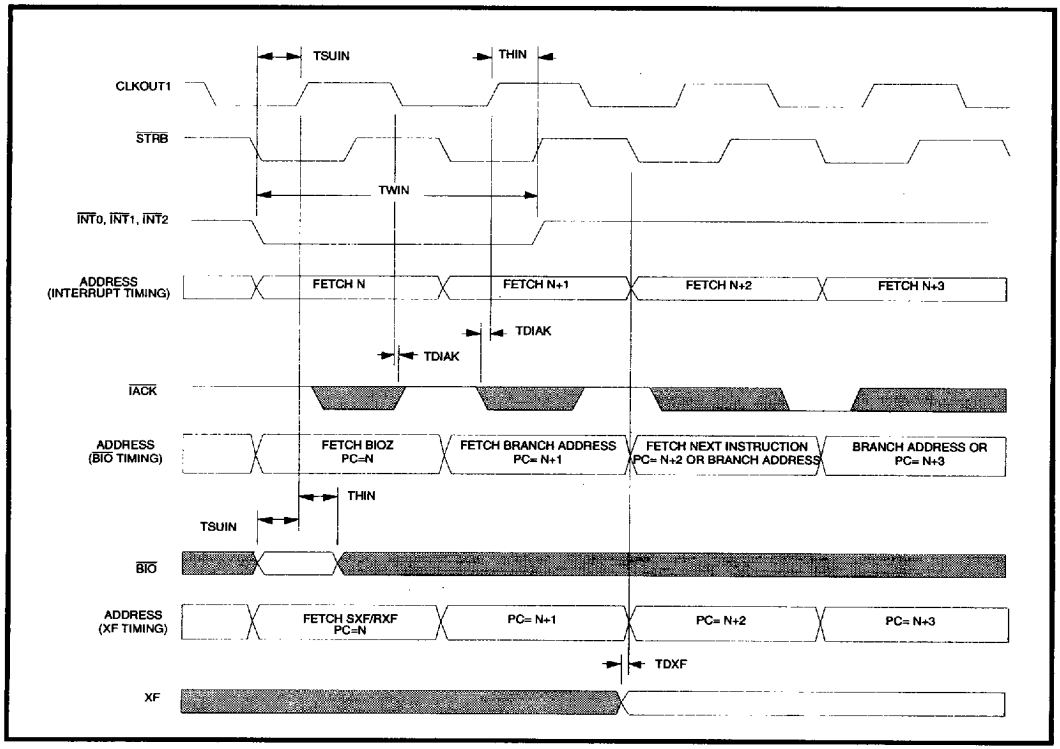

FIGURE 9: Interrupt, $\overline{BIO}$, and XF Timing

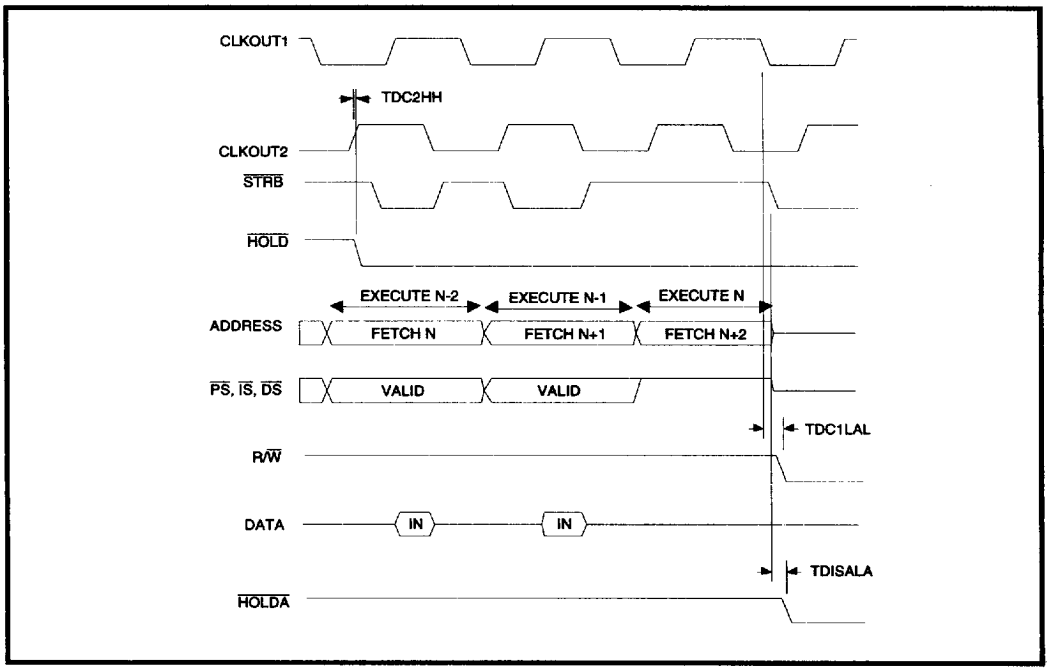

FIGURE 10: Hold Condition Entry Timing

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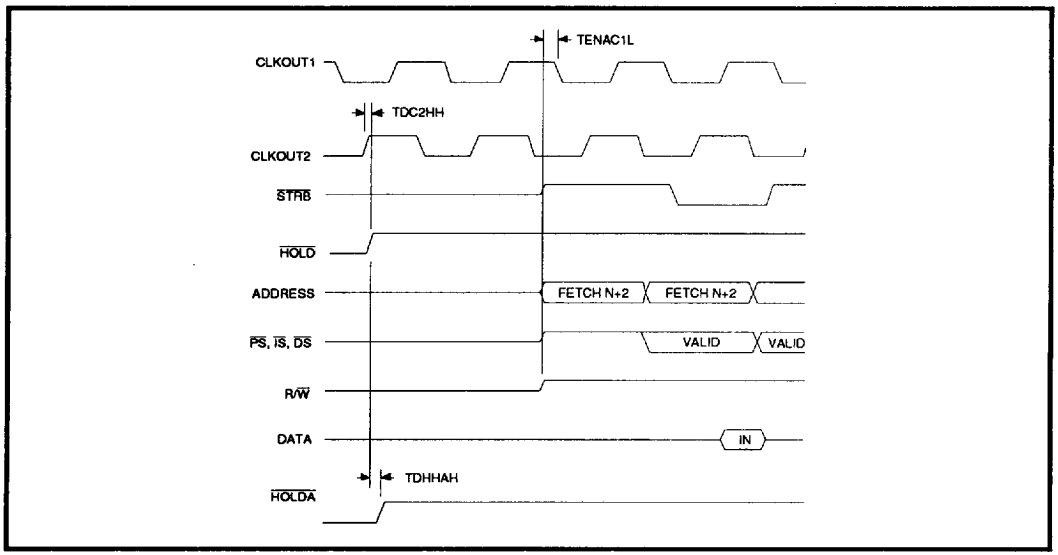


FIGURE 11: Hold Condition Exit Timing

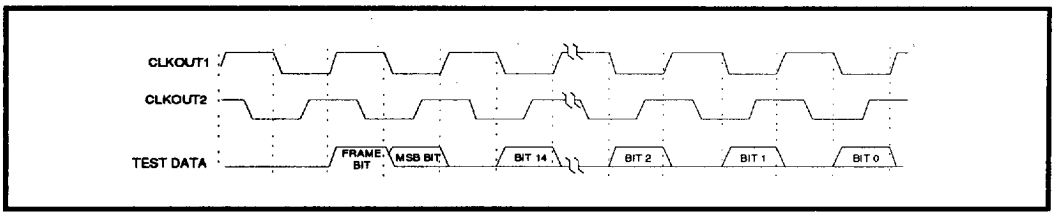


FIGURE 12: Serial Test Pin Timing

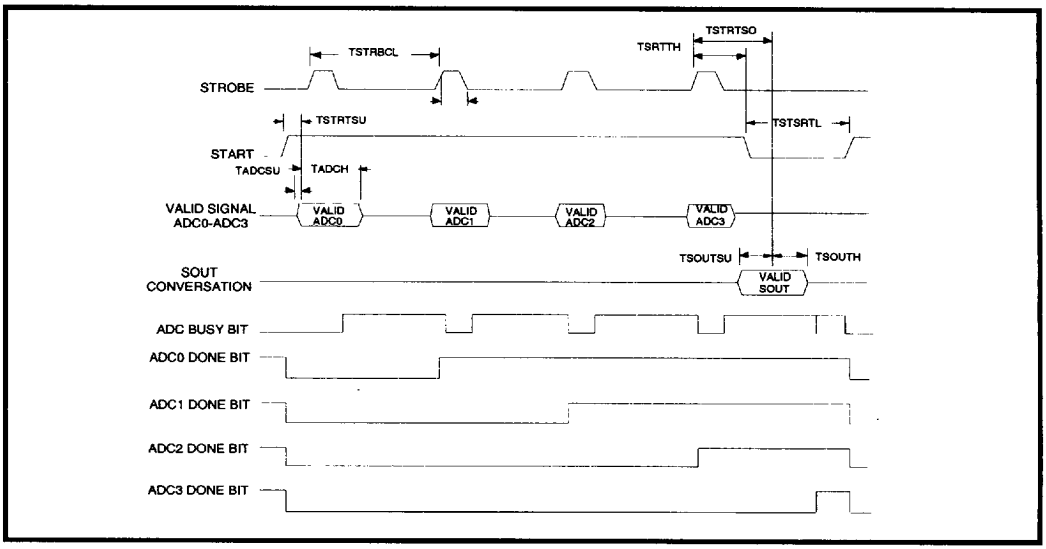


FIGURE 13: ADC Normal Mode Timing

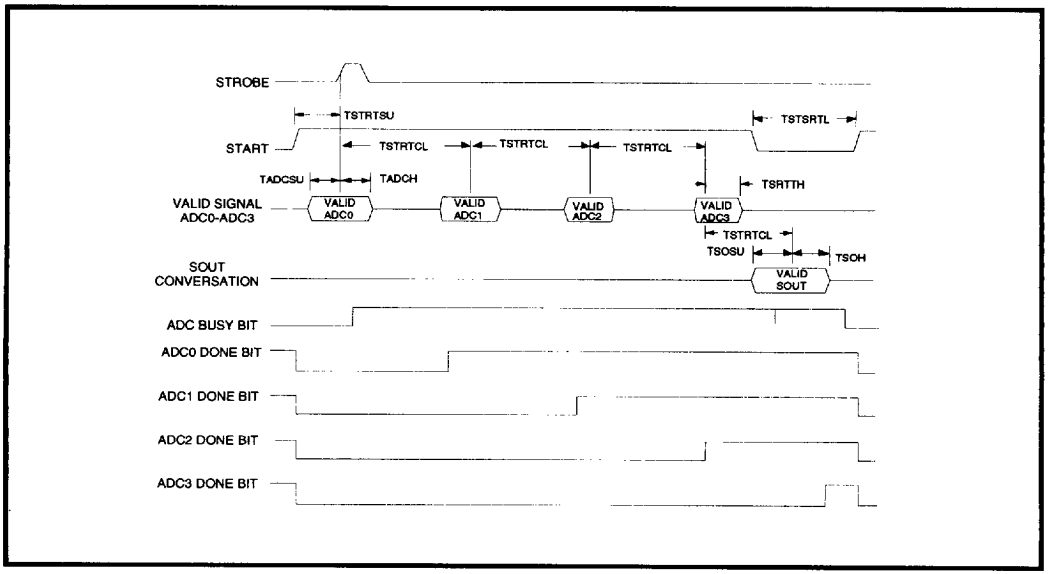
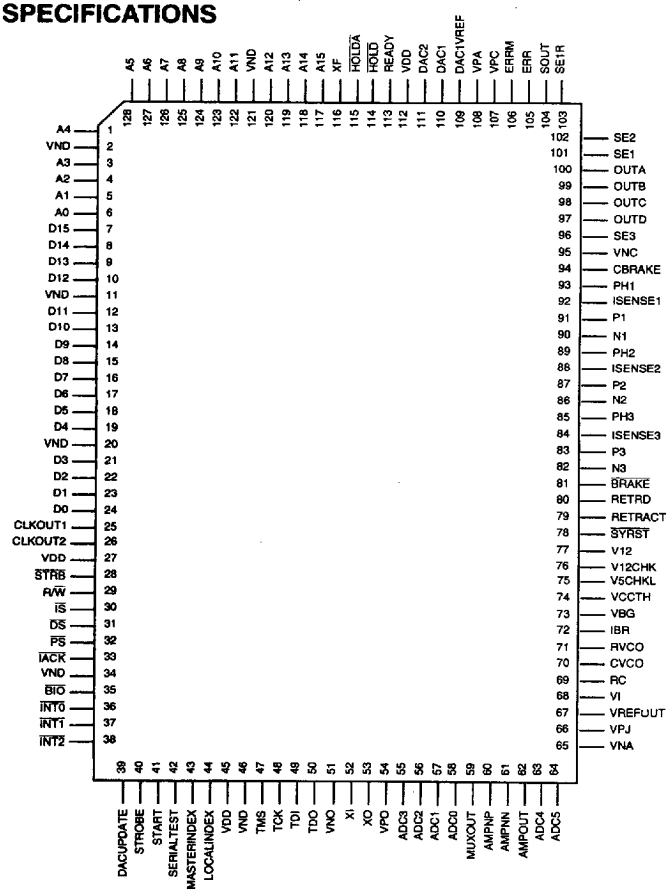


FIGURE 14: ADC Normal-Auto Mode Timing

SSI 32H6840
Advanced Servo and Spindle Predriver with DSP

PACKAGE PIN SPECIFICATIONS

(Top View)



128-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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