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SSI 32P3011
Pulse Detector with Programmable Filter

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DESCRIPTION

The SSI 32P3011 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 48 Mbit/s.

The SSI 32P3011 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed.

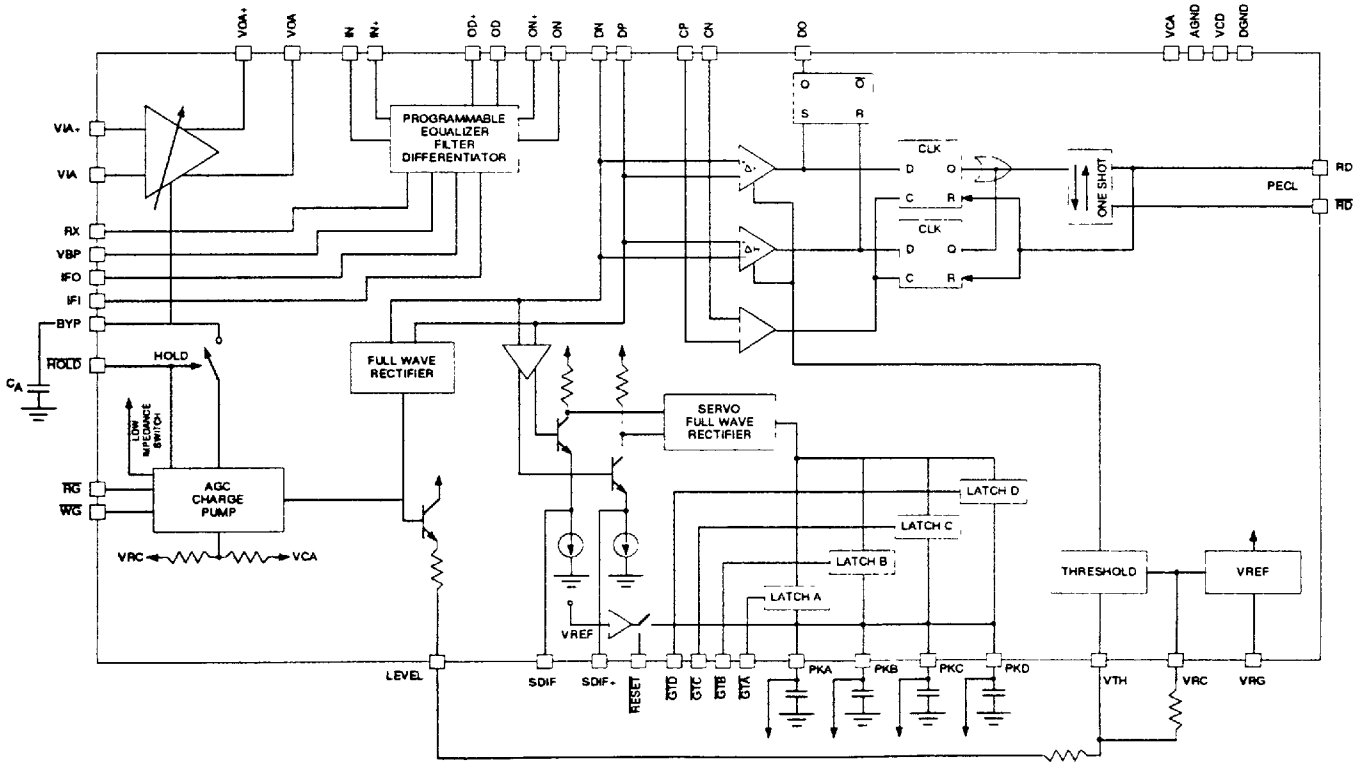
Ideal for constant density recording applications, the SSI 32P3011 low pass filter has a programmable 5-18 MHz bandwidth and 0-14 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3011 requires only a +5V power supply and is available in a 44-lead SOM package.

FEATURES

- **Compatible with 48 Mbit/s data rate operation**
- **Fast Attack/Decay modes for rapid AGC recovery**
- **Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals**
- **Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±0.75 ns filter group delay variation from 0.3 *fc* to *fc* *fc* = 18 MHz**
- **Independent positive and negative threshold qualification to suppress error propagation**
- **0.5 ns max pulse pairing**
- **Servo differentiator and 4-burst servo capture**
- **+5V only operation**
- **44-lead SOM package**

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The SSI 32P3011 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 48 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit. The 4-Burst Servo Capture portion includes four gated servo peak detector/latches that can be reset.

AGC Amplifier

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}] \quad \text{(See note 1)}$$

AGC Actions

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1 Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

AUTOMATIC

Slow Decay: When the DP/DN signal is below 1 Vppd, a slow decay current, ID, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the maximum Id is 4.5 µA when the filter cutoff frequency is 18 MHz.

Slow Attack: When the DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, ICH, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 30 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Fast Attack: When the DP/DN signal exceeds 1.25 Vppd, the device enters a Fast Attack mode. A fast attack current, ICHF, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

Note:
1. In a closed AGC loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. Ao = 11, K = 0.22, VR = 3.6.

USER CONTROL

Fast Recovery: When FAST REC = 1, a fast decay current, IDF, continuously charges the BYP capacitor. This function raises the AGC amplifier gain rapidly. This fast decay current is 20 x ID. The automatic AGC actions remains active in the Fast Recovery mode. With the large Fast Attack current, the DP/DN signal level quickly reaches an equilibrium at ~ 125% of nominal level. Without the Fast Recovery function, the AGC amplifier gain can only be slowly increased with the slow decay current.

Hold: All the above AGC actions can be suspended with $\overline{HOLD}$ = 0. The AGC amplifier gain is held constant, except for any leakage effect at the BYP pin.

While the Fast Recovery function reduces the AGC amplifier gain recovery time, the input impedance control function speeds up the input settling. In a Write Mode, a large DC voltage could be stored at the external AC coupling capacitors. When switched back to the Read Mode, the DC voltage across these capacitors must settle to its normal level. With LOWZ = 1, the input RC time constant is lower for fast input recovery.

Programmable Filter

The SSI 32P3011 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 5-18 MHz; the high frequency equalization is programmable from 0-14 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{at } T = 27°C$$

IFI should be made proportional to IFO for fc temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(\text{MHz}) = 22.5 \cdot \frac{\text{IFI}}{\text{IFO}} \cdot \frac{1}{\text{Rx}(\text{k}\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(\text{MHz}) = 22.5 \cdot \frac{1}{\text{Rx}(\text{k}\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(\text{MHz}) = 18 \cdot \frac{\text{F\_Code}}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$\text{Boost}(\text{dB}) = 20\log_{10}\left[\left(\frac{\text{Kb} \cdot \text{VBP}}{\text{VRG}}\right) + 1\right]$$

Kb = 0.02808 fc + 3.368

fc is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

When DACs are used, the boost relation then reduces to:

$$\text{Boost}(\text{dB}) = 20\log_{10}\left[\left(\text{Kb} \cdot \frac{\text{S\_Code}}{127}\right) + 1\right]$$

Dual Hysteresis Comparator & Hysteresis Threshold Setting

The SSI 32P3011 uses a dual comparator architecture to allow independent positive and negative threshold qualification. Each signal peak which exceeds the threshold is qualified regardless of the previous qualified peak's polarity. This has the advantage of suppressing error propagation, if one signal peak is weak in magnitude and missed.

The SSI 32P3011 allows two implementations of hysteresis: fixed by hysteresis threshold or DP/DN tracking hysteresis threshold. Fixed hysteresis threshold can be simply done by setting a DC voltage at the VTH pin, such as a resistor divider from VCC to VRC. The hysteresis threshold at the comparator can be computed as Hysteresis Gain x (VTH - VRC). For high performance system applications, however, the DP/DN tracking hysteresis threshold is recommended.

DP/DN tracking hysteresis has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The hysteresis threshold is designed as a percentage of the DP/DN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the VTH pin. The LEVEL output is an amplified and rectified replica of the DP/DN voltage. It can be computed as: Level Gain x (DP - DN) ppd + VRC. With the resistor divider, a fraction of the LEVEL output is presented at the VTH pin. The hysteresis threshold, as a function of (DP - DN)ppd, can be summarized as:

Level Gain x (DP - DN)ppd x Resistor Dividing Ratio x Hysteresis Gain.

For a typical case of 1 Vppd at the DP/DN pins, assume equal value resistors in the divider network, the hysteresis threshold is 0.75 x 1 x 0.5 x 0.445 = 0.17V. This represents 34% hysteresis on a 1 Vppd signal.

While both the Level Gain and the Hysteresis Gain bear moderate tolerance due to typical process variations, they inversely track each other to yield a much tighter hysteresis threshold in a closed loop. In designing the hysteresis threshold, the nominal Level Gain and Hysteresis Gain values should be used. The tolerance on DP/DN tracking hysteresis threshold is specified as the Tracking Hysteresis Tolerance. With a 15% tolerance in the above example, the % hysteresis is expected between 34% x (1-0.15) = 29% to 34% x (1+0.15) = 39%.

While the external resistor divider ratio determines the hysteresis threshold, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DP/DN peak-to-peak, but large enough to provide a constant hysteresis threshold in each level qualification.

The pulse qualifier output is the pseudo–ECL differential output, pins RD and $\overline{RD}$. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width is a function of fc (the reference current into the IFI pin).

$Pw = (195.3/fc) - 2.71$ ns

DO is a test point to examine the D input of a qualifier D flip-flop. It requires a 5 kΩ resistor to GND.

The SSI 32P3011 provides a 4-Burst Servo Capture circuit. The signal at the DP/DN inputs is full wave rectified, level shifted and gated to servo peak detector / latches. A servo differentiator block is available if servo signal differentiation is necessary. The transfer function from DP/DN input to the differentiator output is given as:

$$\frac{\text{Vout @ Differentiator}}{(DP-DN)ppd} = \frac{2380Cs}{LCs^2 + C(R+48.1)s+1}$$

where C, L and R are external passive components across SDIF+ and SDIF-

$15\ pF < C < 125\ pF$

$s = j\omega$

If servo signal differentiation is not needed, the servo differentiator can be turned into a ~1X gain block with a 2 kΩ resistor across SDIF+ and SDIF-.

One master reset control, $\overline{RESET}$, is used to initialize all four servo outputs, PKA-D, to a level below the offset bias of servo read data. Each servo burst is individually selected with its $\overline{GT}$x- control. For example, with GTA = 0, the DP/DN signal is full wave rectified and gated to PKA output. The PKx- output is a peak captured 1 Vp signal biased at 2.0V. The output signal can be between 2.0V to 3.0V. Figure 2 shows a typical servo timing sequence and the respective outputs.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
FAST REC	I	TTL compatible input. When high, the device is in Fast Decay Mode.
LOWZ	I	TTL compatible input. When high, the input impedance is lower for faster write-to-read recovery.
$\overline{GTA}$, $\overline{GTB}$, $\overline{GTC}$, $\overline{GTD}$	I	TTL compatible input. When low the corresponding servo gate channel is enabled.
$\overline{HOLD}$	I	TTL compatible input. When low the AGC action is suspended.
$\overline{RESET}$	I	TTL input, when low, all four servo capture outputs are reset to a level below normal servo read bias.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DO	O	ECL compatible data comparator latch output pin.
RD, $\overline{RD}$	O	ECL compatible read data output pins.
LEVEL	O	Buffered NPN emitter output that provides a fullwave rectified signal which may be fed to the VTH input. The signal is referred to VRC.
SDIF+, SDIF-	-	Pins for external differentiating network for servo data.
PKA, PKB PKC, PKD	O	Peak detector outputs. A 1000 pF hold capacitor must be connected between PKX and AGND. These outputs are high impedance when not enabled by $\overline{GTX}$
ANALOG PINS		
VRC	-	Reference voltage pin. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO	-	Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.
IFI	-	Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
BYP	-	The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD	-	Analog and Digital +5 volts.
AGND, DGND	-	Analog and Digital grounds. Must be tied together for proper operation.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V < Vcc < 5.5V, 0°C < Ta < 70°C

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65°C to +150°C
Junction Operating Temperature,Tj	+130°C
Supply Voltage, VCA, VCD	-0.7 to 7V
Voltage Applied to Inputs	-0.7 to VCA, VCD V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
Supply Voltage	VCA = VCD = VCC	4.5V < VCC < 5.5V
Ambient Temperature, Ta		0°C < Ta < 70°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
PD	Power Dissipation	Outputs unloaded 4.5V < VCA, VCD < 5.5V		460	600	mW

LOGIC SIGNALS

VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC +0.3	V
IIL	TTL Input Low Current	VIL = 0.4V	-0.4			mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOHE	ECL Output High Voltage		VCC -1.2		VCC-0.4	V
VES	ECL Differential Output Swing |V(RD) – V($\overline{RD}$)|		0.3		0.6	V
TRF	EC1 Output Rise and Fall Time	CL ≤ 10 pF			3.5	ns
TCS	Control Input Switching Times				0.1	µs

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. C_A = 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIB	Input Range	Filter boost at fc = 0 dB	24		240	mVppd
		Filter boost at fc = 11 dB	20		100	mVppd
VD	DP-DN Voltage	VIA± = 0.1 Vppd	0.90		1.10	Vppd
VDV	DP-DN Voltage Variation	24 mV < VIA± < 240 mV			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity w.r.t. BYP Voltage			38		dB/V
DR	VOA+ VOA- Dynamic Range	THD = 1% max	0.75			Vppd
RINDA	Differential Input Resistance	LOWZ = 0	3.7		7.4	kΩ
		LOWZ = 1		160		Ω
RINSA	Single Ended Input Resistance	LOWZ = 0		3.0		kΩ
		LOWZ = 1		80	150	Ω
VOS	Differential Output Offset Variation	from min. gain to max. gain	-200		+200	mV
VIN	Input Referred Noise Voltage	gain = max, Rs = 0Ω filter not connected to VOA± Bw = 15 MHz		12	18	nV/√Hz
BW	Bandwidth	No AGC action, Gain = 22	55	86		MHz
CMRR	Common Mode Rejection Ratio	gain = 22, Vin = 0 VDC + 100 mVpp @ 5 MHz	40	65		dB
PSRR	Power Supply Rejection Ratio	gain = 22, 100 mVpp on VCA, VCD @ 5 MHz	40	58		dB
TGD	Gain Decay Time	VIA± = 240 mV to 120 mV VOA± > 0.9 Final Value IFI = 600 µA		40		µs
TGA	Gain Attack Time	VIA± = 120 mV to 240 mV VOA± < 1.1 Final Value IFI = 600 µA		2		µs

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V < VCC < 5.5V, 0°C < Ta < 70°C

AGC CONTROL

The input signals are AC coupled to DP and DN. C_A = 1000 pF.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ID	Discharge Current	FASTREC = 0, DP - DN = 0V		0.008 x IFI		A
IDF	Fast Discharge Current	FASTREC = 1		20 x ID		A
ICH	Charge Pump Attack Current	FASTREC = 0, DP - DN = 0.55V		30 x ID		A
ICHF	Charge Pump Fast Attack Current, Ichf	FASTREC = 0, DP - DN = 0.675V		7 x ICH		A
IK	BYP Pin Leakage Current	$\overline{HOLD}$ = 0, V(BYP) = Vcc–1.5V	-0.1		+0.1	µA
VRC	VRC Reference Voltage			VCA -VRG		V
IVRC	VRC Output Drive	ΔVRC < 20 mV	-0.75		+0.75	mA
VRG	VRG Reference Voltage	Isource 0 mA to 1 mA	2.2		2.45	V

EQUALIZER/FILTER

The input signals are AC coupled to IN+ and IN-.

fc	Filter Cutoff Frequency	$fc(MHz) = 22.5 \cdot \frac{IFI}{IFO} \cdot \frac{1}{Rx(k\Omega)}$	5		18	MHz
IFO	IFO Reference Current	IFO = 0.75/RX; Tj = 27°C 5 kΩ > RX > 1.25 kΩ	0.15		0.6	mA
RIFO	IFO Output Resistance	IFO = 0.6 mA @ Tj = 27°C	25			kΩ
VIFO	IFO Output Voltage Compliance	IFO = changes < 6%	0		Vcc -1.5	V
IFI	IFI Program Current Range	Tj = 27°C, 27 MHz > *fc* > 9 MHz	0.167		0.6	mA
RIFI	IFI Input Resistance	IFI = 0.6 mA @ Tj = 27°C			2.5	kΩ
VIFI	IFI Input Bias Voltage	IFI = 0.6 mA @ Tj = 27°C	0.75		2.5	V
FCA	FCA Filter FC Accuracy	Rx = 5 kΩ, IFI = 4 IFO	-10		10	%
RX	RX Range		1.25		5	kΩ
AO	Normal Low Pass Gain AO = (ON ±) / (IN±)	Fin = 0.67*fc*	1.4		2.2	V/V
AD	Differentiated Low Pass Gain AD = (OD ±) / (IN±)	Fin = 0.67*fc*	0.9AO		1.3AO	V/V

EQUALIZER/FILTER (continued)
The input signals are AC coupled to IN+ and IN-.

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
FBA	Boost Accuracy	VBP = VRG	fc = 5 MHz	11.58	13.08	14.58	dB
			fc = 18 MHz	12.26	13.76	15.26	dB
		VBP/VRG = 0.5	fc = 5 MHz	7.80	8.80	9.80	dB
			fc = 18 MHz	8.36	9.36	10.36	dB
TGD1	Group Delay Variation	fc = 18 MHz, VBP = 0 to VRG fc > Fin > 0.3 fc		-0.75		+0.75	ns
TGD2		fc = 5 to 18 MHz, VBP = 0 to VRG fc > Fin > 0.3 fc		-2.5		+2.5	%
VOSVF	Output Offset Voltage Variation	150 µA < IFI < 600 µA		-200		+200	mV
DRF	VOF Filter Output Dynamic Range	Fin = 0.67 fc THD = 5% max, 0 < Ta < 25°C THD = 3% max, 25 < Ta < 70°C		1.5			Vpp
RINF	Filter Input Differential Resistance			3.0	4		kΩ
CINF	Filter Input Capacitance					7	pF
ROF	Filter Output Resistance	IO = 0.5 mA				60	Ω
IOF	Filter Output Current			-1.0		2.0	mA
VNN	Eout Output Noise Voltage; ON+, ON-	BW = 100 MHz, RS = 50Ω VBP = 0, fc = 18 MHz			2.0	3.0	mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, fc = 18 MHz			4.0	5.5	mVRms
VND	Eout Output Noise Voltage; OD+, OD-	BW = 100 MHz, RS = 50Ω VBP = 0, fc = 18 MHz			5.0	7.0	mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, fc = 18 MHz			11.0	15.0	mVRms

DATA COMPARATOR
The input signals are AC coupled to DP and DN.

RIND	Differential Input Resistance		7		13	kΩ
CIND	Differential Input Capacitance				5	pF
VOSD	Comparator Offset Voltage (Note 1)				4	mV
VLOS	Level Offset Voltage	V(LEVEL) – V(VRC), IL = 50 µA, V(DD/DN) = 0v	-30		30	mV

Note 1: Not directly measurable.

DATA COMPARATOR (continued)
The input signals are AC coupled to DP and DN.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
GLEV Level Output Gain	DP-DN = 0.25 to 0.5 VDC, $GLEV = \frac{V_{LEVEL} - V_{RC}}{2 \times (DP-DN)}$	0.712		0.788	V/V
RLEV Level Output Resistance			250		Ω
GHYS Threshold Voltage Gain	VTH-VRC = 0.3V	0.43		0.52	V/V
	VTH-VRC = 0.9V	0.42		0.49	
VSH Threshold Voltage Hysteresis (Note 1)			0.20 x GHYS x (VTH -VRC)		V/V
TPDD Propagation Delay	From DP-DN to DO		5		ns
IVTH VTH Input Bias Current	VRC ≤ VTH ≤ VRC + 0.9V	-2		2	µA
VLOS Level Offset Voltage	V(LEVEL) - V(VRC), I(LEVEL) = 50 µA	-30		30	mV

CLOCKING
The input signals are AC coupled to CP and CN.

VOSC	Comparator Offset Voltage (Note 1)			4	mV
RINC	Differential Input Resistance		7	13	kΩ
CINC	Differential Input Capacitance			5	pF
TDS	D Flip-Flop Set Up Time	DP-DN threshold to CP-CN zero cross, CP-CN = 1Vppd at 18 MHz		1	ns
PP	Pulse Pairing	Fin = 12 MHz, Vs = 1Vpp		0.6	ns
TPDC	Propagation Delay from CP-CN zero crossing to RD		7		ns
PWRD	RD Output Pulse Width Accuracy	Differential pulsewidth PW(nom, ns) = 195.3/fc – 2.71, fc in MHz	-20	+20	%

Note 1: Not directly measurable.

SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER

An external series network is connected between SDIF and $\overline{SDIF}$ to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ISDIF	SDIF+ to SDIF- pin current	Differentiator impedance must must be set so as not to dip the signal for this level	0.75	1.05	1.35	mA
RDIF	Internal differentiator pull-up resistors	Cannot be directly tested	1.0	1.2	1.4	kΩ
FWR	Input voltage range to maintain FWR voltage gain	Cannot be directly tested	0.1		1.2	Vppd
RERR	Rectification Error				5	%
AFWR	FWR Voltage Gain from DP/DN Input to PKA-D Outputs	2.3 kΩ between SDIF+ and SDIF-	0.72	0.9	1.08	V/Vppd
VCOS	PKA-D Channel to Channel Offset	1Vppd input to servo FWR	-10		+10	mV
PKOB	PKA-D Output Bias	Channel enabled, DP-DN = OV	1.8	2	2.2	V
PK	PKA-D Output Levels		PKOB		PKOB+1	V
PKRST Level	PKA-D Output Reset	$\overline{RESET}$ = Low	PKOB-0.95		PKOB-0.65	V
IRST	PKA-D Peak Reset Discharge Current on each output		480	700	1000	µA
PKLK	PKA-D Leakage Current	Channel Disabled: DP-DN = 1Vpdd			10	µA
IPK	PKA-D Peak Charging Current		10	20		mA
TRON	Reset Current Turn On Delay from $\overline{RESET}$ Fall				50	ns
TROFF	Reset Current Turn Off Delay from $\overline{RESET}$ Rise				100	ns
TSUR	RST Rise Setup Time to GT-Falls		100			ns
TSUG	GT-Rise Setup Time to Next GT-Fall		100			ns

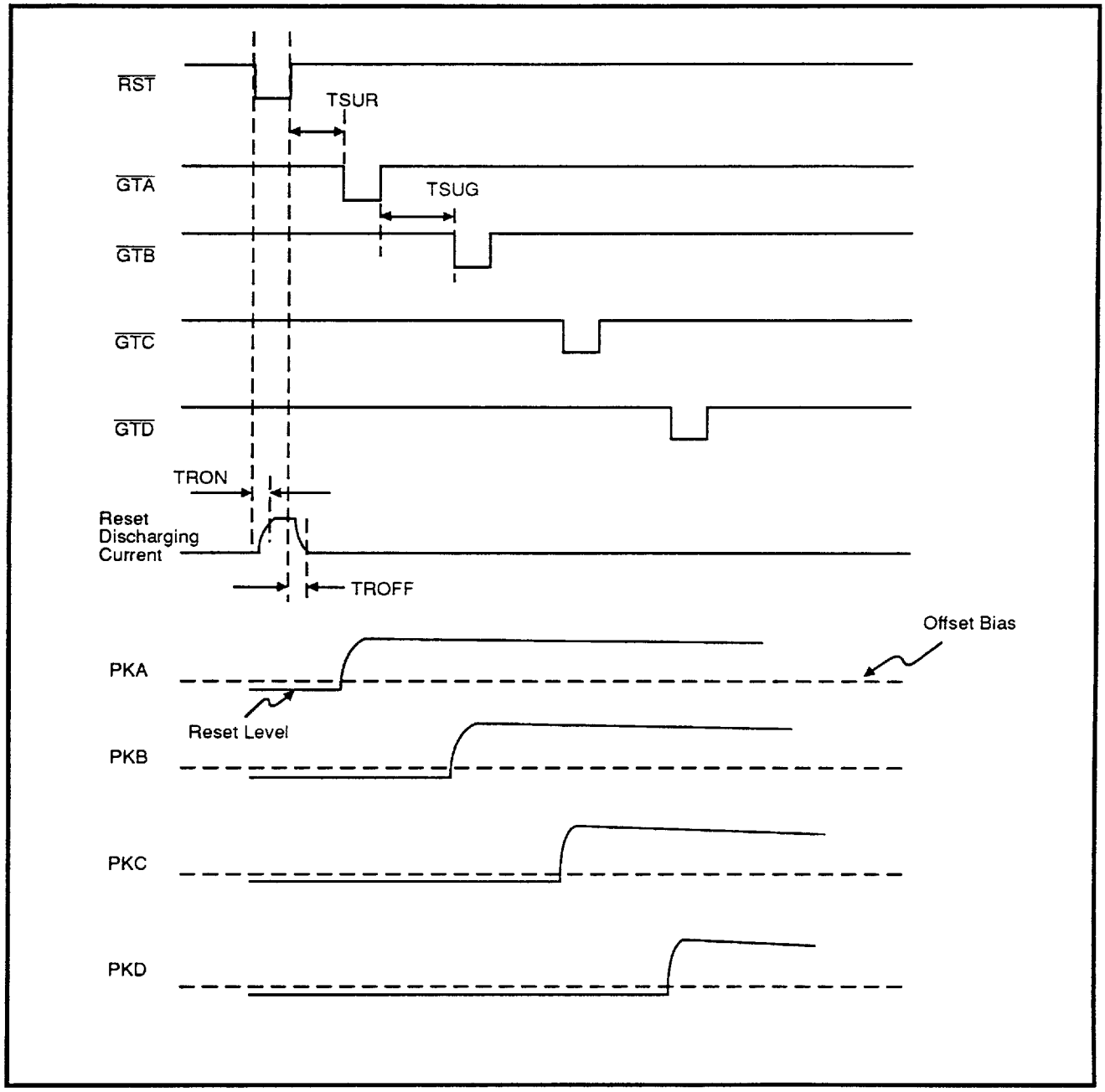
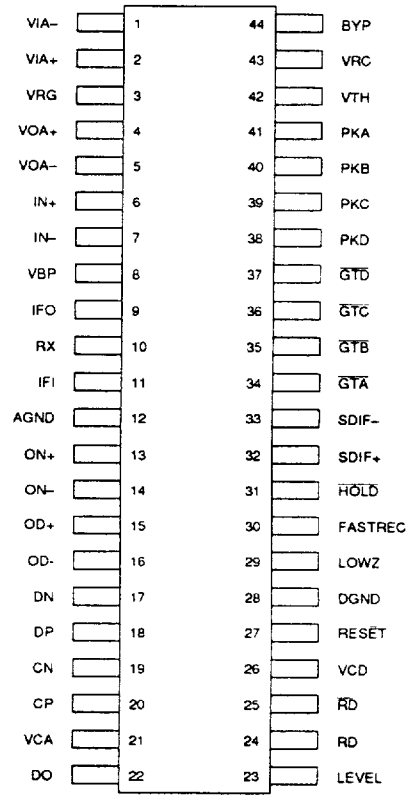


FIGURE 2: Servo Capture Timing Sequence

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θjA

44-Lead SOM	70°C/W



32P3011
44-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32P3011	44-Lead Small Outline (31.6 mil pitch)	32P3011-CM	32P3011-CM

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