SSI 78Q8330/8330A
Ethernet Coaxial Transceiver

January 1993

DESCRIPTION

The SSI 78Q8330 and SSI 78Q8330A are line transceivers for IEEE 802.3 coaxial cable applications. The SSI 78Q8330 is compliant with thin cable (10Base2) requirements and compatible with thick cable (10Base5) operation. The SSI 78Q8330A is tested to be compliant with both 10Base2 and 10Base5 requirements.

These transceivers provide the interface between the single-ended coaxial cable signals and the Manchester-encoded differential logic signals. Primary functional blocks include the receiver, transmitter, collision detection and jabber timer. These ICs may be used in either internal or external MAU environments.

The SSI 78Q8330/8330A design is optimized for low power consumption. Typical supply current while transmitting is 96 mA, and only 56 mA when not transmitting. The low power consumption coupled with 20-pin PLCC or 64-lead TQFP packaging make this product ideal for portable computer applications.

FEATURES

- **SSI 78Q8330 compliant with 10Base2 and compatible with 10Base5 requirements**
- **SSI 78Q8330A compliant with both 10Base2 and 10Base5 requirements**
- **Innovative design minimizes power consumption - ideal for portable computer applications**
- **Integrated jabber timer function**
- **Minimal external component count**
- **For internal or external MAU applications**
- **Available in 20-pin PLCC, DIP, or 64-lead TQFP**

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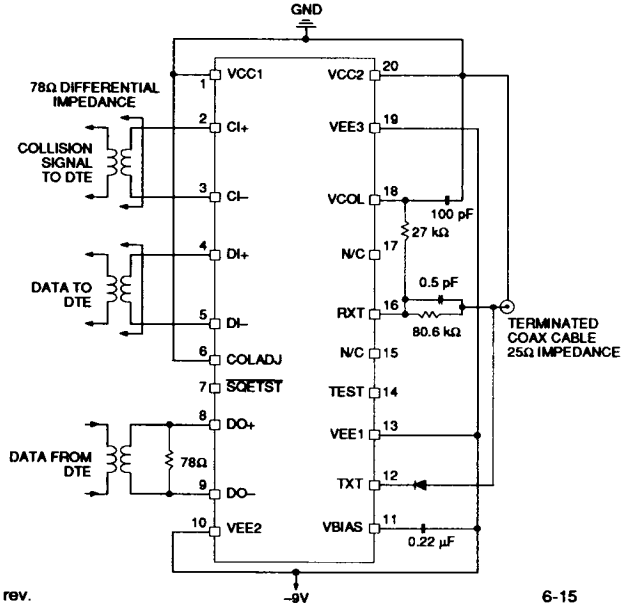
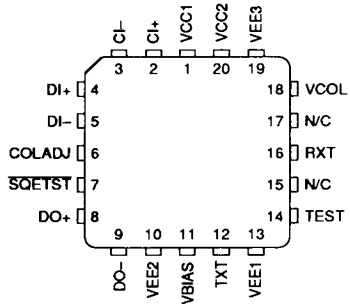
SSI 78Q8330 CONNECTION DIAGRAM



PIN DIAGRAM



20-pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78Q8330/8330A IEEE-802.3/Ethernet/ Cheapernet Transceiver consists of four sections: 1) Transmit - receives signals from DTE and sends it to the coaxial medium, 2) Receive - obtains data from medium and sends it to DTE, 3) Collision Detect - indicates to DTE any collision on the medium, and 4) Jabber - guards medium from DTE transmissions that are excessive in length.

TRANSMITTER

The SSI 78Q8330/8330A receives differential signals from the DTE over the AUI interface.

Differential data is received through a squelch network that rejects signals with pulse widths less than 7 ns, or with levels more positive than -175 mV peak. Signals with pulse widths wider than 50 ns and levels more negative than -275 mV peak from the DTE are guaranteed to be enabled. This minimizes false starts due to noise and ensures no valid packets are missed.

The coax driver provides the driving capability to ensure adequate signal level at the end of the maximum length network segment (500m 10Base5, 185m 10Base2) under the worst-case number of connections (100 nodes 10Base5, 30 nodes 10Base2). The required rise and fall times of data transmitted on the network are maintained by the driver. The driver's output is connected to the medium through external isolating diodes. To safeguard network integrity, the driver is disabled whenever power falls below the minimum operation voltage.

During transmission, the jabber controller monitors the duration that the transmit driver is active and disables the driver if the jabber time is exceeded. This prevents network tie-up due to a "jabbering" transmitter. Once disabled, the driver remains disabled for an additional 310-500 ms after the DO± pair is idle. During the disable time, the 10 MHz internal oscillator signal is sent on the CI± pair to the DTE.

When $\overline{\text{SQETST}}$ is tied to VEE, the IC generates a Collision Detect message at the end of every transmission. This signal is a self-test indication to the DTE that the Medium Attachment Unit (MAU) collision pair is operational.

RECEIVE AND CARRIER DETECT

Received signals are acquired from the coax tap through a high-impedance resistive divider. A high input-impedance (low capacitance, high bandwidth) DC-coupled input amplifier in the chip receives the signal. The received signal is internally AC coupled and then sliced. The carrier detector compares received signals to a reference. Signals meeting carrier squelch criteria are passed to the differential line driver within five bit times from the start of packet.

Received data is transmitted from the DI± pair through an isolation transformer of the AUI interface. Following the last transition in a packet, the DI± pair is held high for two bit times and then decreases to the idle level within eighty bit times.

COLLISION DETECT

The SSI 78Q8330/8330A detects collisions if two or more stations are transmitting on the network.

The average DC level of received signals is compared against the collision threshold reference. If the level is more negative than the reference, an enable signal is generated to the CI± pair.

The collision oscillator is a 10 MHz oscillator which drives the differential CI± pair to the DTE through an isolation transformer. This signal is gated to the CI± pair whenever there is a collision, a Collision Detect test is in progress, or the jabber controller is activated.

The CI± output meets the drive requirements for the AUI interface. The output stays high for two bit times at the end of the packet, decreasing to the idle level within eighty bit times.

JABBER FUNCTION

The jabber timer monitors the activity on the DO± pair and senses TXT faults. It inhibits transmission if the coax driver is active for longer than the jabber time (20-35 ms). A 10 MHz internal oscillator signal is enabled on the CI± pair for the fault duration after the jabber time is exceeded.

After the fault is removed, the jabber timer counts the unjab time of 310-500 ms before it enables the driver.

SQE TEST

A Signal Quality Error (SQE) test will occur at the end of every transmission if the $\overline{\text{SQETST}}$ pin is tied to VEE. An SQE test signal is a 10 MHz signal gated to the CI± pair. The SQE test ensures that the twisted pair assigned for collision notification to the DTE is intact and operational. The SQE test starts eight bit times after the last transition of the transmitted signal and lasts for a duration of eight bit times.

The SQE test can be disabled by connecting the $\overline{\text{SQETST}}$ pin to GND.

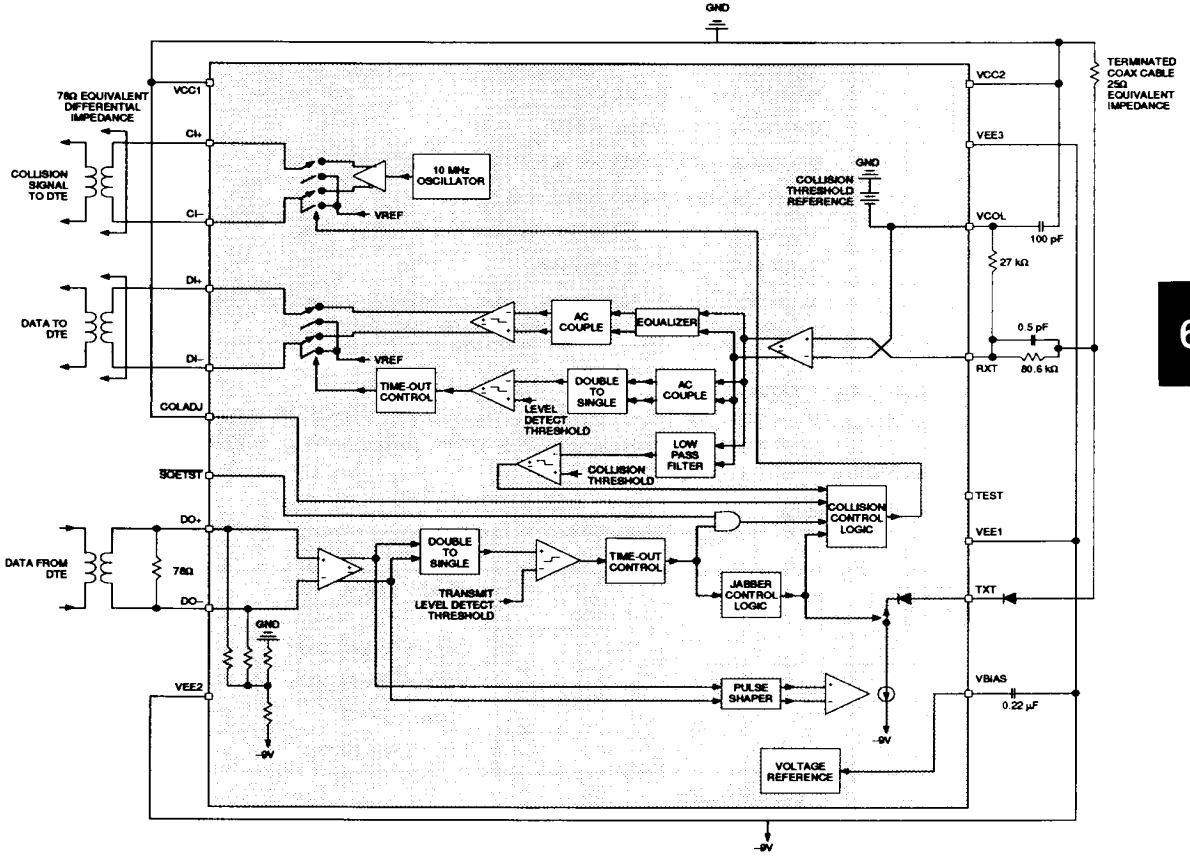


FIGURE 1 : Functional Diagram

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC1, VCC2	-	Positive supply to chip. Tied to external ground.
VEE1, VEE2, VEE3	-	Negative supply to chip. Tied to external -9 volts.
TXT	O	Open collector output current data to coax cable.
DO+, DO-	I	Differential input data from DTE.
RXT	I	Input data from coax cable.
VCOL	I	Collision threshold reference.
DI+, DI-	O	Differential output data to DTE.
CI+, CI-	O	Differential output collision detect signal to DTE.
$\overline{\text{SQETST}}$	I	Pin to activate collision detect test circuit.
VBIAS	-	External bypass pin for internally generated voltage bias.
TEST	I	Pin for placing chip in test mode.
COLADJ	I	Pin tied to VEE sets proper 10BASE5 collision threshold detect level. Pin left open sets proper 10BASE2 collision threshold detect level.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 8.1V < VCC-VEE < 9.9V and 0 °C < T(ambient) < +70 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value. Unless otherwise specified, test configuration is as shown in Figure 1.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage; Vcc (Relative to VEE Pins)	-0.5 to +12 V
VBIAS Pin	-40mA to +40 mA
All other Pins	VEE - 0.3V to VCC + 0.3V
Storage Temperature	-65 to 150 °C
Soldering (Reflow or Dip)	260 °C for 10 sec

POWER SUPPLY CURRENTS AND POWER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Current	Includes current from VCC1, VCC2, TXT pins				
Transmitter active			96	121	mA
Transmitter inactive			56	74	mA

TTL COMPATIBLE INPUTS: $\overline{\text{SQETST}}$ Pin

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Input Low Voltage	Vil		VEE-0.3		VEE+0.8	V
Input High Voltage	Vih		VEE+2.0 or pin open		VCC+0.3	V
Input Low Current		Vil = VEE + 0.4 V	+0.05		-0.4	mA
Input High Current		Vih = VEE + 2.4 V			100	µA

TRANSMITTER TO COAX

Input Capacitance TXT Pin	CTXT	f = 10 MHz Transmitter inactive				
		8.1< VCC - VEE < 9.9V			9.5	pF
		0 < VCC - VEE < 8.1V			11.0	pF
Input Resistance TXT Pin	RTXT	V(TXT) = VCC - 4V, Transmitter inactive	1000			kΩ
Differential Input Impedance DO+ to DO- Pins	ZDO	f = 10 MHz	1.6		5.6	kΩ
DO+/- Common Mode Input Resistance	Ricm	DO+ tied to DO-	1.5		2.8	kΩ
DO+/- Common Mode Output Voltage	Vicm	DO+/- open	VEE+3.0		VEE+5.0	V
DO+/- Input Current	Iidl & Iidh	VEE < V(DO+/-) <VCC, DO+ tied to DO-	-5		7	mA
Output Leakage Current on TXT Pin	IBTXT	Transmitter Inactive	-0.5		+5.0	µA
TXT Output High Voltage	VH	25 Ω TXT pin to VCC	VCC-.425		VCC	V
TXT Output Low Voltage	VL	25 Ω TXT pin to VCC	VCC-2.200		VCC-1.625	V
TXT Differential Output Voltage	VTXTHL	VTXTHL = VH-VL, 25 Ω TXT pin to VCC	1.400		2.200	V
TXT Average Output Voltage	VTXTOFF	VTXTOFF = (VH+VL)/2 25 Ω TXT pin to VCC	VCC -1.125	VCC -1.00	VCC -.925	V
Differential Input Squelch Threshold	VIDC	V(DO+)-V(DO-)	175	225	275	mVp
TXT Output Current Rise/Fall Time	tTXTR, tTXTF	f = 5 and 10 MHz	20		30	ns

ELECTRICAL SPECIFICATIONS

TRANSMITTER TO COAX (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Difference In Driver Rise vs. Fall Times	tTDRF	|tTXTR - tTXTF| f = 5 and 10 MHz		0.5	2	ns
Transmitter Turn On Delay	tTON	f = 10 MHz 1 Bit = 100 ns			2	Bits
DO+/- Input Pulse Width to Stay On	tPWSON				105	ns
DO+/- Input Pulse Width to Turn Off	tPWOFF		200			ns
Transmit Static Delay	tTSDR, tTSDF	f = 10 MHz		36	50	ns
Transmit Output Current Data	tTSKEW	tTSKEW =tTSDR - tTSDF f = 5 and 10 MHz	-2.0		+2.0	ns
Jabber Control Time	tJCT		20	30	35	ms
Jabber Reset Time	tJRT		0.31	0.42	0.50	s
Jabber Recovery Time	tJREC	Minimum gap between transmitted packets to prevent jabber activation	1.0			µs
TXT Output Current Pulse Harmonic Content	f2,f3HA	f = 10 MHz, on specified board with 47 pF capacitor between TXT and GND 2nd, 3rd, Harmonics			-20	dB
	f4, f5HA	4th, 5th Harmonics			-30	dB
	f6,f7HA	6th, 7th Harmonics			-40	dB
	f8HA	All Higher Harmonics			-50	dB

RECEIVER FROM COAX

Input Capacitance RXT Pin	CRXT	20-pin PLCC		1.3	1.85	pF
Input Resistance RXT Pin	RRXT	V(RXT) = VCC - 1.5V	120			kΩ
Input Bias Current RXT Pin	IBRXT		-1.5		+20	µA
Receiver Carrier Sense Threshold (measured at coax)	VCAT1	VCAT1 = VCC - V(RXTL), f = 5 MHz, V(RXTH) = VCC	400		800	mVp

RECEIVER FROM COAX (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Receiver Hysteresis (measured at coax)	VCAT2	VCAT2 = [V(RXTH)- V(RXTL)]/2 f = 5 MHz, [V(RXTH)+ V(RXTL)]/2 = VCC -1V			100	mVp
Receiver Turn-Off Holding Time	tROFF		200		1000	ns
Receiver Static Delay	tRSDR, tRSDF	f = 10 MHz		20	50	ns
Receiver Turn-On Delay	tRON	f = 10 MHz 1 Bit = 100 ns VLAT > VCC-600 mV		2	5	Bits
Receiver Output Data Symmetry	tRSKEW	tRSKEW = tRSDR -tRSDF f = 5 and 10 MHz, after first 2 µS from the input beginning packet	-2		2	ns

COLLISION DETECT CIRCUIT

With $\overline{SQETST}$ set high the collision detect output is enabled when a collision is detected on the coax and for jabber timeout. With $\overline{SQETST}$ set low the collision detect output is also enabled at the end of every transmission to the coax.

Collision Sense Threshold	VCOT	COLADJ pin to VEE (for 10BASE5)	VCC -1.492		VCC -1.629	V
		COLADJ pin open (for 10BASE2)	VCC -1.404		VCC -1.581	V
Collision Output Turn-On Delay	tCON			600	900	ns
Collision Reset Time	tCOFF				2000	ns
Collision Output	fCL	fCL= 1/(Tcl + Tch) 78Q8330A	8.5		11.5	MHz
Frequency		78Q8330	8.5		12.5	MHz
Collision Output Duty Cycle	tCOL	$tCOL = \frac{tch}{tch + tcl}$	40		60	%
Collision Detect Test Delay Time	tSTD		0.6		1.5	µs
Collision Detect Test Length	tSTL	1 Bit = 100ns	5	8	15	Bits
Collision Detect Test Holding Time	tHLD		200		1000	ns

ELECTRICAL SPECIFICATIONS

DI+/- AND CI+/- OUTPUT DRIVERS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Differential Output Voltage	VODC	V(CI+) - V(CI-), V(DI+) - V(DI-), RI = 78 Ω	±550		±850	mVp
CI+/- Common Mode Output Voltage	Vcmt1	Output active or idle, VBIAS = (VCC + VEE)/2 ± 5%	VBIAS -1.7		VBIAS - 0.5	V
DI+/- Common Mode Output Voltage	Vcmt2	Output active or idle	VCC-1.7		VCC-0.5	V
DI+/- or CI+/- Differential Output Voltage Imbalance	Vodi	Output active		±5	±20	mV
DI+/- or CI+/- Differential Output Idle Voltage	Vod Off	Output idle	-20		+20	mV
DI+/- or CI+/- Rise Time	tRR	20-80%, RI = 78			5	ns
DI+/- or CI+/- Fall Time	tRF	80-20%, RI = 78			5	ns

TEST MODE

The following test modes are entered by setting the voltage of the TEST pin:

1. Normal mode
2. tJRT and tJCT reduced by factor of 32
3. Activate transmitter and receiver, deactivate jabber and collision detect

TEST Pin Voltage	Mode 1		Pin Open		
	Mode 2	VEE+2.5		VEE+3.5	V
	Mode 3	VEE		VEE+0.2	V

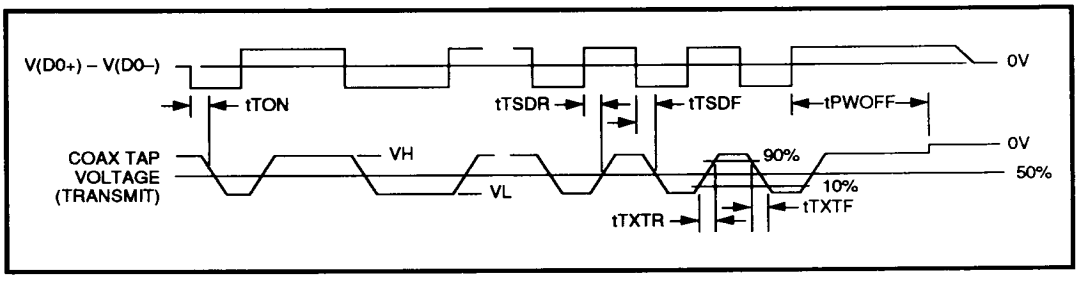


FIGURE 2 : Transmit Function

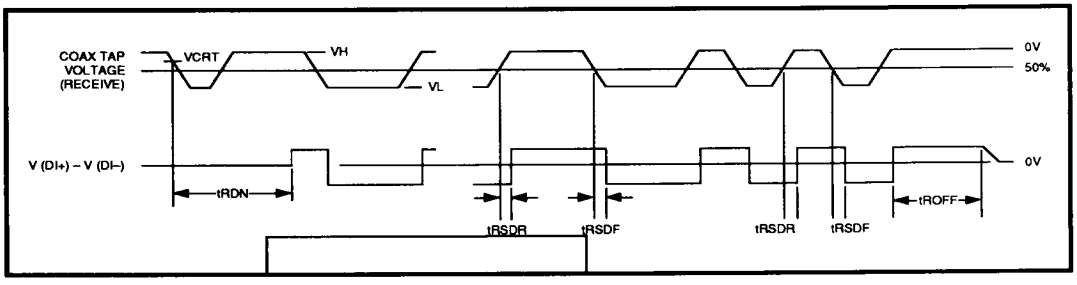


FIGURE 3: Receive Function

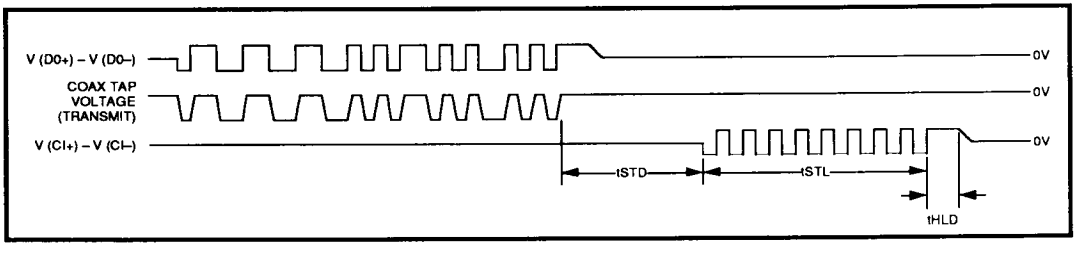


FIGURE 4: SQE Test

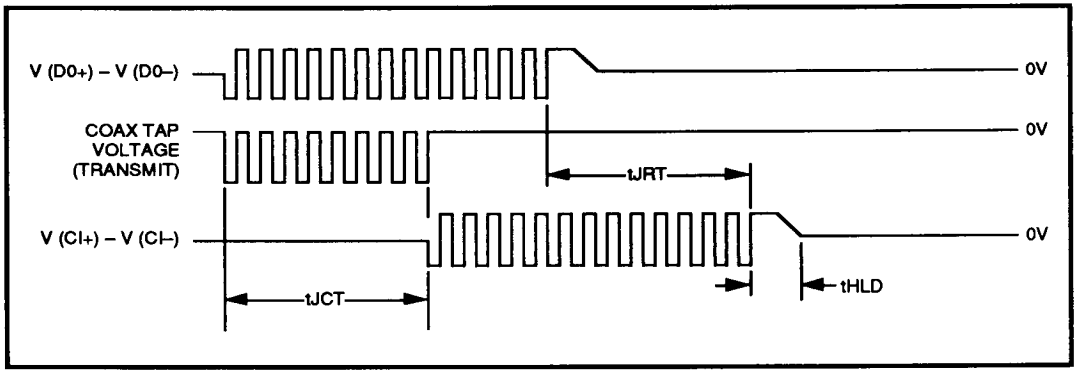


FIGURE 5: Jabber Function

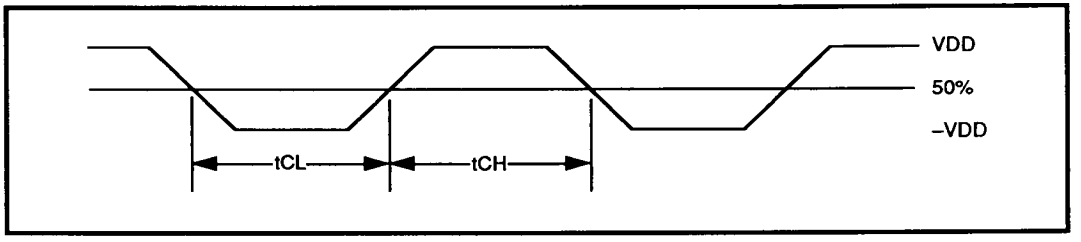


FIGURE 6 : CI± Parameters

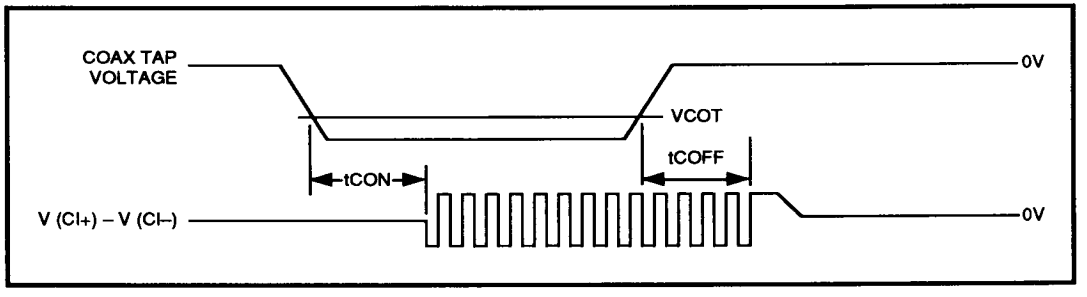
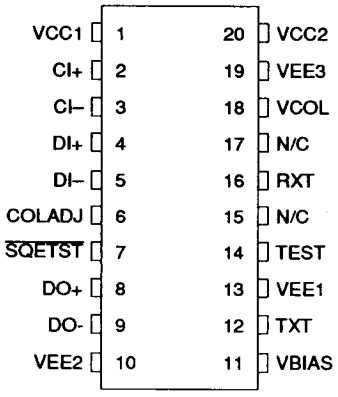


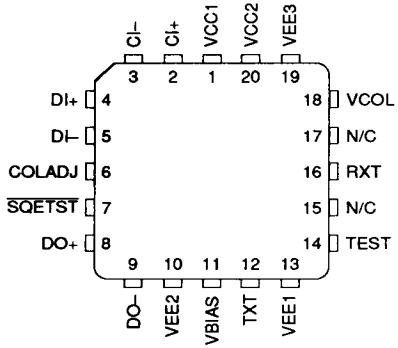
FIGURE 7: Collision Detect Timing

PACKAGE PIN DESIGNATIONS

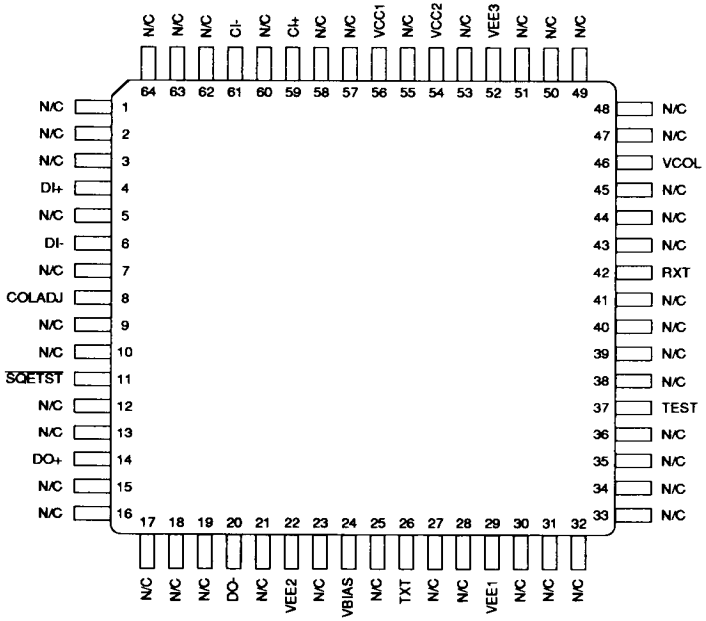
(Top View)



20-Pin DIP



20-Pin PLCC



64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78Q8330		
20-Pin Plastic DIP	78Q8330-CP	78Q8330-CP
20-Pin PLCC	78Q8330-CH	78Q8330-CH
64-Lead TQFP	78Q8330-CGT	78Q8330-CGT
SSI 78Q8330A		
20-Pin Plastic DIP	78Q8330A-CP	78Q8330A-CP
20-Pin PLCC	78Q8330A-CH	78Q8330A-CH
64-Lead TQFP	78Q8330A-CGT	78Q8330A-CGT

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