BA6491FS

3-phase, full-wave, motor driver

The BA6491FS is an IC that can be used to control and drive floppy disk drive spindle motors. This IC uses a 3-phase, full-wave drive system.

With a built-in digital servo, amplifier circuit, and mono-multi circuit, this device has a high performance and can reduce the number of components required in the floppy drive.

Features

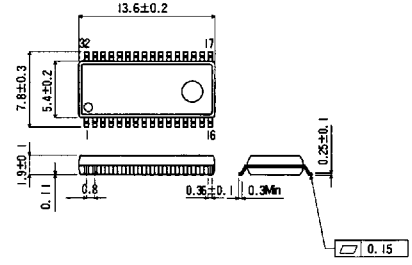
- available in SSOP-P32 package
- oscillator frequency is 1000.8 kHz
- switchable between 300 and 360 rpm
- has an internal index amplifier and mono-multi amplifier. The mono-multi amplifier varies its delay time in response to changes in motor speed
- built-in high performance digital servo circuit
- built-in Hall-effect element power switch
- built-in current limiter and thermal shutdown

Applications

- floppy disk drive

Dimensions (Units : mm)

BA6491FS (SSOP-P32)



Block diagram

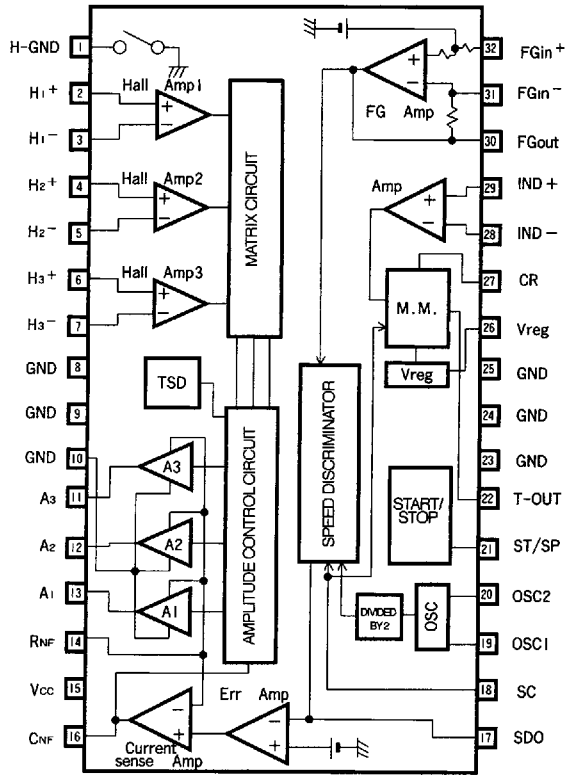


Table 1 Pin description (Sheet 1 of 2)

Pin no.	Pin name	Function
1	H-GND	Hall element bias switch (ground side)
2	H1+	Hall input amplifier 1+ input
3	H1–	Hall input amplifier 1– input
4	H2+	Hall input amplifier 2+ input
5	H2–	Hall input amplifier 2– input
6	H3+	Hall input amplifier 3+ input
7	H3–	Hall input amplifier 3– input

Table 1 Pin description (Sheet 2 of 2)

Pin no.	Pin name	Function
8	GND	Substrate ground
9	GND	
10	GND	Signal, driver ground
11	A_3	Motor output 3
12	A_2	Motor output 2
13	A_1	Motor output 1
14	R_{NF}	Driver voltage supply (current sense pin)
15	V_{CC}	Supply voltage
16	C_{NF}	Error amplifier output phase compensation capacitor
17	SDO	Speed discriminator output, error amplifier input
18	SC	Speed control input
19	OSC1	Oscillator output
20	OSC2	Oscillator input
21	ST/SP	Start/stop control
22	T-OUT	Mono/multi timing output
23	GND	Substrate ground
24	GND	
25	GND	
26	Vreg	Regulated voltage output
27	CR	Connection point for components to set mono/multi timing
28	IND–	Mono/multi input amplifier, inverted input
29	IND+	Mono/multi input amplifier, positive input
30	FGout	FG amplifier output
31	FGin–	FG amplifier, Inverted input
32	FGin+	FG amplifier, positive input

Absolute maximum ratings (T_a = 25°C)

Parameter	Symbol	Limits	Unit	Conditions
Applied voltage	V_{CC}	7.0	V	
Power dissipation	P_d	600	mW	Reduce power by 4.8 mW/°C for each degree above 25°C.
Maximum permissible output current	I_{Omax}	1000	mA	Output current must be such that max P_d or ASO is not exceeded.
Operating temperature range	T_{opr}	−25 ~ +75	°C	
Storage temperature range	Tstg	−55 ~ +150	°C	

Recommended operating conditions (T_a = 25°C)

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	V_{CC}	4.2		6.5	V

Electrical characteristics (unless otherwise noted, T_a = 25°C, V_{CC} = 5 V) (Sheet 1 of 2)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Supply current	I_{CC}	18	23	33	mA	
Stand-by current	I_{st}			3	µA	Pin 21 = 5 V
Hall-in phase input range	V_{HB}	1.5		4.5	V	
Hall amplifier input sensitivity	V_{Hin}	60			mV_{pk-pk}	Differential input
Output saturation voltage	V_{sat}		1.04	1.3	V	I_{out} = 350 mA, total, high, low ends
Speed discriminator high output level	V_{DH}	2.52	2.83	3.14	V	I = 100 µA (sink)
Speed discriminator low output level	V_{DL}	0.72	0.90	1.08	VA	I = 100 µA (source)
Speed discriminator output source current	I_{Dout}	14	20	26	µA	
Speed discriminator output sink current	I_{Din}	14	20	26	µA	
FG amplifier gain	G_{FG}	38.5	42	44.5	dB	f = 300 Hz
Speed discriminator minimum input	V_{FGmi}	2.0			mV_{pk-pk}	In terms of FG amplifier input

Electrical characteristics (unless otherwise noted, T_a = 25°C, V_{CC} = 5 V) (Sheet 2 of 2)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Speed discriminator noise margin	V_{FGnm}			0.5	mV_{pk-pk}	In terms of FG amplifier input
Control input gain	G_{Err}	−14	−11	−8.7	dB	V_{RNF} with respect to $V_{pin\ 17}$ R_{NF} = 0.56 ohms
Oscillator frequency	f_{osc}		1000.8	1100	kHz	
Oscillation frequency accuracy	f_{osc}	−0.2		+0.2	%	f_{OSC} = 1000.8 kHz
Current limiter voltage	V_{CI}	175	205	235	mV	Measured from pin 14 to V_{CC}, R_{NF} = 0.56 Ω
Start/stop input high level voltage	V_{21H}	3.0		5.0	V	Standby state
Start/stop input low level voltage	V_{21L}	0.0		1.5	V	Operating state
Speed switching input high level voltage	V_{18H}	1.5		5.0	V	f_{FG} = 360 Hz (phase locked)
Speed switching input low level voltage	V_{18L}	0.0		1.0	V	f_{FG} = 360 Hz (phase locked)
Hall bias saturation voltage	V_1	1.2	1.5	1.8	V	Pin 1 current = 10 mA
In-phase input voltage	V_{BID}	1.5		4.0	V	
Input offset voltage	V_{osID}	−8	0	+8	mV	
Input hysteresis	V_{hyID}	10		30	mV	
Regulator voltage	V_{reg}	1.8	2.1	2.4	V	
Mono/multi timing certainty	T_1	1.80	2.00	2.20	ms	Pin 18 = LOW
Mono/multi timing certainty	T_2	1.50	1.67	1.83	ms	Pin 18 = HIGH
Mono/multi timing ratio	T_1/T_2	1.15	1.20	1.25		
Output high level voltage	V_{OHID}	3.0	4.0		V	5 mA source current
Output low level voltage	V_{OLID}		0.5	1.0	V	5 mA sink current

Input and output equivalent circuits

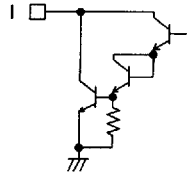


Figure 1 Pin 1

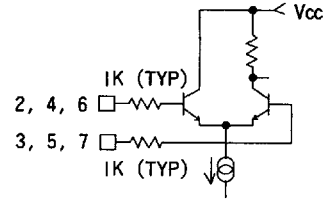


Figure 2 Hall inputs pins 2 ~ 7

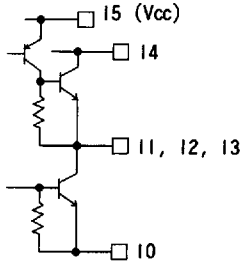


Figure 3 Pin 10 ~ 15

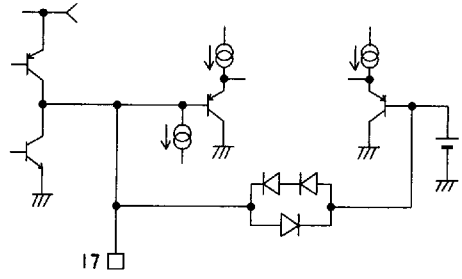


Figure 4 Pin 17

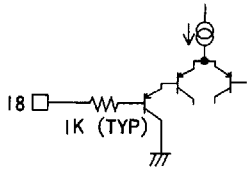


Figure 5 Pin 18

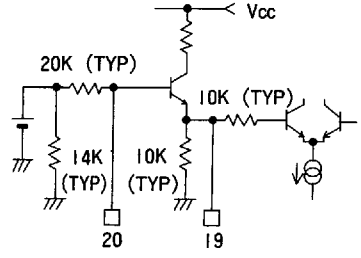


Figure 6 Pins 19 and 20

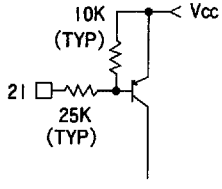


Figure 7 Pin 21

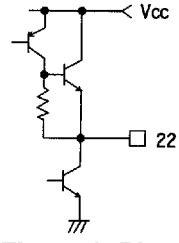


Figure 8 Pin 22

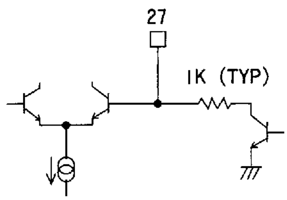


Figure 9 Pin 27

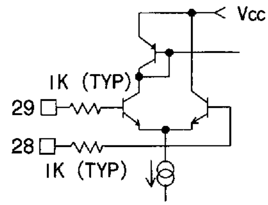


Figure 10 Pin 28 and 29

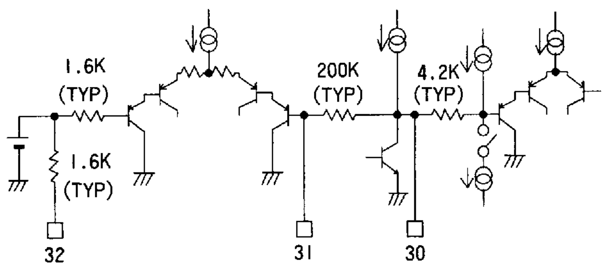


Figure 11 Pins 30 ~ 32

Operation

Motor drive circuit

The motor drive is a three-phase full wave pseudo-linear current drive in which the rotor position is sensed by Hall elements. The motor drive current is sensed measuring the voltage dropped across the small resistor R_{NF} that is in series with the drive current.

The functional blocks that make up the motor drive circuit include the Hall amplifiers, a matrix circuit, an amplitude control circuit, the motor winding drivers, an error amplifier, and a current feedback amplifier, as shown in Figure 12.

Figure 13 shows the phase relationships between the various waveforms in the signal path from the Hall elements to the motor drivers.

The Hall amplifiers receive the voltage signals from the Hall elements as differential signals. The signals are amplified by the Hall amplifiers and output to the matrix circuit (as voltage signals H1, H2, and H3).

Figure 12 Motor drive functional diagram

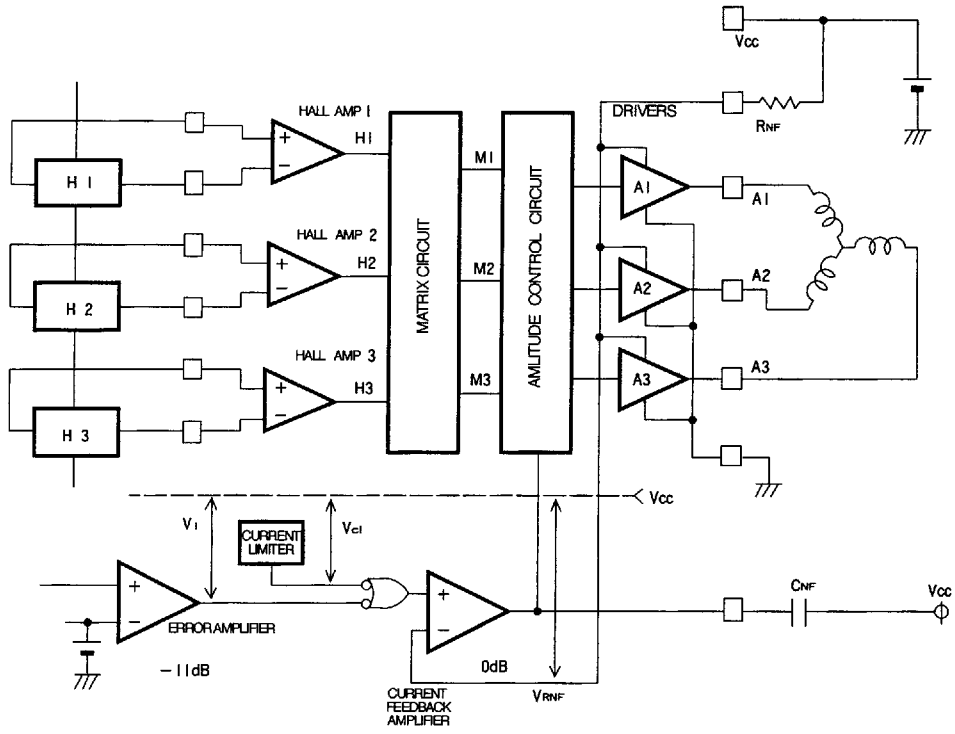
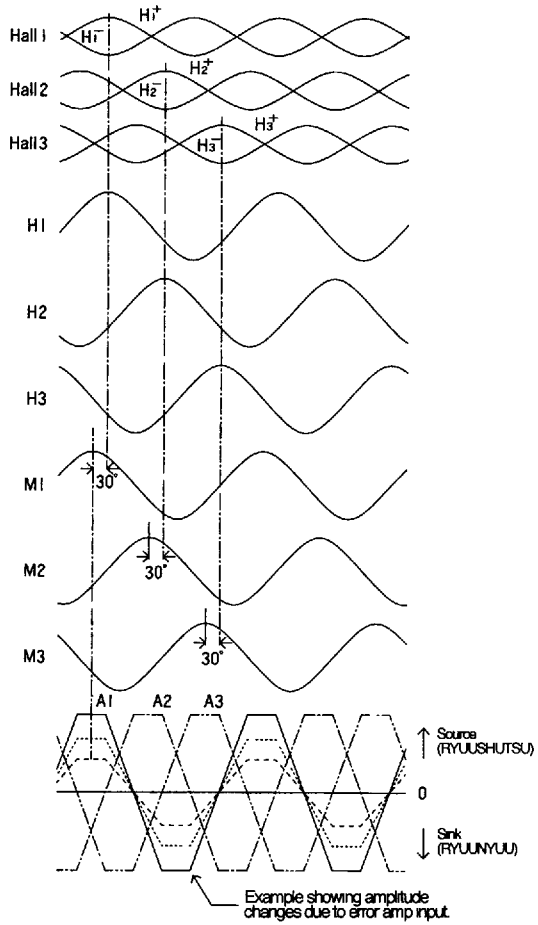


Figure 13 Motor drive signal phase relationships



The matrix circuit combines the three voltage signals H1, H2, and H3 to create the current signals M1, M2, and M3. For example, H2, the Hall amplifier 2 output voltage signal, is subtracted from H1, the Hall amplifier 1 output voltage signal, to create the current signal M1, which, leads H1 by 30 degrees as shown in Figure 13.

M2 and M3 are generated similarly.

In the amplitude control circuit, the amplitudes of M1, M2, and M3 are controlled by the current feedback amplifier signal. Driver amplifiers A1, A2, and A3 amplify the three signals equally to generate the drive waveforms.

The drive current waveforms are "180° on" trapezoidal waveforms, which have low noise and a low total current ripple.

The total drive current is controlled by the error amplifier input voltage. The error amplifier has a gain of -11dB ($E_O = 0.28\ E_I$). V_1 is the error amplifier output voltage, and V_{RNF} is the voltage developed across R_{NF} by the motor drive current.

The current feedback amplifier operates to maintain V_1 and V_{RNF} equal, to control the total drive current.

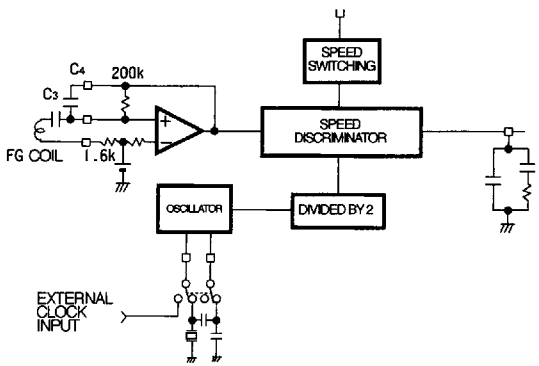
If V_1 exceeds set current limit voltage V_{C1}, V_{C1} takes over as the controlling voltage. This limits the total drive current to a value equal to V_{C1}/R_{NF}.

With total feedback applied to the feedback amplifier, the gain can easily go to 0 dB, causing the feedback loop to go into oscillation. Avoiding this requires that adequate phase compensation be used to reduce the high frequency gain. An external pin is provided to connect a capacitor (C_{NF}) for this purpose.

Speed control circuit

The speed control circuit is a non-adjustable digital servo system that uses a frequency-locked loop (FLL). The circuit, shown in Figure 14, is made up of an oscillator, a divide-by-2 circuit, an FG amplifier, and a speed discriminator.

Figure 14 Speed control equivalent circuit



The internal master clock for the IC can be generated by using an external ceramic resonator and capacitors to complete the IC internal circuit, or by using an external clock source. The clock frequency is halved in the divide-by-2 circuit.

The FG amplifier amplifies the small voltage generated in the motor FG pickup, and shapes the amplified signal to form the rectangular wave speed signal. The FG amplifier gain (G_{FG}) is set at 42 dB (typical) by internal resistors.

C_3 and the internal 1.6 kΩ resistor form a high-pass filter. C_4 and the internal 200 kΩ resistor form a low-pass filter to filter out any noise in the FG signal. (Resistances values are typical values.)

The high-pass and low-pass filter cutoff frequencies (f_H and f_L)are given by the following equations.

$$f_H = \frac{1}{2\pi \times 1.6\ \text{k}\Omega \times C_3}$$

$$f_L = \frac{1}{2\pi \times 200\ \text{k}\Omega \times C_4}$$

C_3 and C_4 are selected such that $f_H < f_{FG} < f_L$

The circuit, as seen at the FG amplifier input, has hysteresis.

The speed discriminator further divides the basic clock to create a reference frequency. The speed discriminator compares the speed signal from the FG amplifier with the reference frequency, and outputs an error pulse corresponding to the difference. The speed of the motor in rpm (N) is determined by the following equation:

$$N = 60 \times \frac{f_{osc}}{n} \times \frac{1}{Z}$$

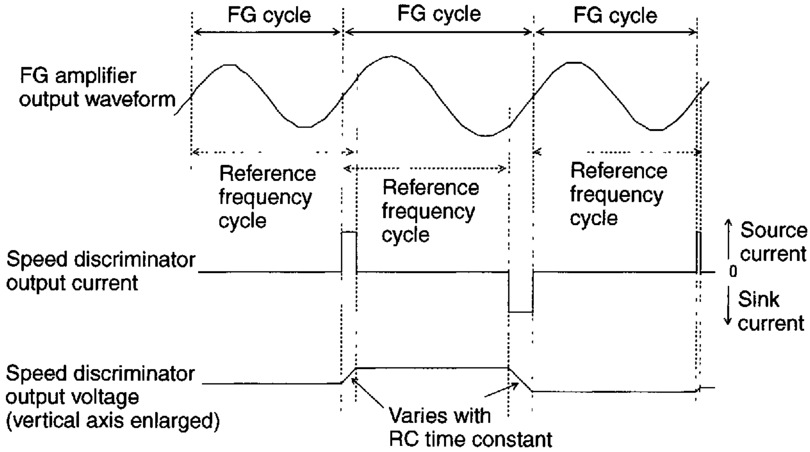
where:
f_{OSC} = reference frequency
n = number of speed discriminator counts x 2
Z = number of FG teeth.

The number of speed discriminator counts depends on the voltage applied to the speed control pin as follows:

Speed control pin	Number of counts
HIGH	1390
LOW	1668

The purpose of the resistor and capacitors connected to the speed discriminator output (Figure 14) is to smooth the error pulses that form the output waveform shown in . This error signal waveform is applied to the error amplifier to control the motor drive circuit, as described previously.

Figure 15 Speed control circuit waveforms



Mono/multi circuit

The mono/multi input amplifier receives a Hall element signal as a differential input and amplifies it. The amplifier has hysteresis.

The mono/multi circuit creates a time delay from the zero-crossing point. The delay can be set as desired by changing the time constant of an external RC network. The delay time is also changed by the speed control pin voltage. The ratio between the delay times for the HIGH and LOW states of the speed control pin is

$T_1/T_2 = 1.2$ (typical),

where:
T_1 = time delay when the speed control pin is LOW
T_2 = time delay when the speed control pin is HIGH.

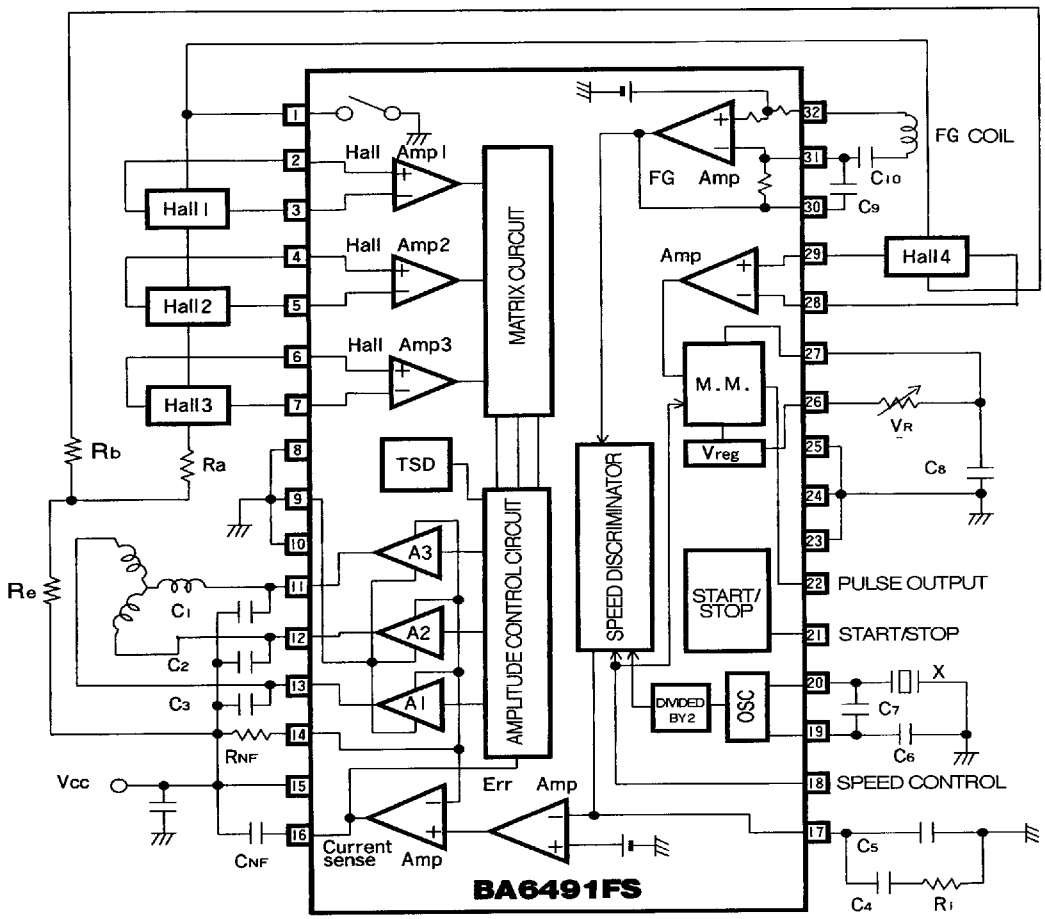
Start/stop circuit

The start/stop circuit puts the IC in the operating state when the START/STOP pin is LOW, and in the standby state when the pin is HIGH. In the standby state, the supply current is almost zero. The Hall element bias switch is linked to the Start/Stop circuit such that the bias switch is opened in the standby mode. This isolates to the Hall elements and stops the motor.

Thermal shutdown

The thermal shutdown (TSD) circuit is an over-temperature protection circuit that turns off IC current when the chip junction temperature rises to approximately 170°C (typical). The TSD resets when the temperature drops below 155°C.

Figure 16 Application example



Precautions for use

Ceramic resonator external circuit constants

The proper values for externally-connected circuit constants depend on the ceramic resonator used. The circuit constants should be decided only after you have determined which manufacturer's resonator you will be using, and have studied the resonator.

The circuit is shown in Figure 16. The decision as to which capacitors to use should be largely based on the precision and temperature characteristics of the capacitors.

External clock oscillator

An external clock can be directly coupled to the OSC2 pin (pin 20). When you use an external clock, ensure that nothing is connected to pin 19 and that the voltage peaks at the OSC2 pin do not exceed the voltage on V_{CC} or fall below ground potential.

Oscillator frequency vs. motor speed

The speed of rotation of the motor (FG amp output, at pin 15) may vary due to variances in integrator circuit constants and the performance characteristics of the motor. You can correct the motor speed to compensate for these variances by adjusting the oscillator frequency. The frequency can be finely adjusted by changing the values of the external capacitors. For detailed information on how to do this, consult the ceramic resonator manufacturer.

Hall element connection methods

Hall elements can be connected in series or parallel. If the elements are connected in series, however, care must be taken not to allow the Hall element output to exceed the Hall in-phase input range (V_{HB}), as listed in the "Electrical characteristics" table.

Hall element input levels

Excessively large signals on the Hall inputs can cause switching noise. The differential input amplitude should be kept to about 100 $mV_{pk\text{-}pk}$ to minimize this effect.

Pins 8, 9, and 23 ~ 25

These pins are all connected to the chip substrate, and also function as cooling fins. They should be connected to the ground pattern.

Electrical characteristic curves

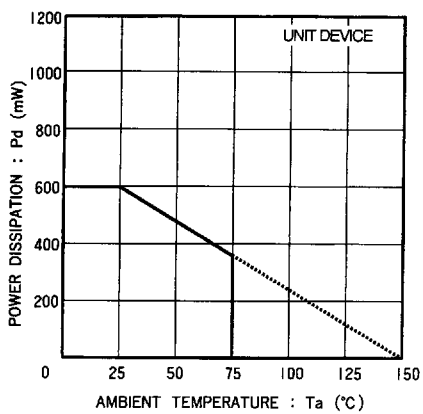


Figure 17

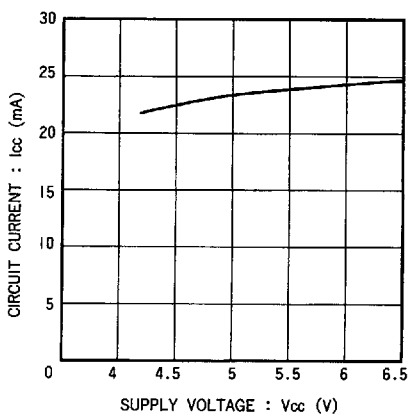


Figure 18

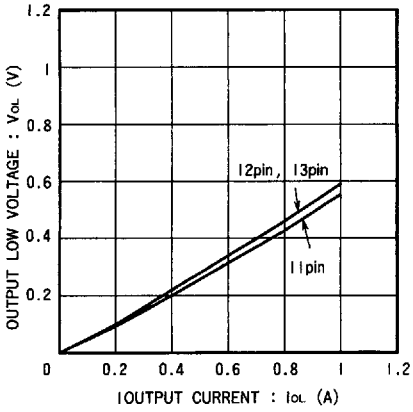


Figure 19

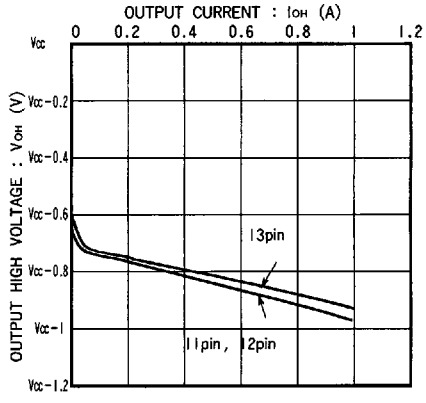


Figure 20

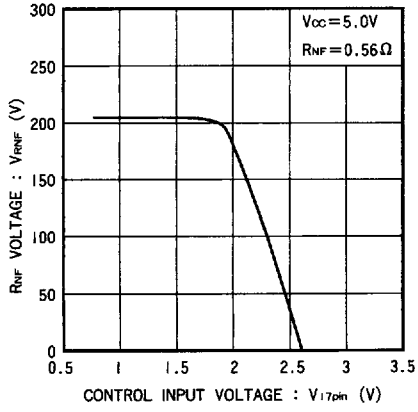


Figure 21