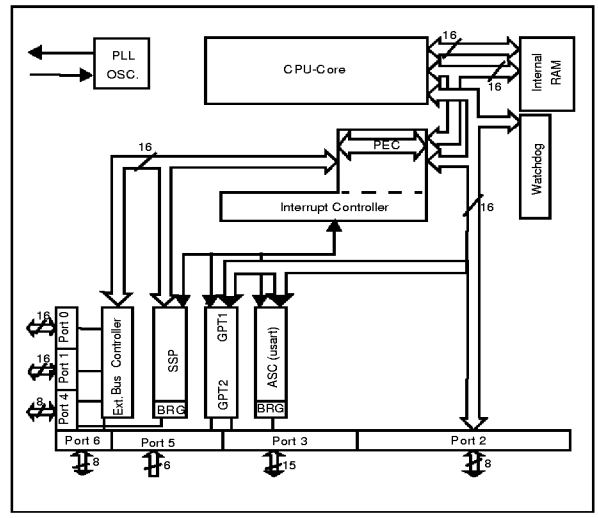
SGS-THOMSON MICROELECTRONICS

ST10R163

16-BIT ROMLESS MICROCONTROLLER

DATASHEET

- High performance 16-bit CPU with 4-stage pipeline
- 80ns instruction cycle time at 25-MHz CPU clock
- 400 ns multiplication (16 × 16 bits), 800 ns division (32 / 16 bit)
- Enhanced boolean bit manipulation facilities
- Additional instructions to support HLL and operating systems
- Register-based design with multiple variable register banks
- Single-cycle context switching support
- Up to 16 MBytes linear address space for code and data (1 MByte with SSP used)
- 1Kbytes on-chip RAM
- Programmable external bus characteristics for different address ranges
- 8-Bit or 16-bit external data bus
- Multiplexed or demultiplexed external address/ data buses
- Five programmable chip-select signals
- Hold- and hold-acknowledge bus arbitration support
- Clock Generation via on-chip PLL or via direct or prescaled clock input
- 1024 bytes on-Chip special function register area
- Idle and power down modes
- 8-channel interrupt-driven single-cycle data transfer facilities via peripheral event controller (PEC)
- 16-priority-level interrupt system with 20 sources, sample-rate down to 40 ns
- Two multi-functional general purpose timer units with 5 timers
- Two serial channels (synchronous/ asynchronous and high-speed-synchronous serial port - SSP)
- Programmable watchdog timer
- Oscillator Watchdog
- Up to 77 general purpose I/O lines



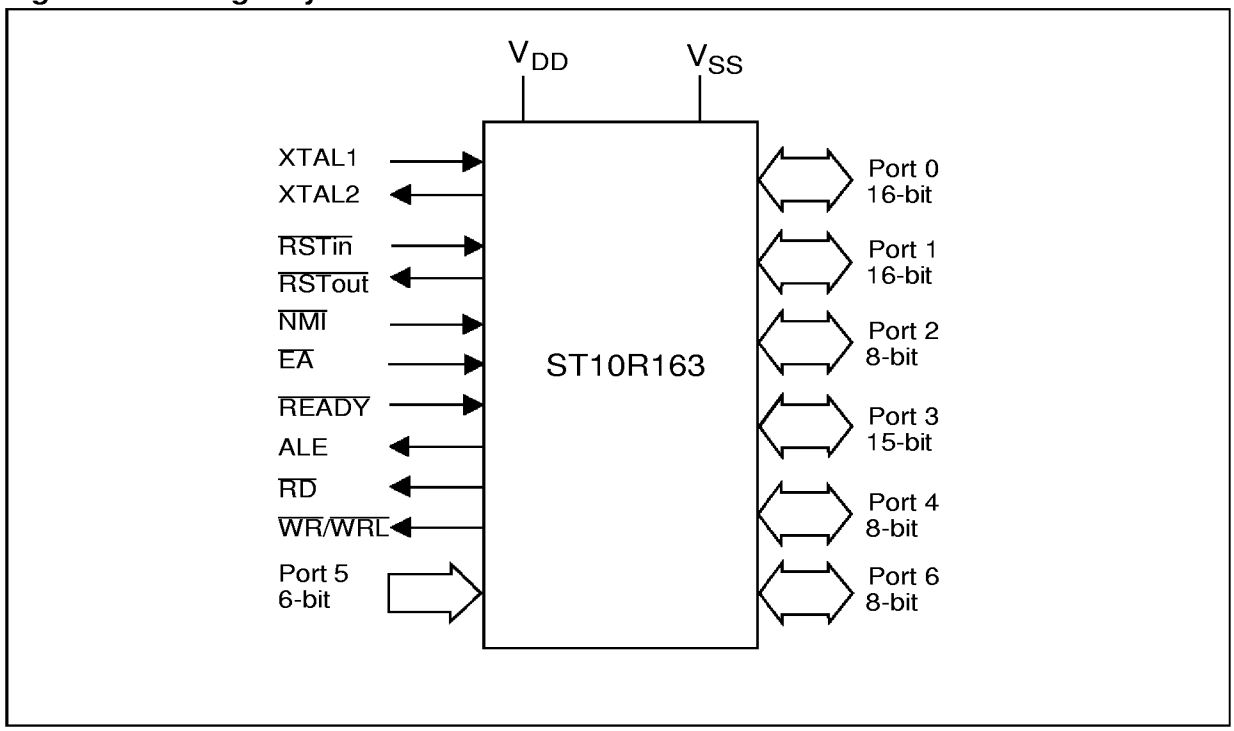
- Supported by a wealth of development tools like C-compilers, macro-assembler packages, emulators, evaluation boards, HLL-debuggers, simulators, logic analyser disassemblers, programming boards
- 100-Pin Thin Quad Flat Pack Package (TQFP)

Table of Contents

1 INTRODUCTION

The ST10R163 is a ROMless derivative of the SGS-THOMSON ST10 family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced IO capabilities.

Figure 1.1 Logic Symbol



2 PIN DATA

Figure 2.1 TQFP Pin Configuration (top view)

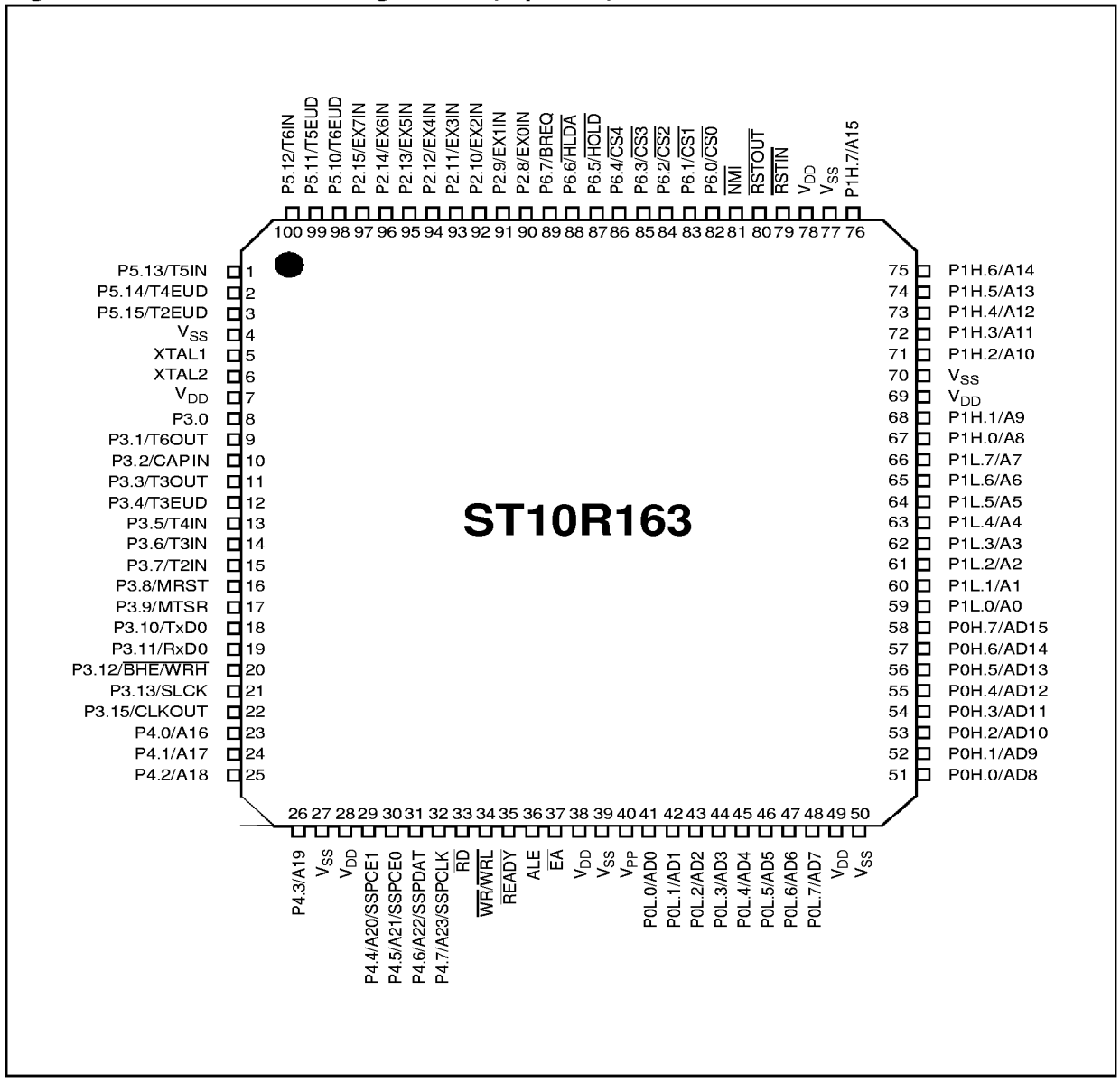


Table 2.1 Pin Definitions and Functions

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
P5.10 – P5.15	98-100 1- 3 98 99 100 1 2 3	I I I I I I I I	Port 5 is a 6-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as timer inputs: P5.10 T6EUD GPT2 Timer T6 Ext.Up/Down Ctrl.Input P5.11 T5EUD GPT2 Timer T5 Ext.Up/Down Ctrl.Input P5.12 T6IN GPT2 Timer T6 Count Input P5.13 T5IN GPT2 Timer T5 Count Input P5.14 T4EUD GPT1 Timer T4 Ext.Up/Down Ctrl.Input P5.15 T2EUD GPT1 Timer T2 Ext.Up/Down Ctrl.Input
XTAL1 XTAL2	5 6	I O	XTAL1:Input to the oscillator amplifier and input to the internal clock generator XTAL2:Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
P3.0 – P3.13, P3.15	8 21 22 9 10 11 12 13 14 15 18 19 20 22	I/O I/O I/O O I O I I I I O I/O O O O	Port 3 is a 15-bit (P3.14 is missing) bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The following Port 3 pins also serve for alternate functions: P3.1 T6OUT GPT2 Timer T6 Toggle Latch Output P3.2 CAPIN GPT2 Register CAPREL Capture Input P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output P3.4 T3EUD GPT1 Timer T3 Ext.Up/Down Ctrl.Input P3.5 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture P3.6 T3IN GPT1 Timer T3 Count/Gate Input P3.7 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture P3.10 T×D0 ASC0 Clock/Data Output (Asyn./Syn.) P3.11 R×D0 ASC0 Data Input (Asyn.) or I/O (Syn.) P3.12 $\overline{BHE}$ Ext. Memory High Byte Enable Signal, $\overline{WRH}$ Ext. Memory High Byte Write Strobe P3.15 CLKOUTSystem Clock Output (=CPU Clock)

Table 2.1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
P4.0 – P4.7	23-26 29-32-	I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 can be used to output the segment address lines:
	23	O	P4.0 A16 Least Significant Segment Addr. Line
	...	...	... ...
	26	O	P4.3 A19 Segment Address Line
	29	O	P4.4 A20 Segment Address Line,
		O	SSPCE1 SSP Chip Enable Line 1
	30	O	P4.5 A21 Segment Address Line,
		O	SSPCE0 SSP Chip Enable Line 0
	31	O	P4.6 A22 Segment Address Line,
		I/O	SSPDAT SSP Data Input/Output Line
	32	O	P4.7 A23 Most Significant Segment Addr. Line
		O	SSPCLK SSP Clock Output Line
$\overline{RD}$	33	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/$\overline{WRL}$	34	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	35	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level.
ALE	36	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	37	I	External Access Enable pin. A low level at this pin during and after Reset forces the ST10R163 to begin instruction execution out of external memory. A high level forces execution out of the internal ROM. The ST10R163 must have this pin tied to '0'.

Table 2.1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
PORT0: P0L.0 – P0L.7, P0H.0 - P0H.7	41 48 51 58	I/O	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** • Data Path Width: 8-bit 16-bit • P0L.0 – P0L.7: D0 – D7 D0 - D7 • P0H.0 – P0H.7: I/O D8 - D15 **Multiplexed bus modes:** • Data Path Width: 8-bit 16-bit • P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 • P0H.0 – P0H.7: A8 - A15 AD8 - AD15
PORT1: P1L.0 – P1L.7, P1H.0 - P1H.7	59 66 67 - 68 71 - 76	I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.
$\overline{\text{RSTIN}}$	79	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10R163. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
$\overline{\text{RSTOUT}}$	80	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	81	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the ST10R65 to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.

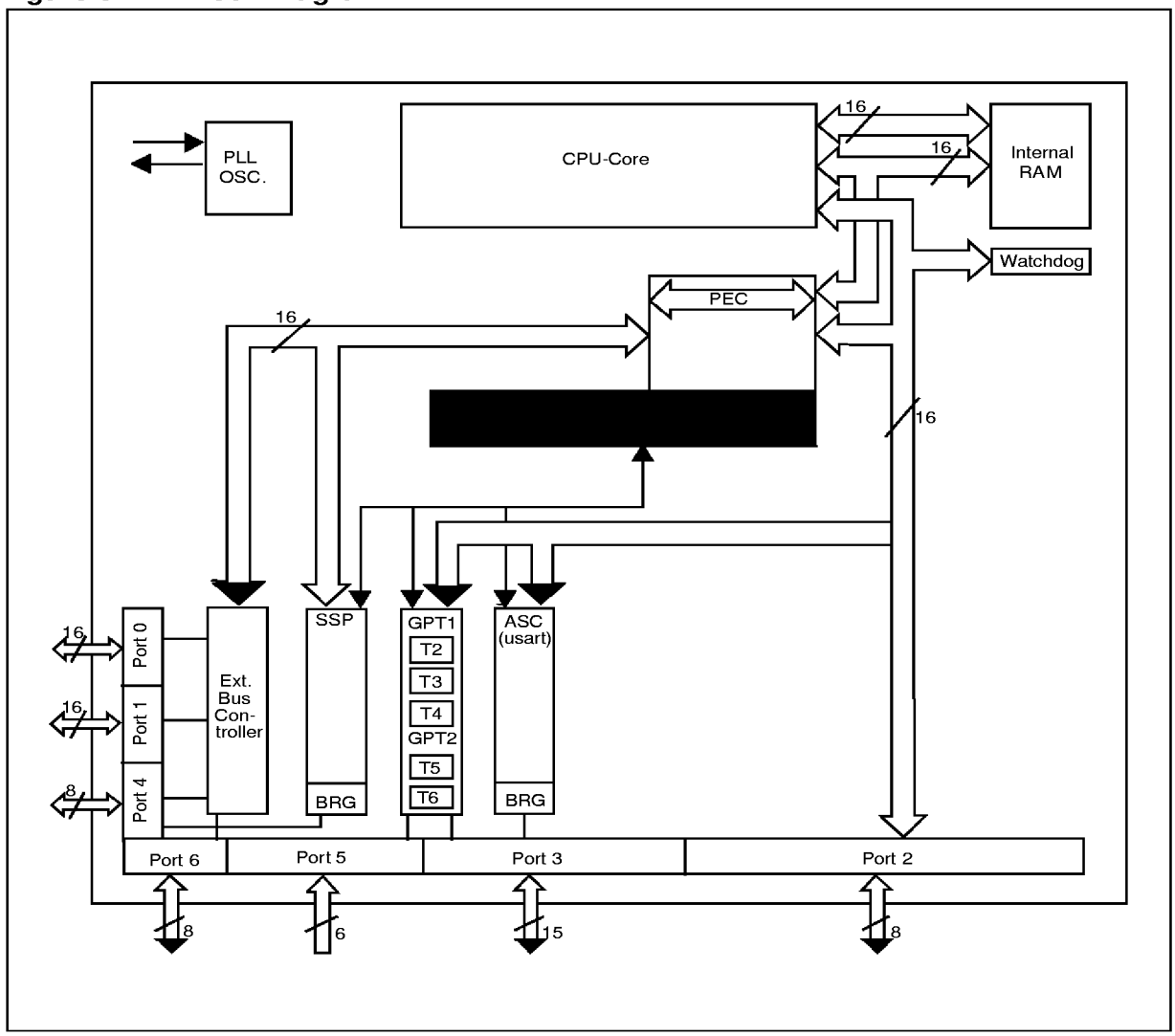
Table 2.1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Function
P6.0 – P6.7	82 - 89	I/O	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins also serve for alternate functions:
	82	O	P6.0 $\overline{CS0}$ Chip Select 0 Output
	...	...	... ...
	86	O	P6.4 $\overline{CS4}$ Chip Select 4 Output
	87	I	P6.5 $\overline{HOLD}$ External Master Hold Request Input (Master mode: O, Slave mode: I)
	88	I/O	P6.6 $\overline{HLDA}$ Hold Acknowledge Output
	89	O	P6.7 $\overline{BREQ}$ Bus Request Output
P2.8 – P2.15	90 - 97	I/O	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins also serve for alternate functions:
	90	I	P2.8 EX0IN Fast External Interrupt 0 Input
	...	...	... ...
	97	I	P2.15 EX7IN Fast External Interrupt 7 Input
V_{PP} / OWE	40	-	Flash programming voltage / Oscillator Watchdog Enable. This pin accepts the programming voltage for flash versions of the ST10R163. For compatibility, during normal operation this pin must be connected to V_{CC}. It also enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pullup device holds this input high if nothing is driving it (e.g. on non-flash devices).
V_{DD}	7, 28, 38, 49, 69, 78	-	Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode
V_{SS}	4, 27, 39, 50, 70, 77	-	Digital Ground.

3 FUNCTIONAL DESCRIPTION

The architecture of the ST10R163 combines the advantages of both RISC and CISC processors and an advanced peripheral subsystem. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the ST10R163.

Figure 3.1 Block Diagram



4 MEMORY ORGANIZATION

The memory space of the ST10R163 is configured in a Von Neumann architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have been made directly bit addressable.

The ST10R163 is able to incorporate on-chip mask-programmable ROM for code or constant data. No ROM is integrated on-chip.

1 KByte of on-chip RAM is provided as storage for user defined variables, the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, ..., RL7, RH7) General Purpose Registers (GPRs).

1024 bytes (2 * 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for other, future members of the ST10 family.

In order to meet the needs of system designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

5 EXTERNAL BUS CONTROLLER

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). This can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input or output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the choice of a wide range of different types of memories and external peripherals. In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which allow to access different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported via a particular 'Ready' function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration so that external resources can be shared with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register SYSCON. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output.

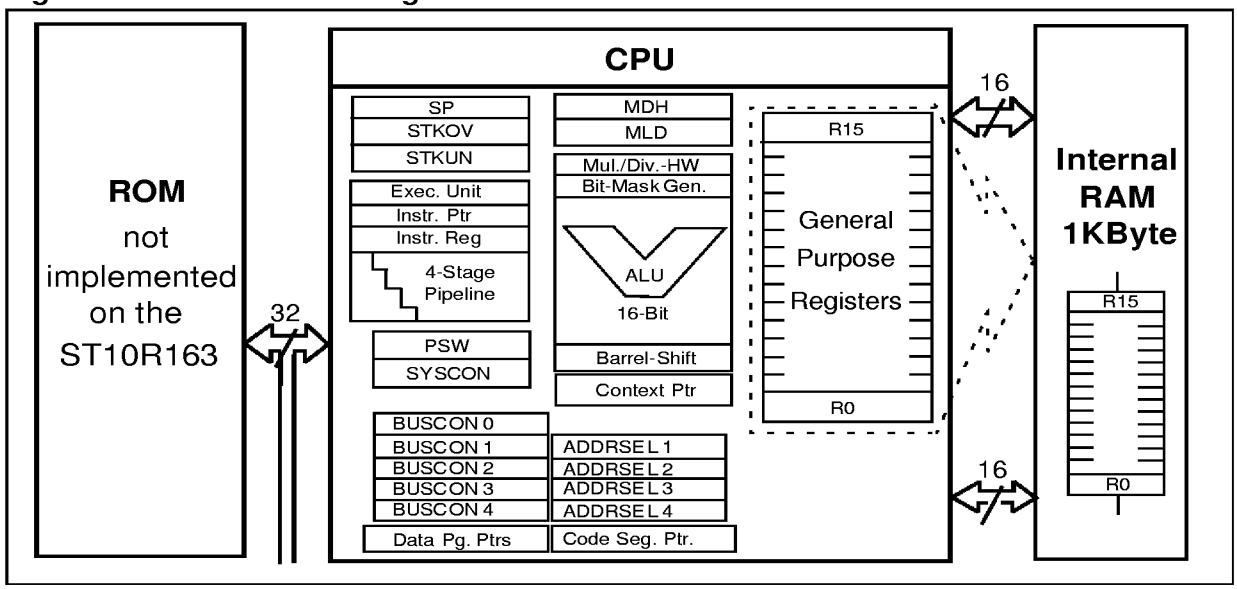
By setting bit DP6.7 to '1' the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, the address space can be restricted to 1 MByte, 256 KByte or to 64 KByte. In this case Port 4 outputs four, two or no address lines at all. If an address space of 16 MBytes is used, it outputs all 8 address lines,.

Note: When the on-chip SSP Module is to be used the, segment address output on Port 4 must be limited to 4 bits (i.e. A19...A16) in order to enable the alternate function of the SSP interface pins.

6 CENTRAL PROCESSING UNIT (CPU)

Figure 6.1 CPU Block Diagram



The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been added for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the ST10R163's instructions can be executed in one machine cycle which requires 80ns at 25MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized for speed: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the 'Jump Cache', reduces the execution time of repeatedly performed jumps in a loop, from 2 cycles to 1 cycle.

The CPU includes an actual register context. This consists of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at a time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are compared against the stack pointer value during each stack access to detect stack overflow or underflow.

A highly efficient instruction set allows maximum use of the CPU. The instruction set is classified in the following groups.

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instruction
- Compare and Loop Control Instruction
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes exist.

7 INTERRUPT SYSTEM

With an interrupt response time from 250 ns to 600 ns (in the case of internal program execution), the ST10R163 reacts quickly to the occurrence of non-deterministic events.

The architecture of the ST10R163 supports several mechanisms for fast and flexible response to the service requests that can be generated from various sources, internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced, either by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In a standard interrupt service, program execution is suspended and a branch to the interrupt service routine is performed. For a PEC service, just one cycle is 'stolen' from the current CPU activity. A PEC service is a single, byte or word data transfer between any two memory locations, with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is decremented for each PEC service, except in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are very well suited, for example, to the transmission or reception of blocks of data. The ST10R163 has 8 PEC channels, each of which offers fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield, exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher priority service request. For standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs, feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by the 'TRAP' instruction, in combination with an individual trap (interrupt) number.

The following table shows all of the possible ST10R163 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Table 7.1 List of Possible Interrupt Sources, Flags, Vector and Trap Numbers

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	00'0060h	18h
External Interrupt 1	CC9IR	CC9IE	CC9INT	00'0064h	19h
External Interrupt 2	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
External Interrupt 3	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
External Interrupt 4	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
External Interrupt 5	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
External Interrupt 6	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
External Interrupt 7	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009Ch	27h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00ACh	2Bh
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0h	2Ch
SSP Interrupt	XPIIR	XPIIE	XPINT	00'0104h	41h
PLL Unlock / OWD	XP3IR	XP3IE	XP3INT	00'010Ch	43h

The ST10R163 also provides an excellent mechanism to identify and process exceptions or error conditions that arise during run-time, 'Hardware Traps'. Hardware traps cause an immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can not normally be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Table 7.2 List of Possible Exceptions or Error Conditions in Run Time

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions:					
•Hardware Reset		RESET	00'0000h	00h	III
•Software Reset		RESET	00'0000h	00h	III
•Watchdog Timer Overflow		RESET	00'0000h	00h	III
Class A Hardware Traps:					
•Non-Maskable Interrupt	NMI	NMITRAP	00'0008h	02h	II
•Stack Overflow	STKOF	STOTRAP	00'0010h	04h	II
•Stack Underflow	STKUF	STUTRAP	00'0018h	06h	II
Class B Hardware Traps:					
•Undefined Opcode	UNDOPC	BTRAP	00'0028h	0Ah	I
•Protected Instruction Fault	PRTFLT	BTRAP	00'0028h	0Ah	I
•Illegal Word Operand Access	ILLOPA	BTRAP	00'0028h	0Ah	I
•Illegal Instruction Access	ILLINA	BTRAP	00'0028h	0Ah	I
•Illegal External Bus Access	ILLBUS	BTRAP	00'0028h	0Ah	I
Reserved			[2Ch – 3Ch]	[0Bh – 0Fh]	
Software Traps •TRAP Instruction			Any [00'0000h-00'01FCh] in steps of 4h	Any [00h – 7Fh]	Current CPU Priority

8 GENERAL PURPOSE TIMER (GPT) UNIT

The GPT unit is a flexible multifunctional timer/ counter structure. It may be used for many different time-related tasks such as: event timing and counting, pulse width and duty cycle measurements, pulse generation or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer, in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of module GPT1 can be configured individually for one of three basic modes of operation: Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. Counter Mode allows a timer to be clocked in reference to external events. Pulse width or duty cycle measurement is supported in Gated Timer Mode where the operation of a timer is controlled by the 'gate' level on an external input pin. Each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 320ns (@ 25MHz CPU clock).

The count direction (up/down) for each timer is programmable by software or may be altered dynamically by an external signal on a port pin (TxEUD) to facilitate, for example, position tracking.

Timers T3 and T4 have output toggle latches (TxOTL) which change their state on each timer overflow/underflow. The state of these latches may be output on port pins (TxOUT) for time-out monitoring by external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 are captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered, either by an external signal, or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

With its maximum resolution of 160 ns (@ 20MHz), the GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

Figure 8.1 Block Diagram of GPT1

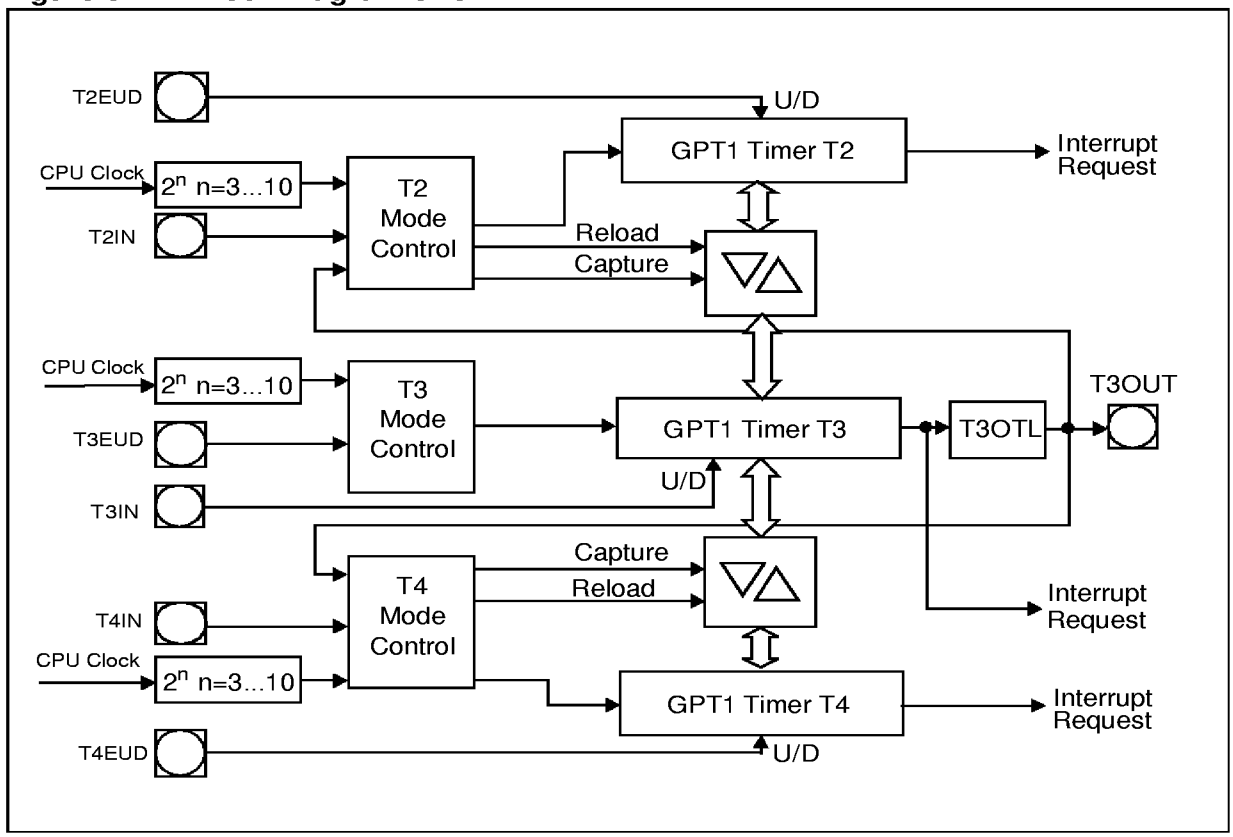
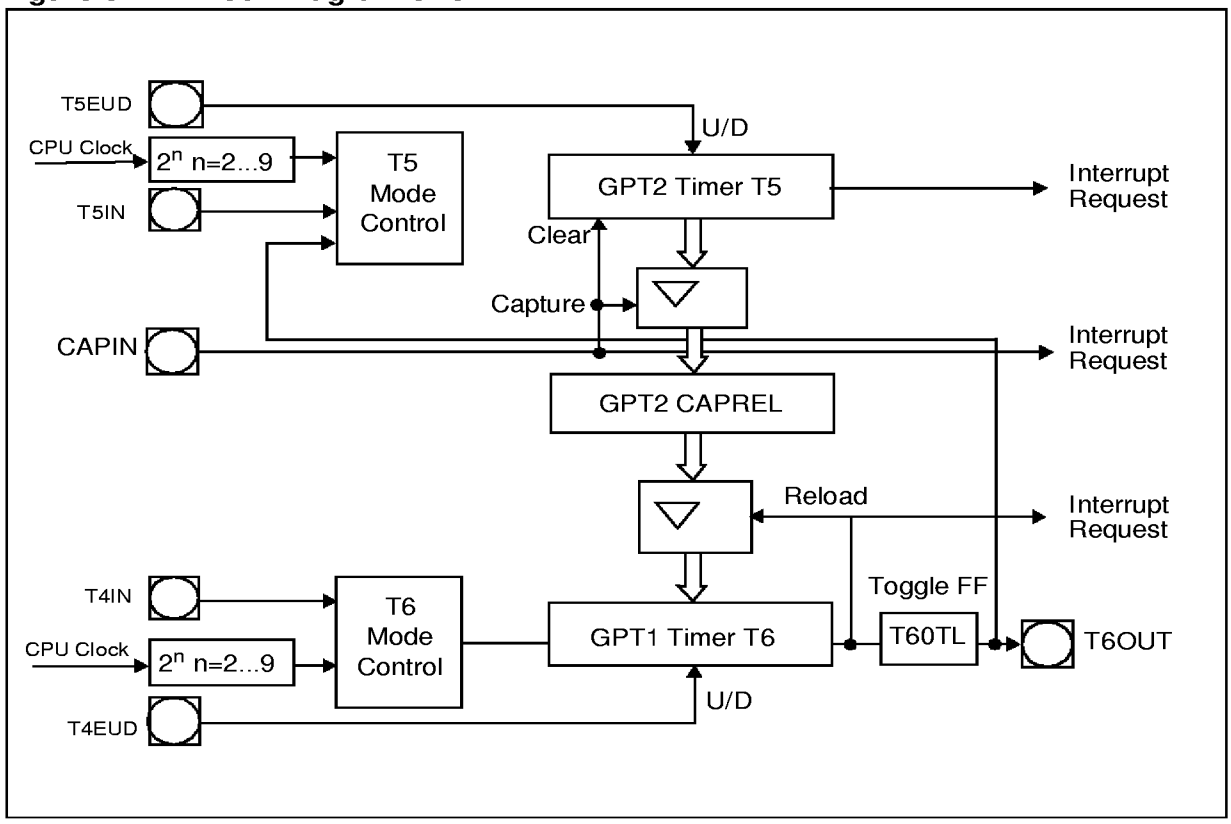


Figure 8.2 Block Diagram of GPT2



9 PARALLEL PORTS

The ST10R163 provides up to 77 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation, or via the control registers for open-drain operation. During the internal reset, all port pins are configured as inputs.

All port lines have associated, programmable, alternate, input or output functions. PORT0 and PORT1 may be used as address and data lines for external memory access. Port 4 outputs the additional segment address bits A23/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional bus arbitration signals ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) and chip select signals. Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{BHE}$ and the system clock output (CLKOUT). Port 5 is used for timer control signals. All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

10 SERIAL CHANNELS

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces, an Asynchronous/Synchronous Serial Channel (ASC0) and a Synchronous Serial Port (SSP).

ASC0 is upward compatible with the serial ports of the Siemens SAB 8051x microcontroller family. It supports full-duplex asynchronous communication up to 625 KBaud and half-duplex synchronous communication up to 6.25 Mbaud (3.125 Mbaud on the ASC0) @ 25-MHz system clock.

A dedicated baud rate generator makes it possible to set up all standard baud rates without oscillator tuning. For transmission, reception, and erroneous reception, 3 separate interrupt vectors are provided for ASC0. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.
A number of optional hardware error detection capabilities have been included to increase the reliability of data transfers. A parity bit can be generated automatically on transmission or checked on reception. Framing error detection recognizes data frames with missing stop bits. An overrun error is generated if the last character received was not read out of the receive buffer register at the time the reception of a new character is complete.

The SSP transmits 1...3 bytes, or receives 1 byte, after synchronously sending 1...3 bytes to a shift clock which is generated by the SSP. The SSP can start shifting with the LSB or with the MSB and selects shifting and latching clock edges as well as the clock polarity. To direct data transfers to one or both of two peripheral devices, up to two chip select lines may be activated.

One general interrupt vector is provided for the SSP.

11 WATCHDOG TIMER

The Watchdog Timer is a fail-safe mechanism. It limits the maximum malfunction time of the controller

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. In this way the chip's start-up procedure is always monitored. The software must be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a pre-specified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Therefore, time intervals between 20 µs and 336 ms can be monitored (@ 25 MHz). The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

12 OSCILLATOR WATCHDOG

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock / OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

A low level on pin OWE disables the OWD's interrupt output so the clock signal is derived from the oscillator clock in any case.

Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.

13 INSTRUCTION SET SUMMARY

The table below lists the instruction set of the ST10R163. More detailed information such as address modes, instruction operation, parameters for conditional execution of instructions, opcodes and a detailed description of each instruction can be found in the **"ST10 Programming Manual"**.

Table 13.1 Instruction Set

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4

Table 13.1 Instruction Set (cont'd)

Mnemonic	Description	Bytes
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on $\overline{\text{RSTOUT}}$ pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

14 SPECIAL FUNCTION REGISTER OVERVIEW

The following table lists all ST10R163 SFRs. The list is in alphabetical order.

Bit-addressable SFRs are marked with "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers with on chip X-Peripherals (CAN) are marked with the letter "X" in the column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 14.1 Special Function Register List

Name	Physical Address	8-Bit Address	Description	Reset Value
ADDRSEL1	FE18h	0Ch	Address Select Register 1	0000h
ADDRSEL2	FE1Ah	0Dh	Address Select Register 2	0000h
ADDRSEL3	FE1Ch	0Eh	Address Select Register 3	0000h
ADDRSEL4	FE1Eh	0Fh	Address Select Register 4	0000h
BUSCON0b	FF0Ch	86h	Bus Configuration Register 0	0XX0h
BUSCON1b	FF14h	8Ah	Bus Configuration Register 1	0000h
BUSCON2b	FF16h	8Bh	Bus Configuration Register 2	0000h
BUSCO3 b	FF18h	8Ch	Bus Configuration Register 3	0000h
BUSCO4 b	FF1Ah	8Dh	Bus Configuration Register 4	0000h
CAPREL	FE4Ah	25h	GPT2 Capture/Reload Register	0000h
CC8IC b	FF88h	C4h	EX0IN Interrupt Control Register	0000h
CC9IC b	FF8Ah	C5h	EX1IN Interrupt Control Register	0000h
CC10IC b	FF8Ch	C6h	EX2IN Interrupt Control Register	0000h
CC11IC b	FF8Eh	C7h	EX3IN Interrupt Control Register	0000h
CC12IC b	FF90h	C8h	EX4IN Interrupt Control Register	0000h
CC13IC b	FF92h	C9h	EX5IN Interrupt Control Register	0000h
CC14IC b	FF94h	CAh	EX6IN Interrupt Control Register	0000h
CC15IC b	FF96h	CBh	EX7IN Interrupt Control Register	0000h
CP	FE10h	08h	CPU Context Pointer Register	FC00h
CRIC b	FF6Ah	B5h	GPT2 CAPREL Interrupt Control Register	0000h
CSP	FE08h	04h	CPU Code Segment Pointer Register (read only)	0000h
DP0L b	F100h **E**	80h	P0L Direction Control Register	00h
DP0H b	F102h **E**	81h	P0h Direction Control Register	00h
DP1L b	F104h **E**	82h	P1L Direction Control Register	00h
DP1H b	F106h **E**	83h	P1h Direction Control Register	00h

Table 14.1 Special Function Register List (cont'd)

Name	Physical Address	8-Bit Address	Description	Reset Value
DP2 b	FFC2h	E1h	Port 2 Direction Control Register	00--h
DP3 b	FFC6h	E3h	Port 3 Direction Control Register	0000h
DP4 b	FFCAh	E5h	Port 4 Direction Control Register	00h
DP6 b	FFCEh	E7h	Port 6 Direction Control Register	00h
DPP0	FE00h	00h	CPU Data Page Pointer 0 Register (10 bits)	0000h
DPP1	FE02h	01h	CPU Data Page Pointer 1 Register (10 bits)	0001h
DPP2	FE04h	02h	CPU Data Page Pointer 2 Register (10 bits)	0002h
DPP3	FE06h	03h	CPU Data Page Pointer 3 Register (10 bits)	0003h
EXICON b	F1C0h **E**	E0h	External Interrupt Control Register	0000h
MDC b	FF0Eh	87h	CPU Multiply Divide Control Register	0000h
MDH	FE0Ch	06h	CPU Multiply Divide Register – High Word	0000h
MDL	FE0Eh	07h	CPU Multiply Divide Register – Low Word	0000h
ODP2 b	F1C2h **E**	E1h	Port 2 Open Drain Control Register	00--h
ODP3 b	F1C6h **E**	E3h	Port 3 Open Drain Control Register	0000h
ODP6 b	F1CEh **E**	E7h	Port 6 Open Drain Control Register	00h
ONES	FF1Eh	8Fh	Constant Value 1's Register (read only)	FFFFh
P0L b	FF00h	80h	Port 0 Low Register (Lower half of PORT0)	00h
P0H b	FF02h	81h	Port 0 High Register (Upper half of PORT0)	00h
P1L b	FF04h	82h	Port 1 Low Register (Lower half of PORT1)	00h
P1H b	FF06h	83h	Port 1 High Register (Upper half of PORT1)	00h
P2 b	FFC0h	E0h	Port 2 Register (8 bits)	00--h
P3 b	FFC4h	E2h	Port 3 Register	0000h
P4 b	FFC8h	E4h	Port 4 Register (8 bits)	00h
P5 b	FFA2h	D1h	Port 5 Register (read only)	XXXXh
P6 b	FFCCh	E6h	Port 6 Register (8 bits)	00h
PECC0	FEC0h	60h	PEC Channel 0 Control Register	0000h
PECC1	FEC2h	61h	PEC Channel 1 Control Register	0000h
PECC2	FEC4h	62h	PEC Channel 2 Control Register	0000h
PECC3	FEC6h	63h	PEC Channel 3 Control Register	0000h
PECC4	FEC8h	64h	PEC Channel 4 Control Register	0000h
PECC5	FECAh	65h	PEC Channel 5 Control Register	0000h
PECC6	FECCh	66h	PEC Channel 6 Control Register	0000h
PECC7	FECEh	67h	PEC Channel 7 Control Register	0000h

Table 14.1 Special Function Register List (cont'd)

Name	Physical Address	8-Bit Address	Description	Reset Value
PSW b	FF10h	88h	CPU Program Status Word	0000h
RP0H b	F108h **E**	84h	System Start-up Configuration Register (Rd. only)	XXh
S0BG	FEB4h	5Ah	Serial Channel 0 Baud Rate Generator Reload Register	0000h
S0CON b	FFB0h	D8h	Serial Channel 0 Control Register	0000h
S0EIC b	FF70h	B8h	Serial Channel 0 Error Interrupt Control Register	0000h
S0RBUF	FEB2h	59h	Serial Channel 0 Receive Buffer Register (read only)	XXh
S0RIC b	FF6Eh	B7h	Serial Channel 0 Receive Interrupt Control Register	0000h
S0TBIC b	F19Ch **E**	CEh	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000h
S0TBUF	FEB0h	58h	Serial Channel 0 Transmit Buffer Register (write only)	00h
S0TIC b	FF6Ch	B6h	Serial Channel 0 Transmit Interrupt Control Register	0000h
SP	FE12h	09h	CPU System Stack Pointer Register	FC00h
SSPCON0	EF00h **X**	---	SSP Control Register 0	0000h
SSPCON1	EF02h **X**	---	SSP Control Register 1	0000h
SSPRTB	EF04h **X**	---	SSP Receive/Transmit Buffer	XXXXh
SSPTBH	EF06h **X**	---	SSP Transmit Buffer High	XXXXh
STKOV	FE14h	0Ah	CPU Stack Overflow Pointer Register	FA00h
STKUN	FE16h	0Bh	CPU Stack Underflow Pointer Register	FC00h
SYSCON b	FF12h	89h	CPU System Configuration Register	0xx0h[1)]
T2	FE40h	20h	GPT1 Timer 2 Register	0000h
T2CON b	FF40h	A0h	GPT1 Timer 2 Control Register	0000h
T2IC b	FF60h	B0h	GPT1 Timer 2 Interrupt Control Register	0000h
T3	FE42h	21h	GPT1 Timer 3 Register	0000h
T3CON b	FF42h	A1h	GPT1 Timer 3 Control Register	0000h
T3IC b	FF62h	B1h	GPT1 Timer 3 Interrupt Control Register	0000h
T4	FE44h	22h	GPT1 Timer 4 Register	0000h
T4CON b	FF44h	A2h	GPT1 Timer 4 Control Register	0000h
T4IC b	FF64h	B2h	GPT1 Timer 4 Interrupt Control Register	0000h

Table 14.1 Special Function Register List (cont'd)

Name	Physical Address	8-Bit Address	Description	Reset Value
T5	FE46h	23h	GPT2 Timer 5 Register	0000h
T5CON b	FF46h	A3h	GPT2 Timer 5 Control Register	0000h
T5IC b	FF66h	B3h	GPT2 Timer 5 Interrupt Control Register	0000h
T6	FE48h	24h	GPT2 Timer 6 Register	0000h
T6CON b	FF48h	A4h	GPT2 Timer 6 Control Register	0000h
T6IC b	FF68h	B4h	GPT2 Timer 6 Interrupt Control Register	0000h
TFR b	FFACh	D6h	Trap Flag Register	0000h
WDT	FEAEh	57h	Watchdog Timer Register (read only)	0000h
WDTCON	FFAEh	D7h	Watchdog Timer Control Register	000xh[2)]
XP1IC b	F18Eh **E**	C7h	SSP Interrupt Control Register	0000h
XP3IC b	F19Eh **E**	CFh	PLL unlock Interrupt Control Register	0000h
ZEROS b	FF1Ch	8Eh	Constant Value 0's Register (read only)	0000h

Notes 1:The system configuration is selected during reset.
2:Bit WDTR indicates a watchdog timer triggered reset.

15 ELECTRICAL CHARACTERISTICS

15.1 Absolute Maximum Ratings

- Ambient temperature under bias (T_A): . . . . . 0 to +70 °C
- Storage temperature (T_{ST}): . . . . . – 65 to +150 °C
- Voltage on V_{DD} pins with respect to ground (V_{SS}): . . . . . – 0.5 to +6.5 V
- Voltage on any pin with respect to ground (V_{SS}): . . . . . –0.5 to V_{DD} +0.5 V
- Input current on any pin during overload condition: . . . . . –10 to +10 mA
- Absolute sum of all input currents during overload condition: . . . . . |100 mA|
- Power dissipation: . . . . . 1.5 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN}>V_{DD}$ or $V_{IN}<V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

15.2 Parameter Interpretation

The parameters listed in the Electrical Characteristics tables, 15.1 to 15.8, represent the characteristics of the ST10R163 and its demands on the system.

Where the ST10R163 logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics, is included in the "Symbol" column.

Where the external system must provide signals with their respective timing characteristics to the ST10R163, the symbol "SR" for System Requirement, is included in the "Symbol" column.

15.3 DC Characteristics

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, f_{CPU} = 25 MHz, Reset active T_A = 0 to +70 °C

Table 15.1 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	V_{IL} SR	– 0.5	0.2 V_{DD} – 0.1	V	–
Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	V_{IH} SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage $\overline{RSTIN}$	V_{IH1} SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2} SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OL} CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	V_{OL1} CC	–	0.45	V	I_{OL1} = 1.6 mA
Output high voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} CC	0.9 V_{DD} 2.4	–	V	I_{OH} = – 500 µA I_{OH} = – 2.4 mA
Output high voltage [1] (all other outputs)	V_{OH1} CC	0.9 V_{DD} 2.4	–	V V	I_{OH} = – 250 µA I_{OH} = – 1.6 mA
Input leakage current	I_{OZ2} CC	–	±500	nA	0 V < V_{IN} < V_{DD}
$\overline{RSTIN}$ pull-up resistor	R_{RST} CC	50	150	kΩ	–
Read/Write inactive current [4]	I_{RWH} [2]	–	-40	µA	V_{OUT} = 2.4 V
Read/Write active current [4]	I_{RWL} [3]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [4]	I_{ALEL} [2]		40	µA	V_{OUT} = V_{OLmax}
ALE active current [4]	I_{ALEH} [3]	500		µA	V_{OUT} = 2.4 V
Port 6 inactive current [4]	I_{P6H} [2]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current [4]	I_{P6L} [3]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current [4]	I_{P0H} [2]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L} [3]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance [5] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current	I_{CC}	–	10 + 3.5* f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz] [6]

Table 15.1 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Idle mode supply current	I_{ID}	–	$2 + 1.1 * f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] 6)
Power-down mode supply current	I_{PD}	–	60	µA	$V_{DD} = 5.5$ V 7)

Notes 1:This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2:The maximum current may be drawn while the respective signal line remains inactive.

3:The minimum current must be drawn in order to drive the respective signal line active.

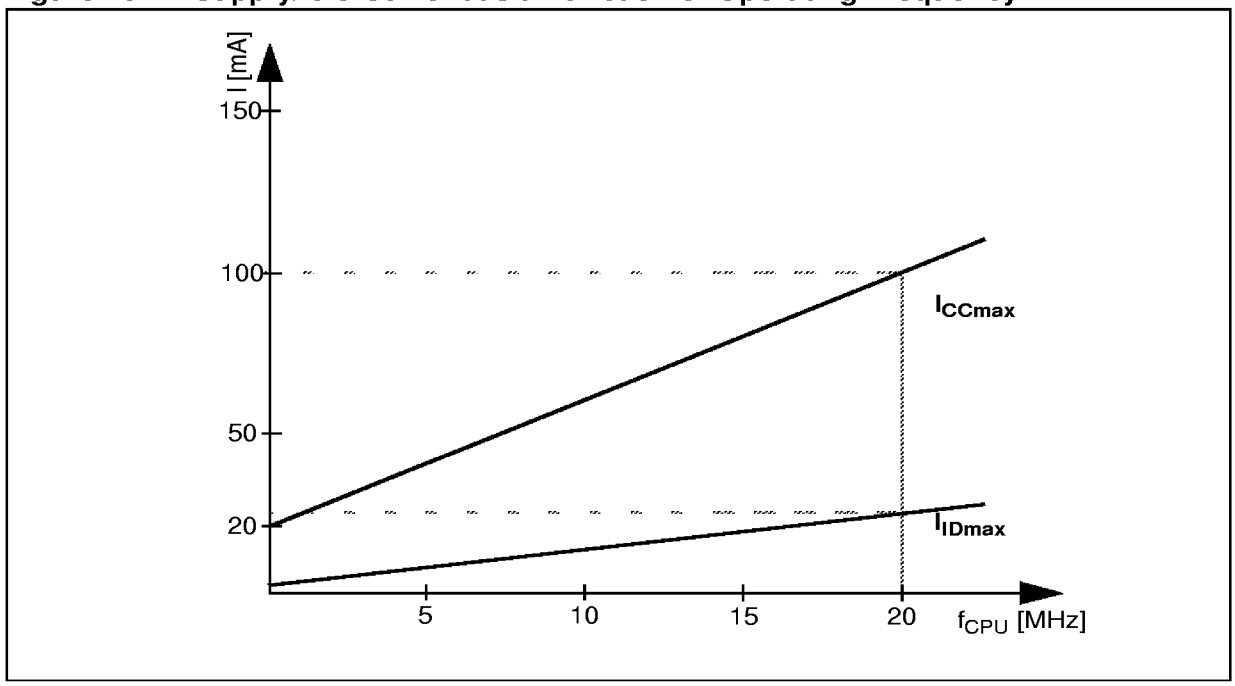
4:This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for $\overline{CS}$ output and the open drain function is not enabled.

5:Not 100% tested, guaranteed by design characterization.

6:The supply current is a function of the operating frequency. This dependency is illustrated in the figure below.
These parameters are tested at V_{DDmax} and 20 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

7:This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1$ V to V_{DD}, $V_{REF} = 0$ V, all outputs (including pins configured as outputs) disconnected.

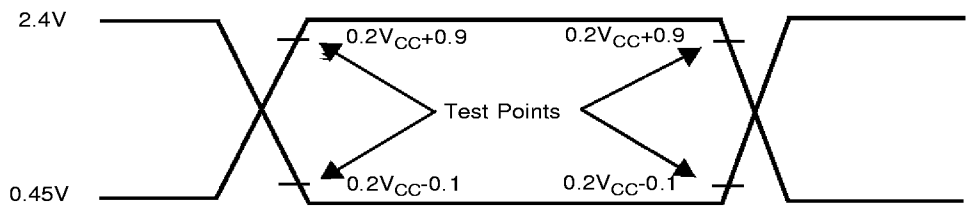
Figure 15.1 Supply/Idle Current as a Function of Operating Frequency



15.4 AC Characteristics

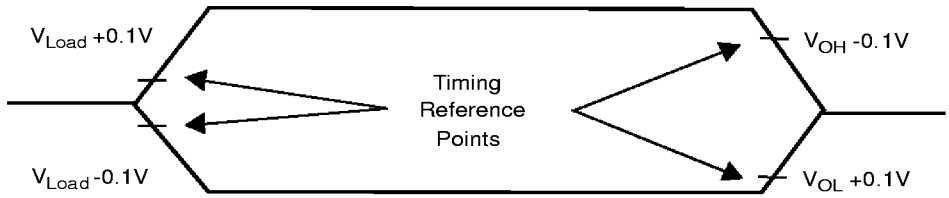
15.4.1 Test Waveforms

Figure 15.2 Input Output Waveforms



AC inputs during testing are driven at 2.4 V for a logic '1' and 0.4 V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

Figure 15.3 Float Waveforms



For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs, but begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

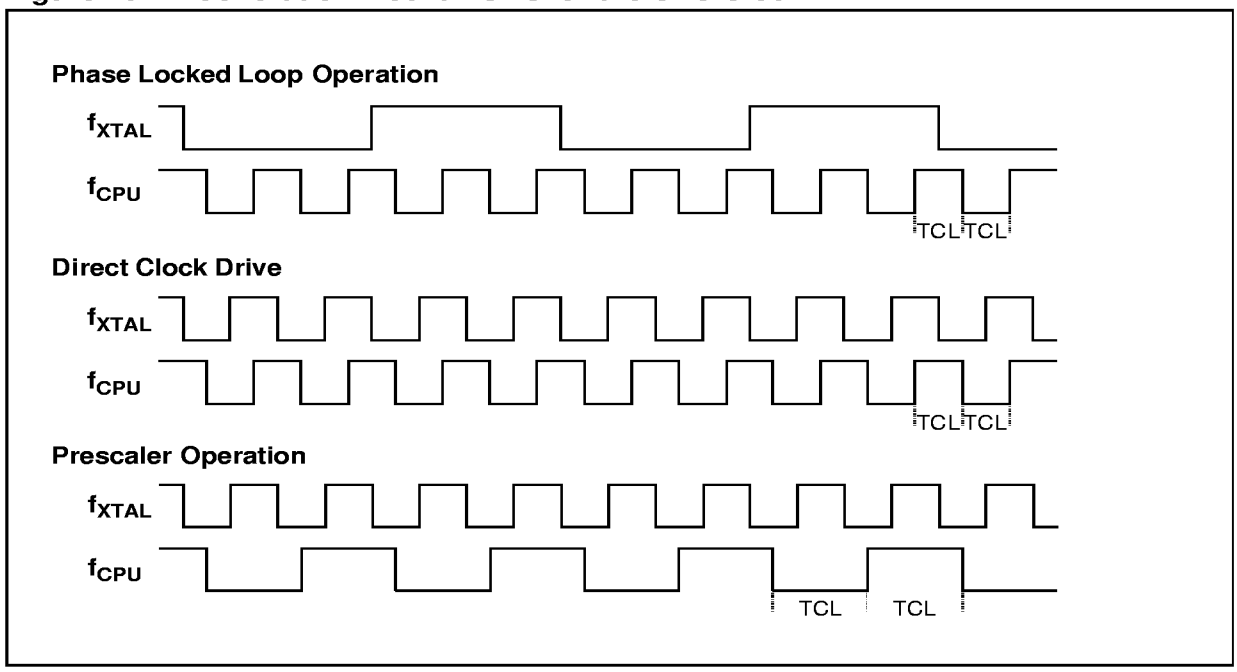
15.4.2 Definition of Internal Timing

The internal operation of the ST10R163 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The external timing (AC Characteristics), therefore, depends on the time (TCL) between two consecutive edges of the CPU clock. The CPU clock f_{CPU} can be generated by different mechanisms. The duration of TCL and its variation (and hence the derived external timing) depends on the mechanism used to generate f_{CPU}. Figure 15.4 shows the CPU clock for direct drive, prescaler or PLL operations. This must be taken into account when calculating the timings for the ST10R163.

Note: The example for PLL operation shown in Figure 15.4 refers to a PLL factor of 4.

Figure 15.4 Generation Mechanisms for the CPU Clock



15.4.3 Clock Generation Modes

The mechanism used to generate the CPU clock is selected during reset by the logic levels on Port 0 pins P0.15-13 (P0H.7-5). Table 15.2 relates the combinations of these three bits to the respective clock generation mode: prescaler operation, direct drive and phase locked loop.

Table 15.2 Clock Mode Selection

P0.15-13 (P0H.7-5)			CPU Frequency $f_{CPU} = f_{XTAL} * F$	External Clock Input Range [1]	Notes
1	1	1	$F_{XTAL} * 4$	2.5 to 6.25 MHz	Default configuration
1	1	0	$F_{XTAL} * 3$	3.33 to 8.33 MHz	
1	0	1	$F_{XTAL} * 2$	5 to 12.5 MHz	
1	0	0	$F_{XTAL} * 5$	2 to 5 MHz	
0	1	1	$F_{XTAL} * 1$	1 to 25 MHz	Direct drive [2]
0	1	0	$F_{XTAL} * 1.5$	6.66 to 16.6 MHz	
0	0	1	$F_{XTAL} / 2$	2 to 50 MHz	CPU clock via prescaler
0	0	0	$F_{XTAL} * 2.5$	4 to 10 MHz	

Notes 1:The external clock input range refers to a CPU clock range of 10...25 MHz.
2:The maximum depends on the duty cycle of the external clock signal.

15.4.4 Prescaler Operation

When pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler. The frequency of f_{CPU} is half the frequency of f_{XTAL}. The high and low time of f_{CPU} (i.e. the duration of an individual TCL) is the period of the input clock f_{XTAL}.

$$TCL = 1/f_{XTAL}$$

The TCLs timings listed in the AC Characteristics can therefore be calculated using the period of f_{XTAL} for any TCL.

15.4.5 Direct Drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset, the on-chip phase locked loop is disabled and the CPU clock is directly driven by the input clock. The frequency of f_{CPU} is, therefore, the frequency of f_{XTAL}. TCL may vary depending on the high and low time (duty cycle) of the input clock f_{XTAL}.

The TCL timings listed below must, therefore, be calculated using the minimum possible TCL. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{XTAL} * DC_{min}$$

DC= duty cycle

For two consecutive TCLs, the deviation caused by the duty cycle of f_{XTAL} is compensated so the duration of 2TCL is always $1/f_{XTAL}$. The minimum value TCL_{min}, therefore, has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

Note:The address float timings in Multiplexed bus mode

(t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} * DC_{max}$) instead of TCL_{min}.

15.4.6 Phase Locked Loop

For all other combinations of pins P0.15-13 (P0H.7-5), during reset the on-chip phase locked loop is enabled and provides the CPU clock (Table 15.2). The PLL multiplies the input frequency by the factor **F** which is selected by the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{XTAL} * \mathbf{F}$).

With every Fth transition of f_{XTAL}, the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly and the CPU clock frequency does not change abruptly.

Due to this adaptation of the input clock, the frequency of fcpu is constantly adjusted so it is locked to f_{XTAL}. The variation causes a jitter of fcpu, which in turn affects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCL must, therefore, be calculated using the minimum TCL that is possible with regard to jitter.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so that it remains locked to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and figure below).

For a period of ***N*** * TCL the minimum value is computed using the corresponding deviation D_N:

$$TCL_{min} = TCL_{NOM} * (1 - |D_N|) / 100$$

$$D_N = \pm(4 - N/15)[\%]$$

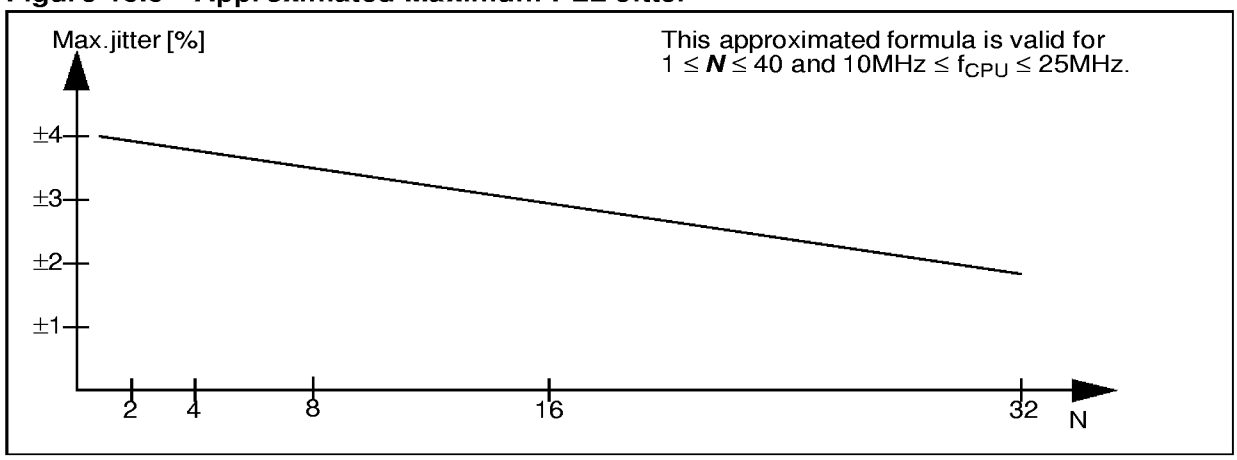
where ***N*** = number of consecutive TCLs and $1 \leq N \leq 40$.

So for a period of 3 TCLs (i.e. ***N*** = 3):

$$D_3 = 4 - 3/15$$
$$= 3.8\%$$
$$(3TCL)_{min} = 3TCL_{NOM} \times (1 - 3.8/100)$$
$$= 3TCL_{NOM} \times 0.962$$
$$(57.72nsec@f_{CPU} = 25MHz)$$

This is important for bus cycles using waitstates and for example, the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Figure 15.5 Approximated Maximum PLL Jitter



15.4.7 Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 15.3 Memory Cycle Variable Definition

Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

15.4.8 External Clock Drive XTAL1

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A= 0 to +70 °C

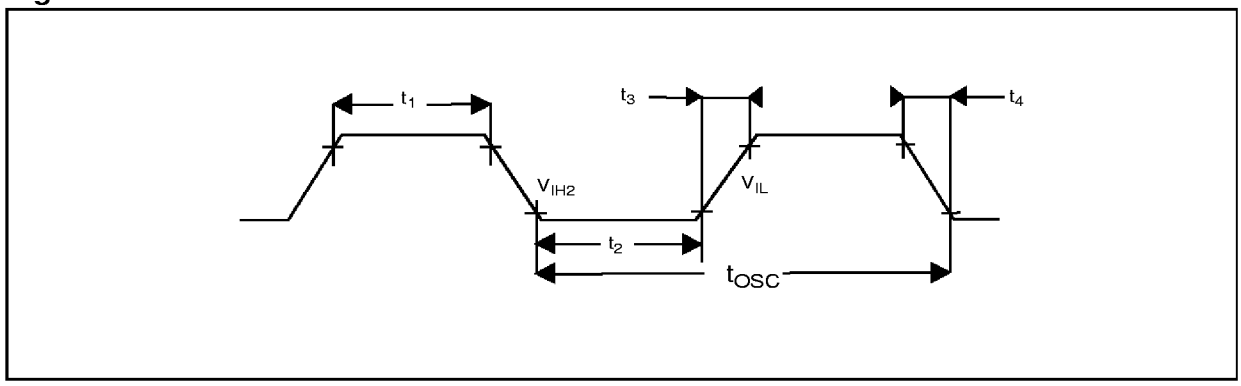
Table 15.4 External Clock Drive Characteristics

Parameter	Symbol	$f_{CPU} = f_{XTAL}$		$f_{CPU} = f_{XTAL} / 2$		$f_{CPU} = f_{XTAL} * N$ N = 1.5/2/2.5/3/4/5		Unit
		min.	max.	min.	max.	min.	max.	
Oscillator period	Tosc SR	40[1)]	1000	20	500	40 * N	100 * N	ns
High time	t_1 SR	18[2)]	–	6[2)]	–	10[2)]	–	ns
Low time	t_2 SR	18[2)]	–	6[2)]	–	10[2)]	–	ns
Rise time	t_3 SR	–	10[2)]	–	6[2)]	–	10[2)]	ns
Fall time	t_4 SR	–	10[2)]	–	6[2)]	–	10[2)]	ns

Notes 1:Theoretical minimum. The real minimum value depends on the duty cycle of the input clock signal; t_1 and t_2 must be met.

2:The input clock signal must reach the defined levels VIL and VIH2.

Figure 15.6 External Clock Drive XTAL1



15.4.9 Multiplexed Bus

V_{DD} = 5 V ± 10%;V_{SS} = 0 V, T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF, C_L (for Port 6, $\overline{CS}$) = 100 pF
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25-MHz CPU clock without waitstates)

Table 15.5 Multiplexed Bus Characteristics

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5 CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6 CC	4 + t_A	–	TCL - 16+ t_A	–	ns
Address hold after ALE	t_7 CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8 CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9 CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10} CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11} CC	–	26	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12} CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13} CC	45 + t_C	–	3TCL - 15 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14} SR	–	20 + t_C	–	2TCL - 20+ t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15} SR	–	40 + t_C	–	3TCL - 20+ t_C	ns
ALE low to valid data in	t_{16} SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17} SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18} SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19} SR	–	26 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22} CC	24 + t_C	–	2TCL - 16+ t_C	–	ns
Data hold after $\overline{WR}$	t_{23} CC	26 + t_F	–	2TCL - 14+ t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25} CC	26 + t_F	–	2TCL - 14+ t_F	–	ns

Table 15.5 Multiplexed Bus Characteristics (cont'd)

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
		min.	max.	min.	max.	
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27} CC	26 + t_F	–	2TCL - 14+ t_F	–	ns
ALE falling edge to $\overline{CS}$	t_{38} CC	-8 - t_A	5 - t_A	-8 - t_A	5 - t_A	ns
$\overline{CS}$ low to Valid Data In	t_{39} SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{40} CC	46 + t_F	–	3TCL - 14+ t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42} CC	12 + t_A	–	TCL - 8+ t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43} CC	-6 + t_A	–	-6 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44} CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45} CC	–	20	–	TCL + 0	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46} SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47} SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48} CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49} CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50} CC	26 + t_C	–	2TCL - 14+ t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51} SR	0	–	0	–	ns
Data float after $\overline{RdCS}$	t_{52} SR	–	20 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{54} CC	20 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{56} CC	20 + t_F	–	2TCL - 20 + t_F	–	ns

Figure 15.7 External Memory Cycle:Multiplexed Bus, With Read/Write Delay, Normal ALE

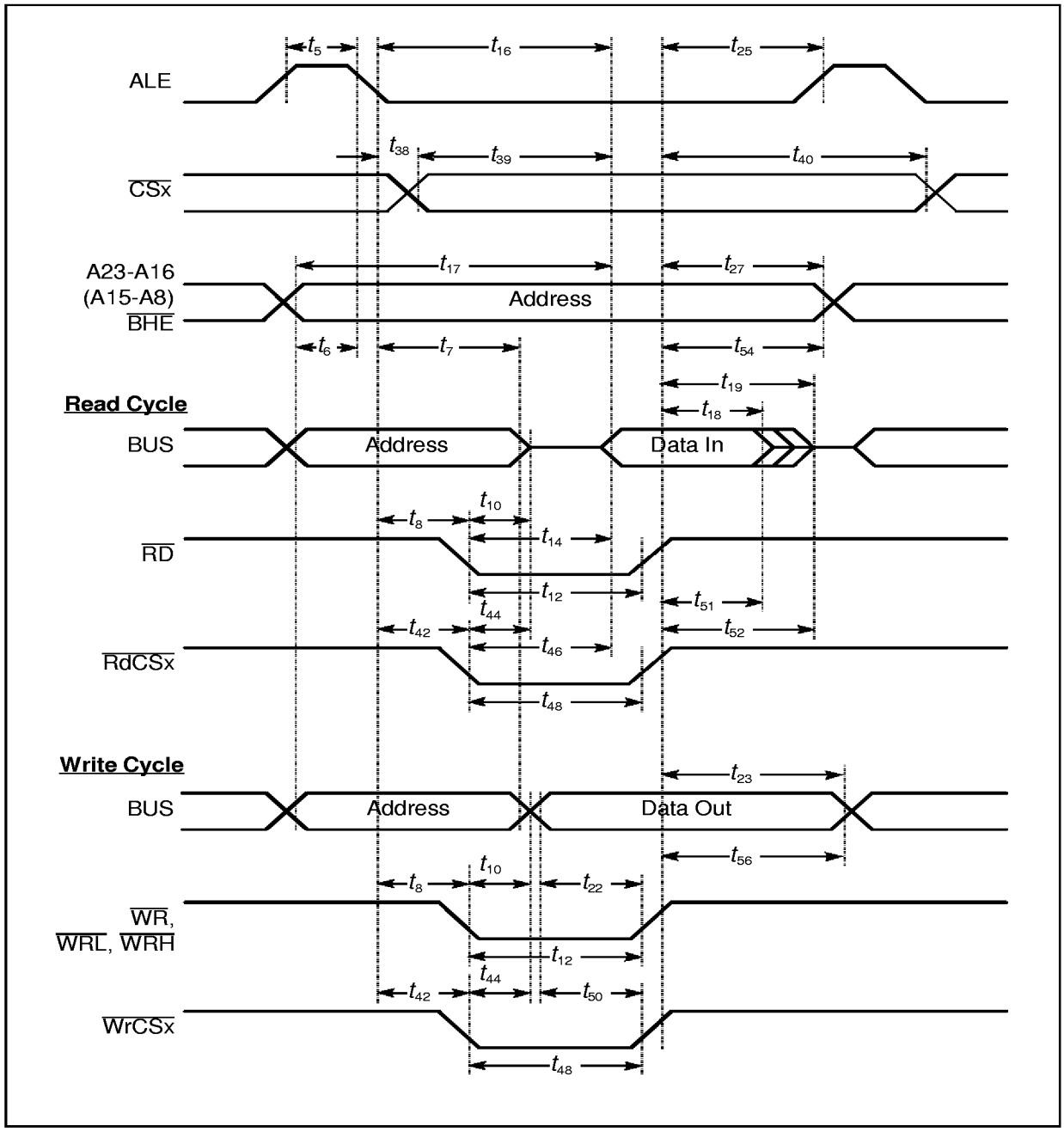


Figure 15.8 External Memory Cycle:Multiplexed Bus, With Read/Write Delay, Extended ALE

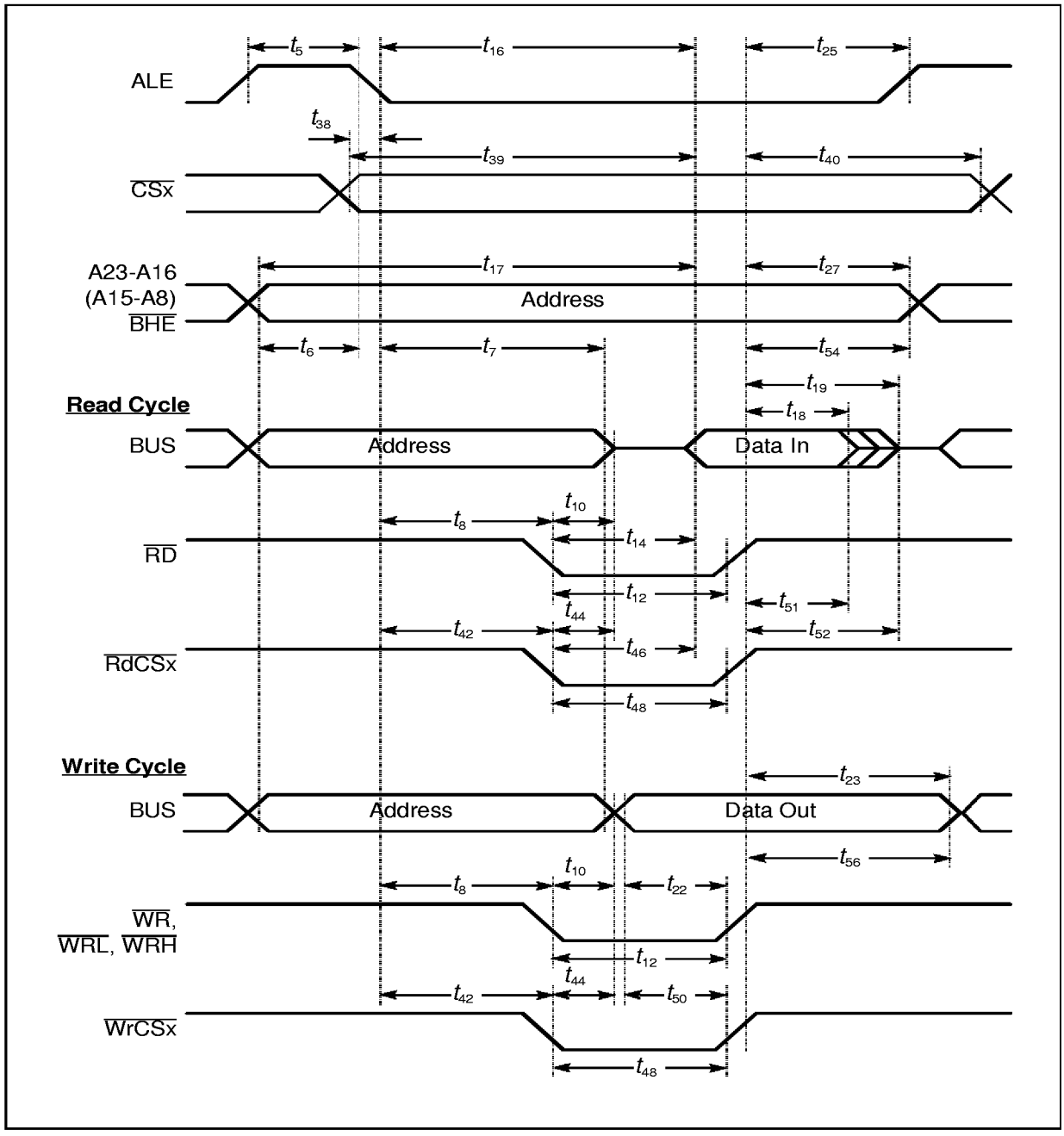


Figure 15.9 External Memory Cycle:Multiplexed Bus, No Read/Write Delay, Normal ALE

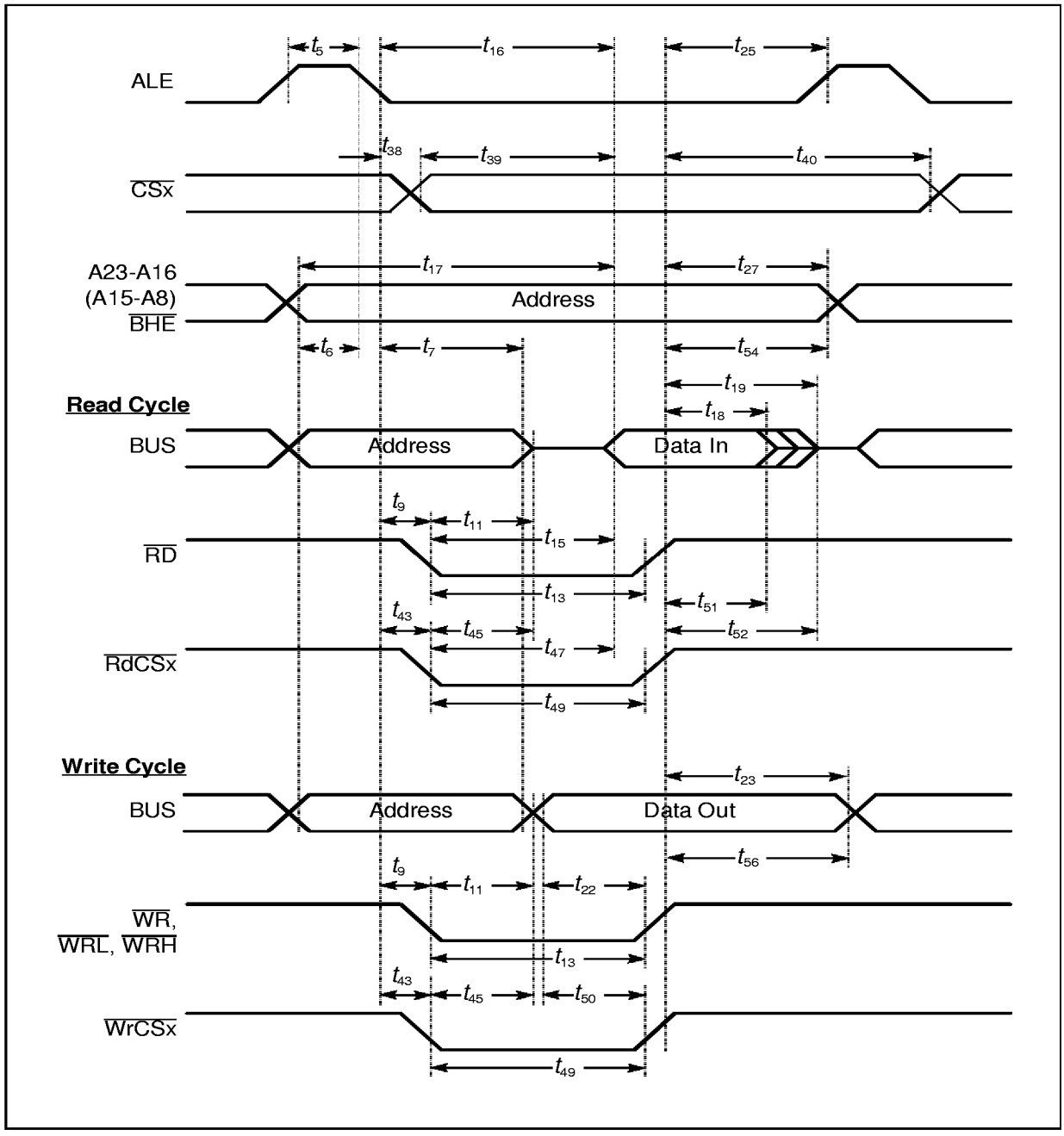
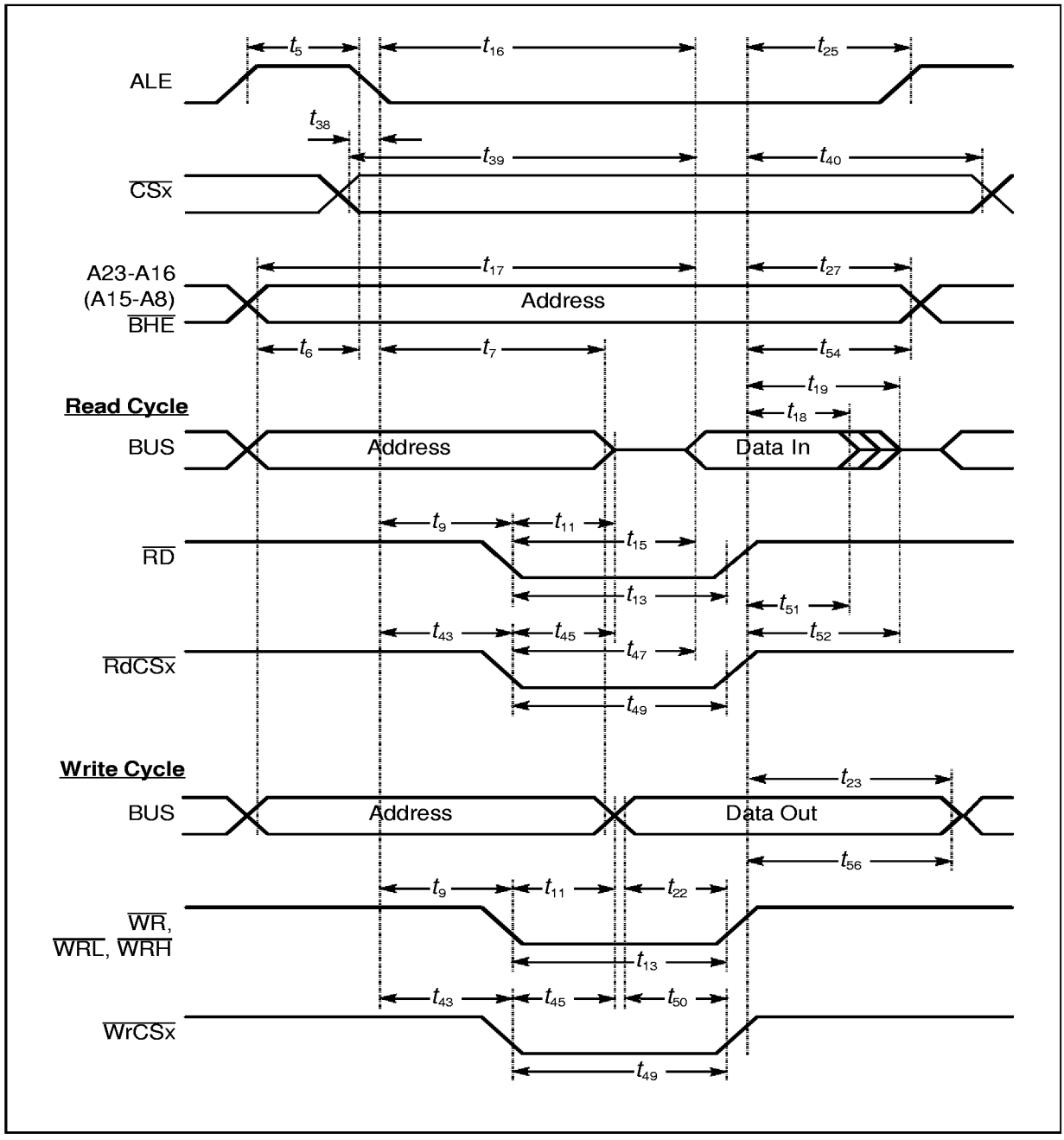


Figure 15.10 External Memory Cycle:Multiplexed Bus, No Read/Write Delay, Extended ALE



15.4.10 Demultiplexed Bus

V_{DD} = 5 V ± 10%;V_{SS} = 0 V, T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF, C_L (for Port 6, $\overline{CS}$) = 100 pF
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Table 15.6 Demultiplexed Bus Characteristics

Parameter	Symbol	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5 CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6 CC	4 + t_A	–	TCL -16+ t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8 CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9 CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12} CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13} CC	45 + t_C	–	3TCL - 15 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14} SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15} SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16} SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17} SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18} SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1)])	t_{20} SR	–	26 + t_F	–	2TCL - 14 + t_F + $2t_A$[1)]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1)])	t_{21} SR	–	10 + t_F	–	TCL - 10 + t_F + $2t_A$[1)]	ns
Data valid to $\overline{WR}$	t_{22} CC	24 + t_C	–	2TCL-16 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24} CC	10 + t_F	–	TCL - 10 + t_F	–	ns

Table 15.6 Demultiplexed Bus Characteristics

Parameter	Symbol	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
		min.	max.	min.	max.	
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26} CC	-10 + t_F	–	-10 + t_F	–	ns
Address hold after $\overline{WR}$[2]	t_{28} CC	0 + t_F	–	0 + t_F	–	ns
ALE falling edge to $\overline{CS}$	t_{38} CC	-8 - t_A	5 - t_A	-8 - t_A	5 - t_A	ns
$\overline{CS}$ low to Valid Data In	t_{39} SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{41} CC	6 + t_F	–	TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42} CC	12 + t_A	–	TCL - 8 + t_A	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43} CC	-6 + t_A	–	-6 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46} SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47} SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48} CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49} CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50} CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51} SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay)	t_{53} SR	–	20 + t_F	–	2TCL - 20 + t_F	ns
Data float after $\overline{RdCS}$ (no RW-delay)	t_{68} SR	–	0 + t_F	–	TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{55} CC	-6 + t_F	–	-6 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{57} CC	6 + t_F	–	TCL - 14 + t_F	–	ns

Notes 1:RW-delay and t_A refer to the next following bus cycle.

2:Read data are latched with the same clock edge that triggers the address change and the rising $\overline{RD}$ edge. Therefore address changes before the end of $\overline{RD}$ have no impact on read cycles.

Figure 15.11 External Memory Cycle:Demultiplexed Bus, With Read/Write Delay, Normal ALE

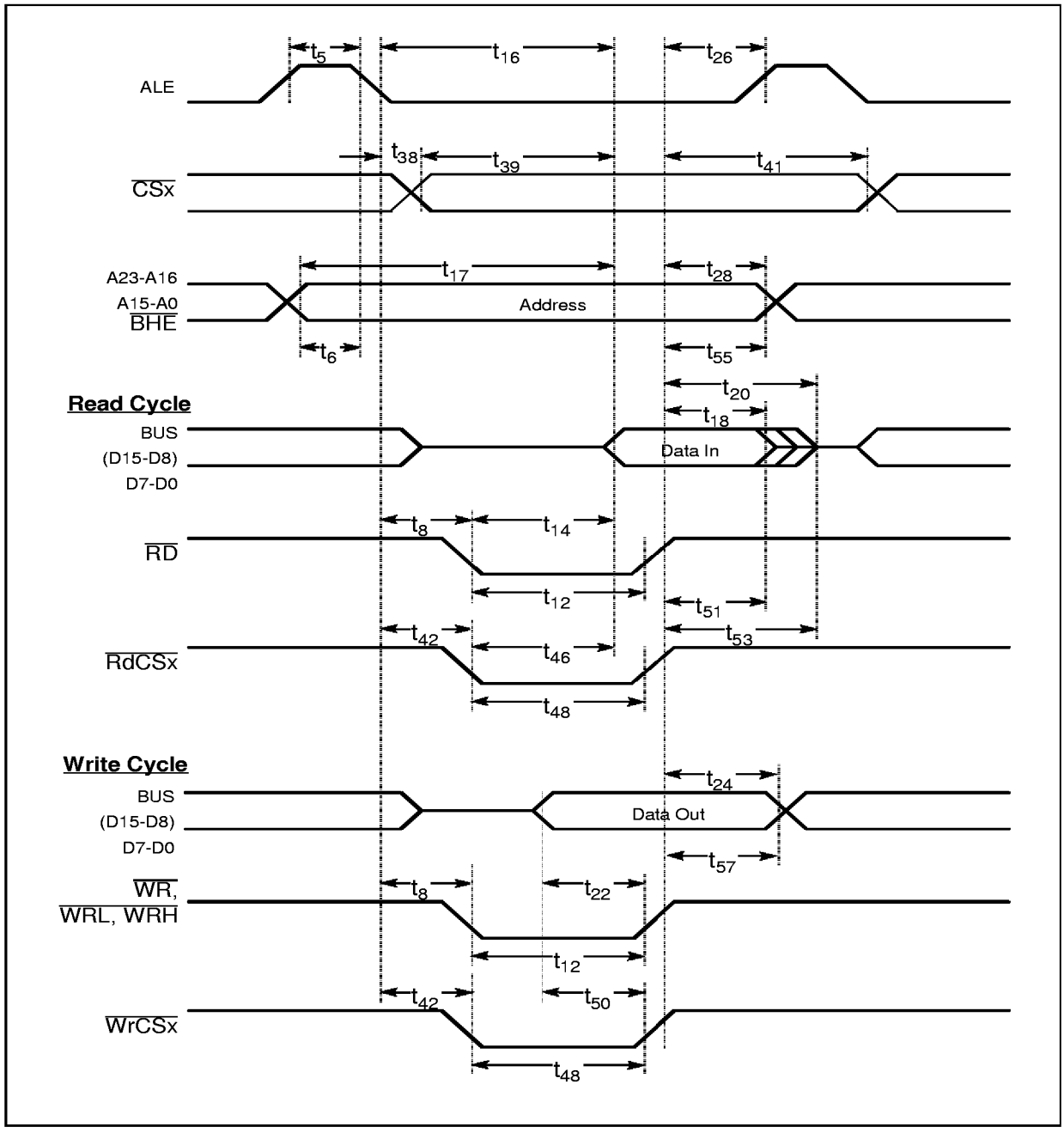


Figure 15.12 External Memory Cycle:Demultiplexed Bus, With Read/Write Delay, Extended ALE

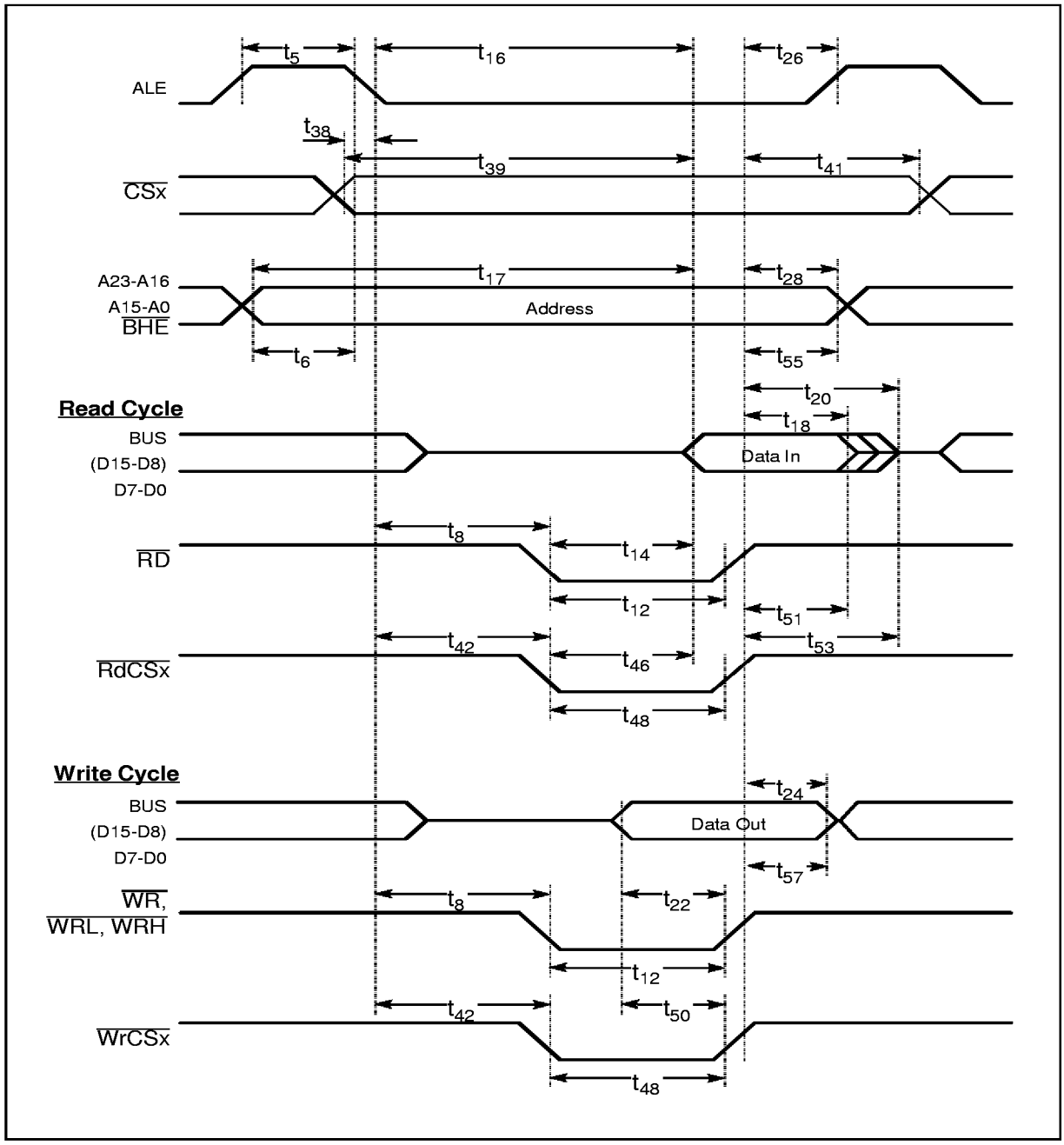


Figure 15.13 External Memory Cycle:Demultiplexed Bus, No Read/Write Delay, Normal ALE

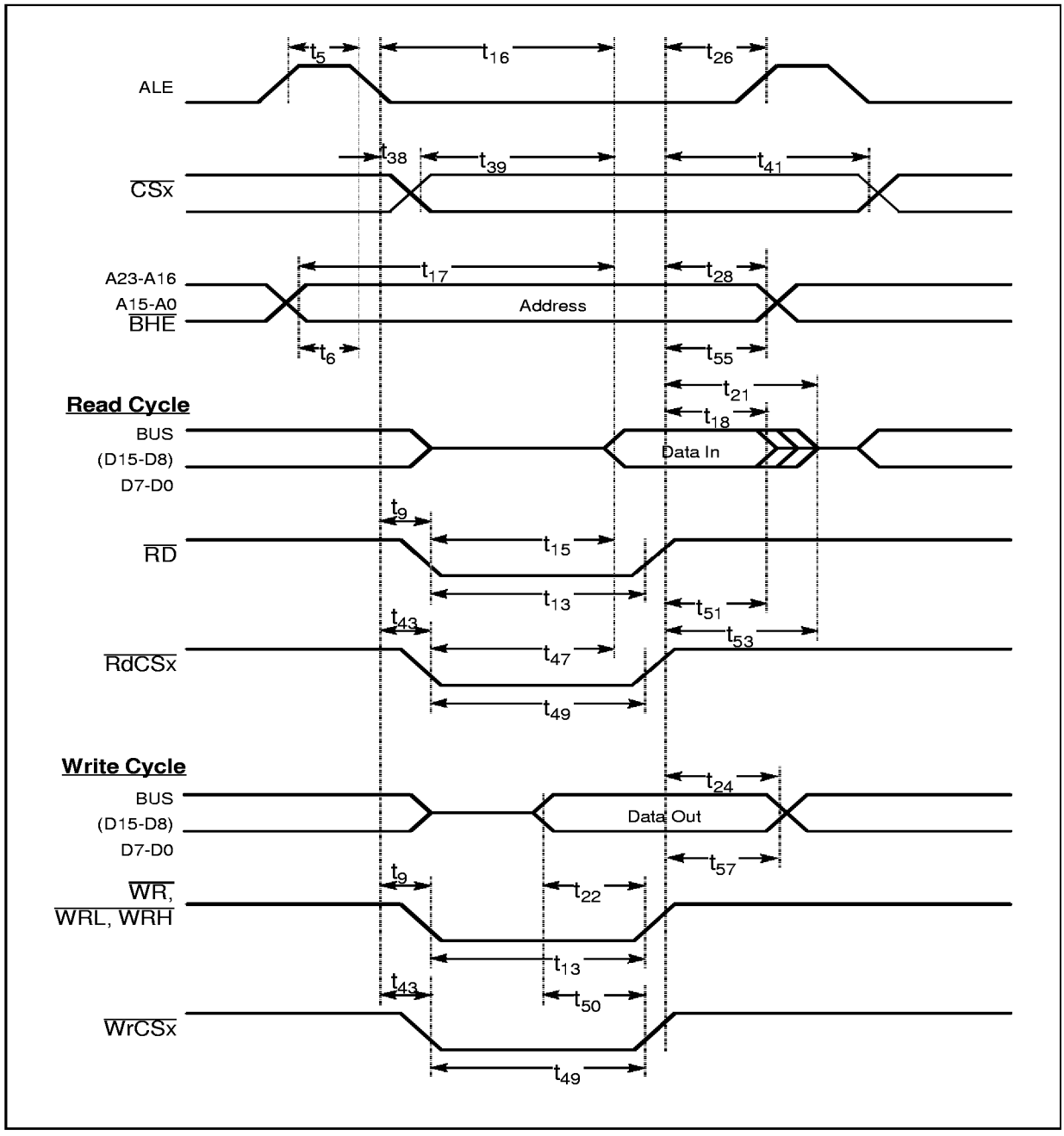
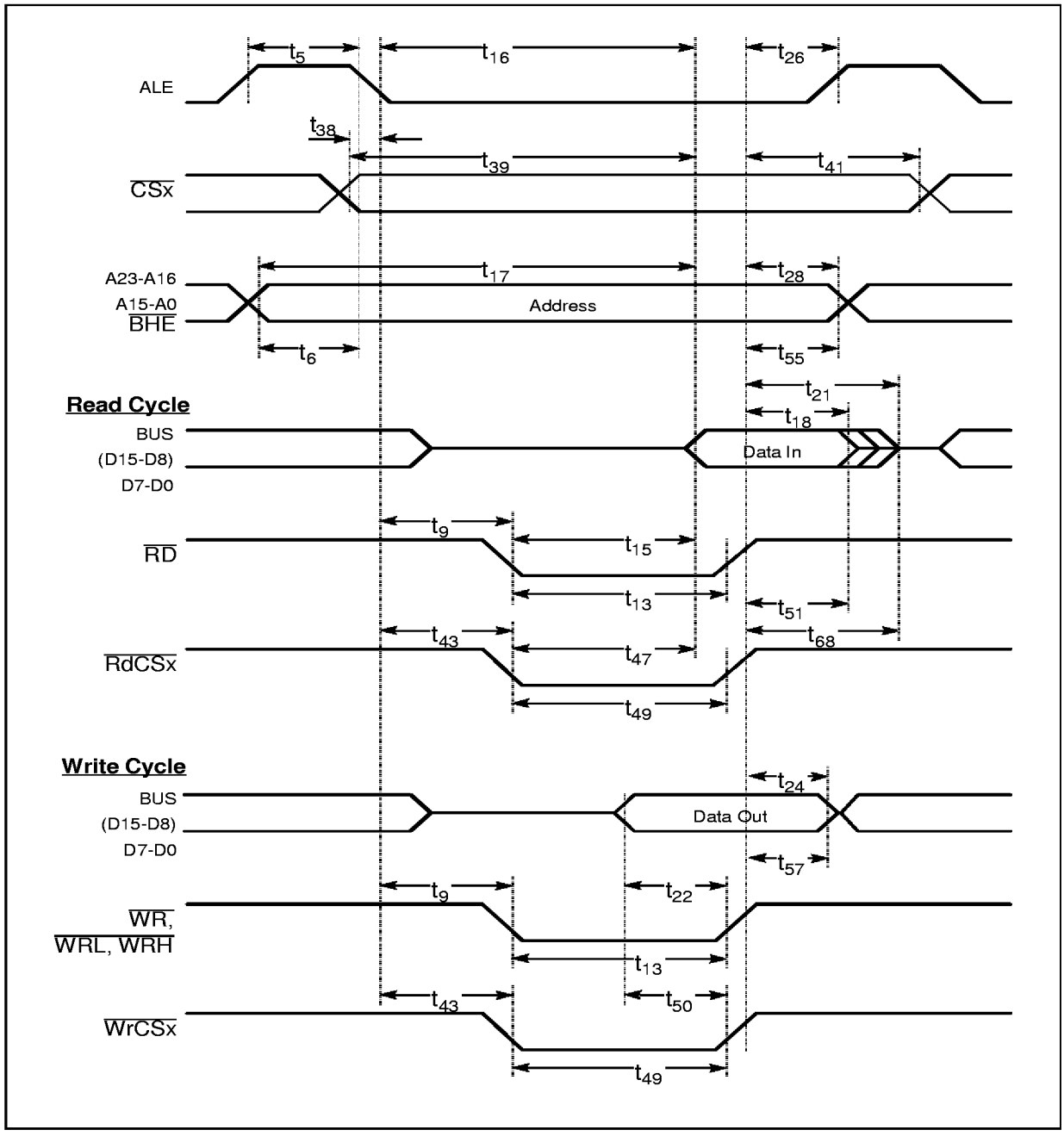


Figure 15.14 External Memory Cycle:Demultiplexed Bus, No Read/Write Delay, Extended ALE



15.4.11 CLKOUT and $\overline{\text{READY}}$

V_{DD} = 5 V ± 10%;V_{SS} = 0 V, T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF, C_L (for Port 6, $\overline{CS}$) = 100 pF

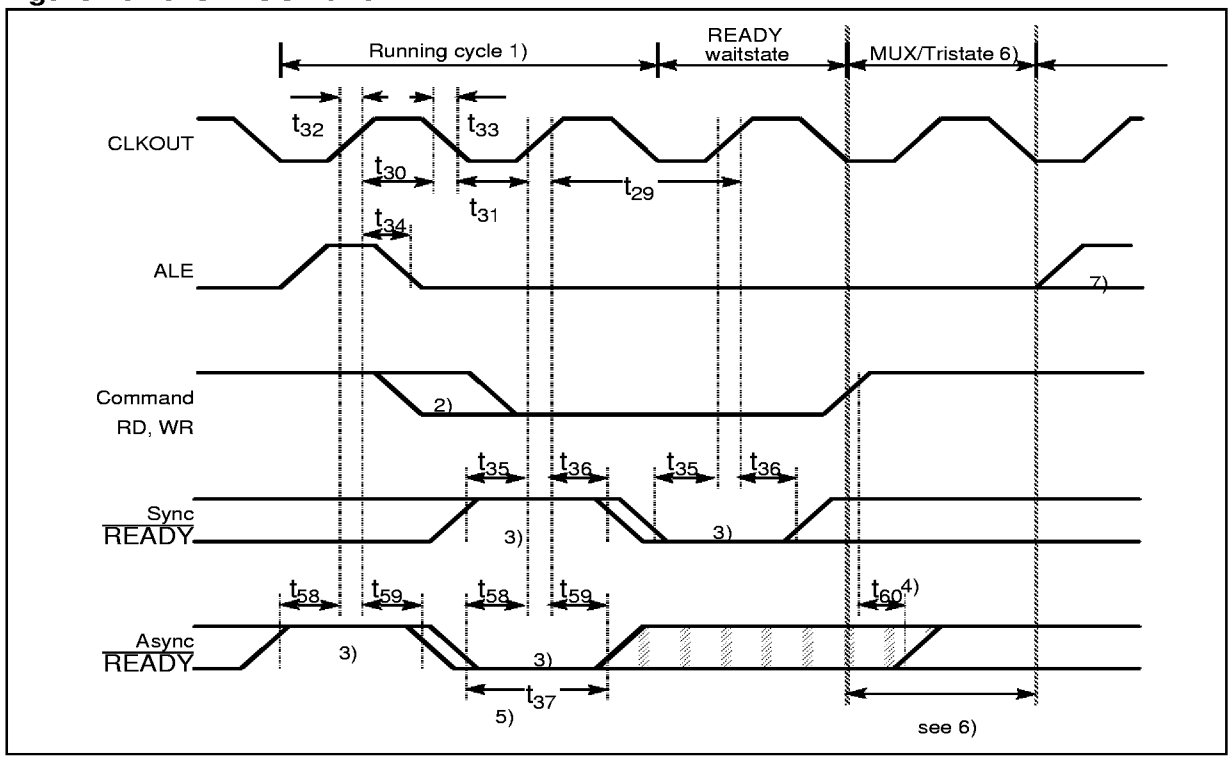
Table 15.7 CLKOUT and $\overline{\text{READY}}$ Characteristics

Parameter	Symbol	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
		min.	max.	min.	max.	
CLKOUT cycle time	t_{29} CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30} CC	14	–	TCL – 6	–	ns
CLKOUT low time	t_{31} CC	10	–	TCL – 10	–	ns
CLKOUT rise time	t_{32} CC	–	4	–	4	ns
CLKOUT fall time	t_{33} CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34} CC	0 + t_A	12 + t_A	0 + t_A	12 + t_A	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35} SR	10	–	10	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36} SR	0	–	0	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37} SR	54	–	2TCL + 14	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58} SR	14	–	14	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59} SR	0	–	0	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{RD}$, $\overline{WR}$ high (Demultiplexed Bus) [2]	t_{60} SR	-	$0+2t_A+t_C+t_F$ [2]	-	TCL - 20 $+2t_A+t_C+t_F$ [2]	ns

Notes 1:These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2:Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

Figure 15.15 CLKOUT and $\overline{\text{READY}}$



Notes 1:Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).

2:The leading edge of the respective command depends on RW-delay.

3:$\overline{\text{READY}}$ sampled HIGH at this sampling point generates a $\overline{\text{READY}}$ controlled waitstate, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.

4:$\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

5:If the Asynchronous $\overline{\text{READY}}$ signal does not fulfil the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfil t_{37} in order to be safely synchronized. This is guaranteed, if $\overline{\text{READY}}$ is removed in response to the command (see Note 4)).

6:Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.

7:The next external bus cycle may start here.

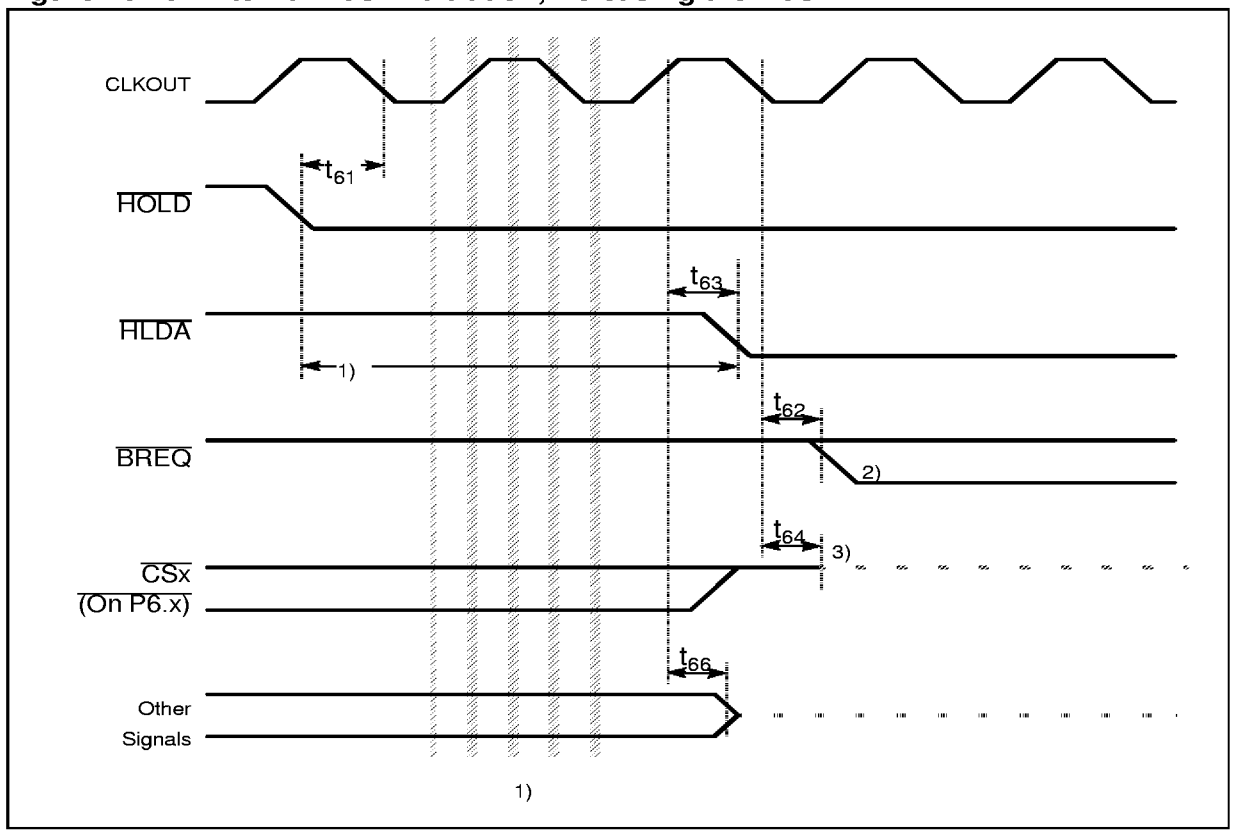
15.4.12 External Bus Arbitration

V_{DD} = 5 V ± 10%;V_{SS} = 0 V, T_A = 0 to +70 °C
C_L (for PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF, C_L (for Port 6, $\overline{CS}$) = 100 pF

Table 15.8 External Bus Arbitration Characteristics

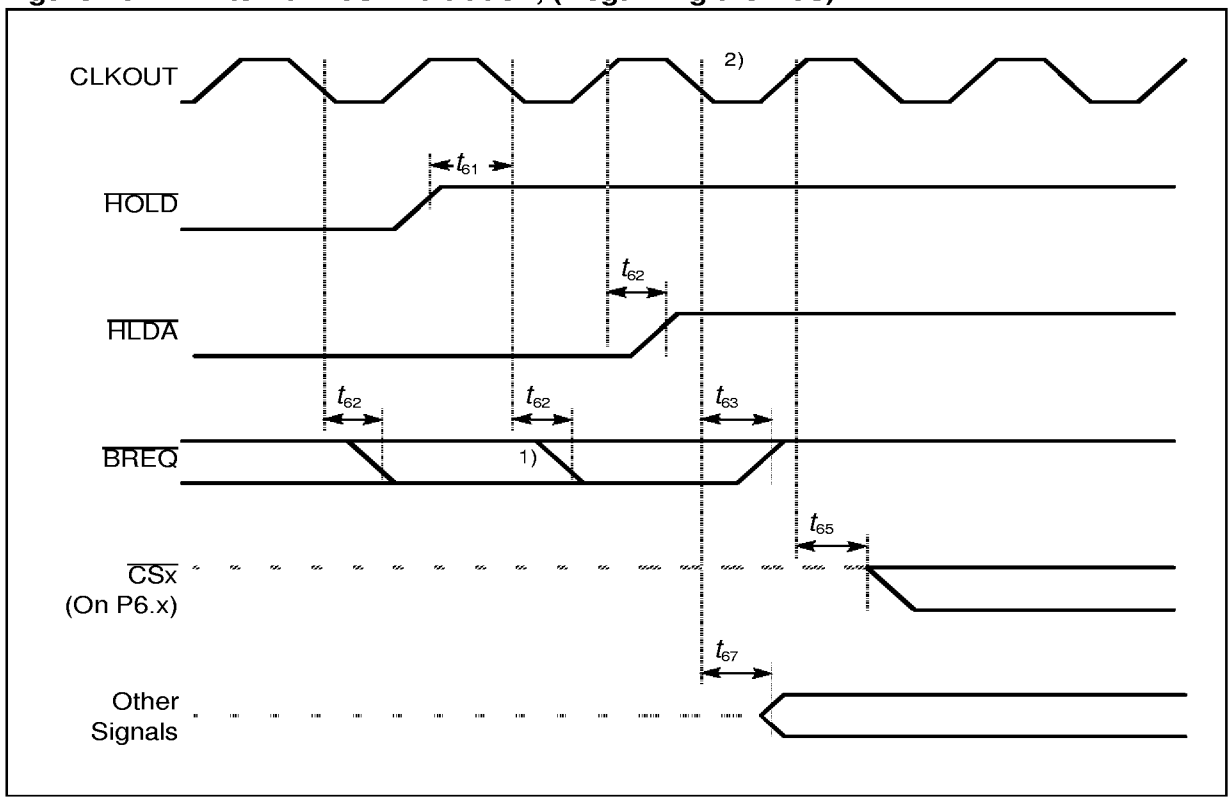
Parameter	Symbol	Max. CPU Clock = 25MHz		Variable CPU Clock 1/2TCL = 1 to 25MHz		Unit
		min.	max.	min.	max.	
$\overline{HOLD}$ input setup time to CLKOUT	t_{61} SR	20	–	20	–	ns
CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	t_{62} CC	–	20	–	20	ns
CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	t_{63} CC	–	20	–	20	ns
$\overline{CSx}$ release	t_{64} CC	–	20	–	20	ns
$\overline{CSx}$ drive	t_{65} CC	-4	24	-4	24	ns
Other signals release	t_{66} CC	–	20	–	20	ns
Other signals drive	t_{67} CC	-4	24	-4	24	ns

Figure 15.16 External Bus Arbitration, Releasing the Bus



Notes 1:The ST10R163 will complete the currently running bus cycle before granting bus access.
2:This is the first possibility for $\overline{BREQ}$ to get active.
3:The $\overline{CS}$ outputs will be resistive high (pullup) after t_{64}.

Figure 15.17 External Bus Arbitration, (Regaining the Bus)



Notes 1:This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence.
Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high.
$\overline{\text{HOLD}}$ may also be de-activated without the ST10R163 requesting the bus.
2:The next ST10R163 driven bus cycle may start here.

15.4.13 Synchronous Serial Port Timing

V_{CC} = 5 V ± 10%; V_{SS} = 0 V, T_A = 0 to +70 °C, C_L = 100 pF

Parameter	Symbol	Max. Baudrate = 12.5 / 10 MBd		Variable Baudrate		Unit
		min.	max.	min.	max.	
SSP clock cycle time	t_{200} CC	80 / 100	80 / 100	4 TCL	512 TCL	ns
SSP clock high time	t_{201} CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
SSP clock low time	t_{202} CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
SSP clock rise time	t_{203} CC	– / –	5 / 5	–	5	ns
SSP clock fall time	t_{204} CC	– / –	5 / 5	–	5	ns
CE active before shift edge	t_{205} CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
CE inactive after latch edge	t_{206} CC	70 / 90	90 / 110	t_{200} - 10	t_{200} + 10	ns
Write data valid after shift edge	t_{207} CC	– / –	10 / 10	–	10	ns
Write data hold after shift edge	t_{208} CC	0 / 0	– / –	0	–	ns
Write data hold after latch edge	t_{209} CC	35 / 45	45 / 55	t_{200}/2 - 5	t_{200}/2 + 5	ns
Read data active after latch edge	t_{210} SR	50 /60	– / –	t_{200}/2 + 10	–	ns
Read data setup time before latch edge	t_{211} SR	20 / 20	– / –	20	–	ns
Read data hold time after latch edge	t_{212} SR	0 / 0	– / –	0	–	ns

Figure 15.18 SSP Write Timing

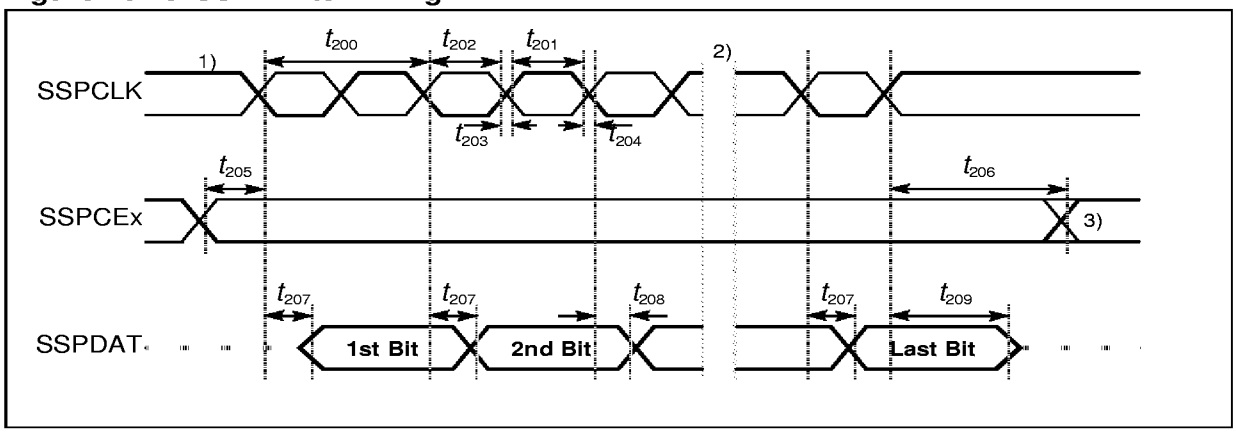
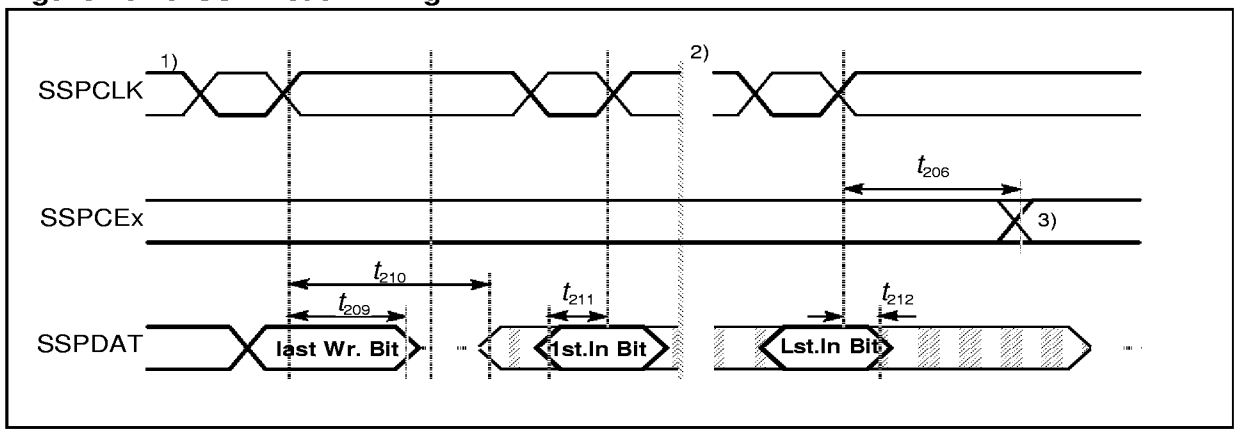


Figure 15.19 SSP Read Timing



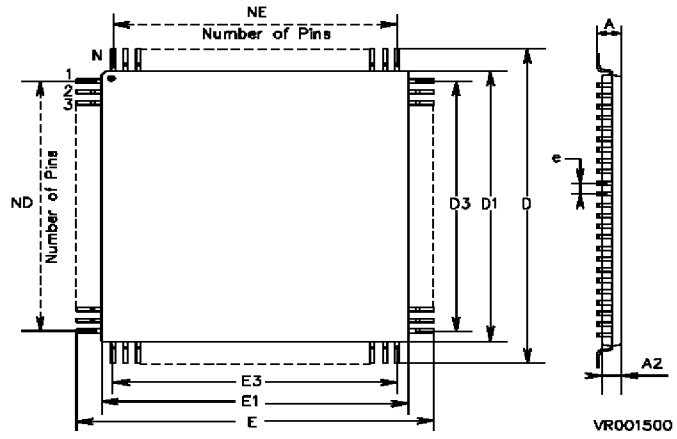
Notes 1:The transition of shift and latch edge of SSPCLK is programmable. This figure uses the falling edge as shift edge (drawn bold).

2:The bit timing is repeated for all bits to be transmitted or received.

3:The active level of the chip enable lines is programmable. This figure uses an active low CE (drawn bold). At the end of a transmission or reception the CE signal is disabled in single transfer mode. In continuous transfer mode it remains active.

16 PACKAGE MECHANICAL DATA

Figure 16.1 Package Outline TQFP100 (14 x 14 mm)



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D3		12.00			0.472	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
e		0.50			0.020	
Number of Pins						
ND	25					
NE	25					
N*	100					

N=2*(ND+NE)

17 ORDERING INFORMATION

Salestype	Temperature range	Package
ST10R163BT1	0°C to 70°C	TQFP100 (14x 14)