YAMAHA LSI

YDC103

SPC7

Signal Processor & Controller for Compact Disc Player

■ OUTLINE

YDC103 is one-chip CMOS LSI to provide various servo control and signal processing needed for the CD player.
By built-in digital PLL clock regeneration circuit and 16k RAM, it performs EFM signal demodulation, error detection and correction, and jitter absorption.
It also performs various intelligent servo controls for focussing, tracking, feeding and disc motor.
In addition, as this LSI has sigma-delta type 1-bit DACs, even analog audio signals are obtained easily with only some external parts attached.
Furthermore, it is provided with a digital audio interface output function which conforms to the EIAJ format.

■ FEATURES

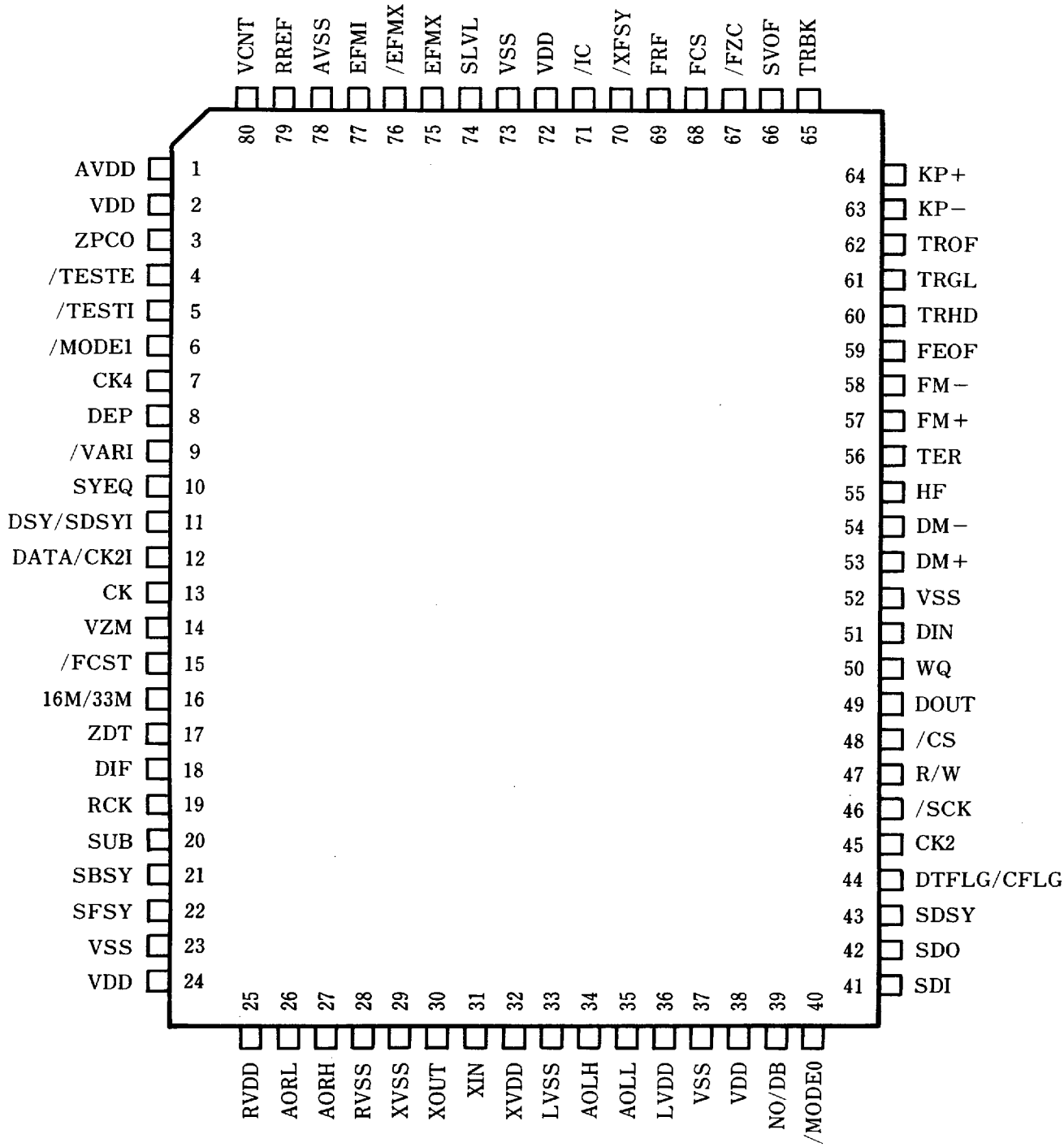
- Generates standard clock and necessary timing singals with a crystal connected.
- With the digital PLL and slice level control circuit built in, it performs EFM signal clock regeneration, synchronous signal separation and EFM demodulation.
- CRC-checks the Q sub-code and outputs to the microprocessor in addition to separating the sub-code and providing the output conforming to the EIAJ format.
- Detects the phase difference between the regenerated and standard clock signals and controls the disc motor by means of PWM.
- Easy servo control by focussing search, track auto search and track count functions.
- The built-in RAM buffers (±4 frames) and de-interleaves the EFM demodulation signals to absorb jitter.
- Error detection and correction for digital audio signals and flag processing. (Double error correction for both C1 and C2).
- Linear interpolation processing is used for up to 8 consecutive uncorrectable error data and preceeding data hold processing for errors over eight.
- The de-emphasis processing function, 8-times digial filter and 3rd order sigma-delta system 1-bit DACs are built in so that analog signals can be obtained easily.
- Outputs digital audio interface signals conforming to EIAJ format.
- Peak level detection function for output of sound level to be used for peak level search, etc.
- Digital attenuation function with 0.4dB resolution and 240 steps.
- Outputs error flags for CD-ROM, etc.
- Capable of playing at ±10% variable speed and capable of playing at a double speed with 33.8688MHz connected.
- 5V single power supply, Si-gate CMOS process.
- 80pin plastic QFP(YDC103-F).

YAMAHA CORPORATION

9945524 0002568 7T2

YDC103 CATALOG
CATALOG No. : LSI-4DC103A2
1995. 12

■ PIN CONFIGURATION



< 80pin Top View >

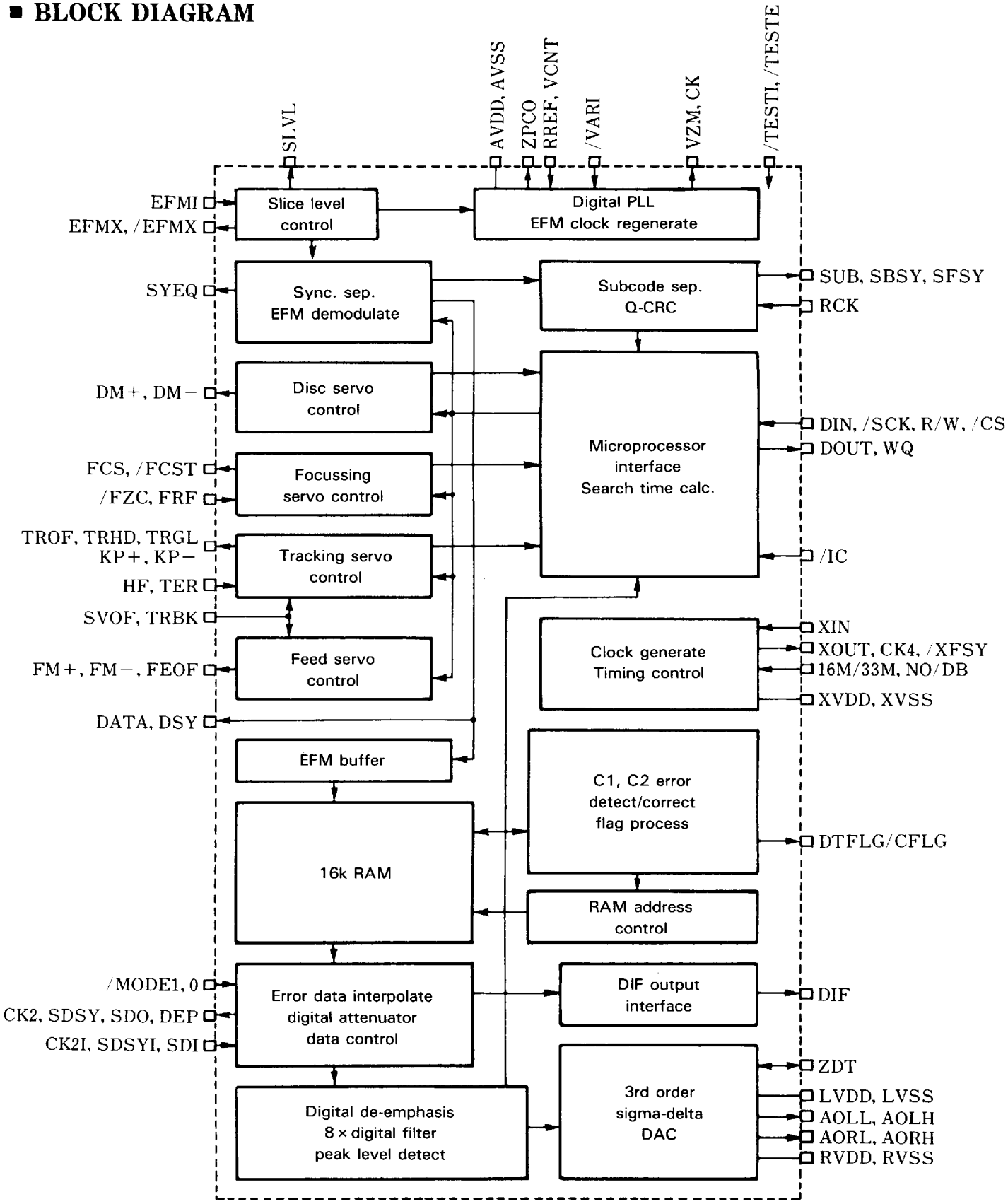
■ PIN FUNCTION

No.	Name	I/O	Function
1	AVDD	A	5V power supply (for PLL block)
2	VDD		5V power supply (for logic block)
3	ZPCO	O	Phase comparator output for digital PLL driving clock generator
4	/TESTE	I+	LSI test terminal (should be left unconnected)
5	/TESTI	I+	LSI test terminal (should be left unconnected)
6	/MODE1	I+	Audio signal output mode select 1
7	CK4	O	Clock output (4.2336MHz)
8	DEP	O	De-emphasis control signal output
9	/VARI	I+	Variable speed select ('L' : variable speed)
10	SYEQ	O	Sync. equal signal output
11	DSY/SDSYI	I/O	EFM demodulation signal, synchronous signal / L/R clock input during DSP mode
12	DATA/CK2I	I/O	EFM demodulation signal, data signal / bit clock input during DSP mode
13	CK	OD	EFM regeneration clock output
14	VZM	OD	Digital PLL driving clock output, dividing into 3 or 6 signal output
15	/FCST	OD	Focus search start signal output
16	16M/33M	I+	Master clock select ('H' : 16.9344MHz, 'L' : 33.8688MHz)
17	ZDT	I+/O	DAC zero detect muting enable/sound signal zero detect output
18	DIF	O	Digital audio interface signal output
19	RCK	I−	Sub-code interface read clock
20	SUB	OD	Sub-code interface sub-code data
21	SBSY	OD	Sub-code interface block synchronous signal
22	SFSY	OD	Sub-code interface frame synchronous signal
23	VSS		Ground (for logic block)
24	VDD		5V power supply (for noise shaper block)
25	RVDD	A	5V power supply (for DAC Rch block)
26	AORL	OA	DAC stream output (L for Rch)
27	AORH	OA	DAC stream output (H for Rch)
28	RVSS	A	Ground (for DAC Rch)
29	XVSS		Ground (for crystal oscillation block)
30	XOUT	O	Crystal oscillator connecting terminal
31	XIN	I	Crystal oscillator connecting terminal (16.9344MHz or 33.8688MHz)
32	XVDD		5V power supply (for crystal oscillation block)
33	LVSS	A	Ground (for DAC Lch)
34	AOLH	OA	DAC stream output (H for Lch)
35	AOLL	OA	DAC stream output (L for Lch)
36	LVDD	A	5V power supply (for DAC Lch)
37	VSS		Ground (for noise shaper block)
38	VDD		5V power supply (for logic block)
39	NO/DB	I+	Normal/double speed select
40	/MODE0	I+	Audio signal output mode select 0

No.	Name	I/O	Function
41	SDI	I	DAC digital data input
42	SDO	O	Audio data output serial data
43	SDSY	O	Audio data output L/R clock
44	DTFLG/CFLG	O	Audio data output error flag
45	CK2	O	Audio data output bit clock
46	/SCK	I	Microprocessor interface serial clock
47	R/W	I	Microprocessor interface R/W identification signal
48	/CS	IO	Microprocessor interface chip select
49	DOUT	OT	Microprocessor interface data output
50	WQ	O	Microprocessor interface data read request signal
51	DIN	I	Microprocessor interface data input
52	VSS		Ground (for logic block)
53	DM+	O	Disc motor control signal (acceleration)
54	DM−	O	Disc motor control signal (deceleration)
55	HF	IS	On-track signal input
56	TER	IS	Tracking error signal input
57	FM+	O	Feed control signal (outward direction)
58	FM−	O	Feed control signal (inward direction)
59	FEOF	O	Feed servo OFF signal
60	TRHD	O	Tracking hold signal
61	TRGL	O	Tracking gain lowering signal
62	TROF	O	Tracking servo OFF signal
63	KP−	O	Kick pulse signal (inward direction)
64	KP+	O	Kick pulse signal (outward direction)
65	TRBK	I	Forced tracking brake signal
66	SVOF	I	Forced servo OFF signal
67	/FZC	I+	Focus error zero cross signal input
68	FCS	O	Focus start signal
69	FRF	I	Focus reflection signal
70	/XFSY	OD+	Crystal frame synchronous signal (7.35kHz)
71	/IC	IS+	Initial clear input
72	VDD		5V power supply (for logic block)
73	VSS		Ground (for logic block)
74	SLVL	OA	EFM slice level voltage output
75	EFMX	OA	Output for EFM duty detection (positive phase)
76	/EFMX	OA	Output for EFM duty detection (reversed phase)
77	EFMI	IA	EFM signal input
78	AVSS	A	Ground (for PLL block)
79	RREF	IA	Digital PLL driving clock generator constant current resistor connecting terminal
80	VCNT	IA	Digital PLL driving clock generator control terminal

Note 1) Symbols in the I/O column indicate as follows.
+ : pull up, − : pull down, D : open drain, T : 3-state, S : schmitt trigger, A : analog terminal
Note 2) For the structural reason, the same power should be supplied to each power supply terminal.

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

1. Clock Oscillation XIN, XOUT, CK4, 16M/33M, NO/DB

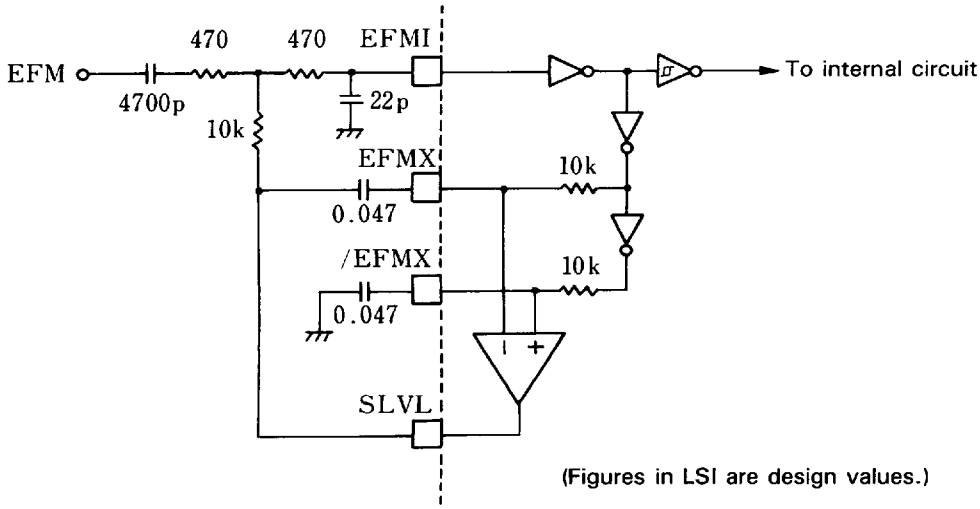
A crystal oscillation circuit is configured with both XI and XOUT terminals.
The oscillation frequency is 33.8688MHz(768fs) when playing at the double speed and 16.9344MHz (384fs) for normal play only. The master clock frequency and normal/double speed play are selected by 16M/33M and NO/DB terminals respectively.

16km/33M	NO/DB	Function
'H'	'H' or 'L'	Normal play (fXI=16.9344MHz)
'L'	'H'	Normal play (fXI=33.8688MHz)
'L'	'L'	Double speed play (fXI=33.8688MHz)

Also, a 4.2336MHz clock signal is output from the CK4 terminal.

2. Slice Level Control Circuit EFMI, EFMX, /EFMX, SLVL

RF signals are inputted from an optical pick-up of an appropriate level(1 to 2Vpp) into the EFMI terminal. The binary signals are output from /EFMX and EFMX terminals in opposite phases. Based on the fact that the average duty of EFM signals is 50%, the difference from these integrated signals is used to configure a circuit to control the slice level of RF signals.
To SLVL terminal, the amplitude difference between /EFMX and EFMX is output by the CMOS operational amplifier. A slice level control circuit can be configured by adding an appropriate time constant to both terminals.



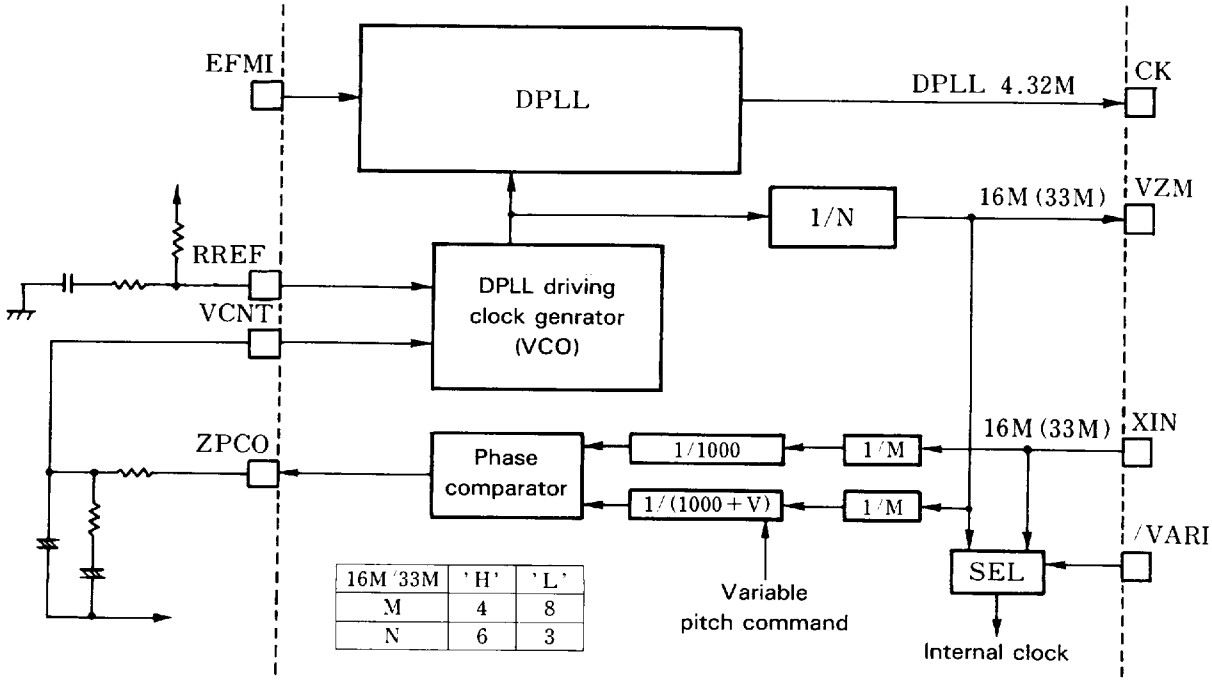
(Figures in LSI are design values.)

3. EFM Clock Regeneration Circuit ZPCO, VCNT, RREF, VZM, CK, /VARI

EFM clock regeneration of this LSI is done by the digital PLL circuit which is realized through digital signal processing, thereby conventionally necessary procedures such as PLL adjustment are now unnecessary.
The CK terminal outputs EFM regeneration clock signals(4.3218MHz on the average) generated in the digital PLL section.

This digital PLL section operates by the clock signals generated by the built-in frequency multiplier called DPLL driving clock generator. To multiply 384fs oscillation frequency by 6 (101.6064 MHz), an LPF is added between ZPCO and VCNT terminals. To RREF terminal, a resistor to determine the free run frequency for the DPLL driving clock generator is added. The clock signals from the generator are divided into 3 or 6 and output from the VZM terminal.

Setting the /VARI terminal to 'L' makes it possible to play at a variable speed within the range of 90% to 110%. During play at a variable speed, varying the dividing ratio of the phase comparator of the DPLL driving clock generator results in generation of clock signals whose pitch is offset from the crystal clock signals. Use of these signals for the system operation makes it possible to play at a variable speed without changing the crystal oscillation frequency. Command from the microprocessor are used for setting the speed. For normal speed play, /VARI should be set to 'H'.



16M /33M	'H'	'L'
M	4	8
N	6	3

4. Synchronous Equal Signal SYEQ

This is a check output terminal. It becomes 'H' when the external frame synchronous signal which detected 11T-11T from the inputted EFM pattern equals to the internal frame synchronous signal by the internal VCO-operated 588 counter.

The 588 counter has a window (588T ± 9T) and it is reset by the external frame synchronus signal that appears within this range. Also, if no external frame synchronous signal has been detected within the window for 12 times or more, the 588 counter is reset by the external frame synchronous signal.

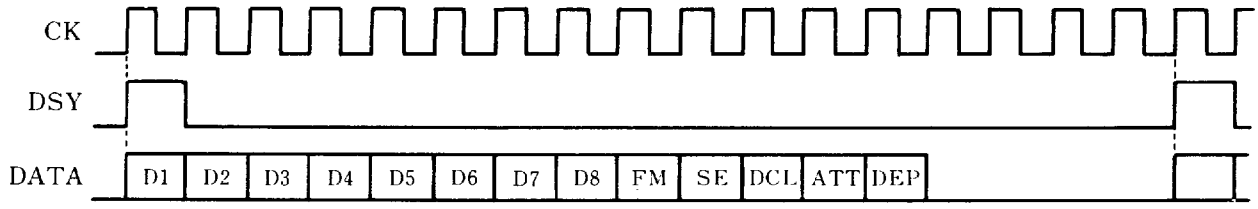
During playing, the internal signal PLLE is generated, which controls the control mode of the spindle motor by judging the status of this SYEQ signal.

With the frame whose SYEQ has become 'H', the internal SYEQ counter counts up by 4 and counts down by 1 at 'L'. As a result, when the counter indicates 1024, PLLE becomes '1' and then it becomes '0' at 767.

5. EFM Demodulation Signal Check Output DATA, DSY

The DATA consists of CK clock bit rate serial signals. Included in 17 bits are 8 bits of EFM demodulation signals and 5 bits of data control signals. DSY signals are synchronous signals that become 'H' when they are equal to the first signal of the DATA output. These terminals are used for checking.

These data cannot be read in the DSP mode described later on.



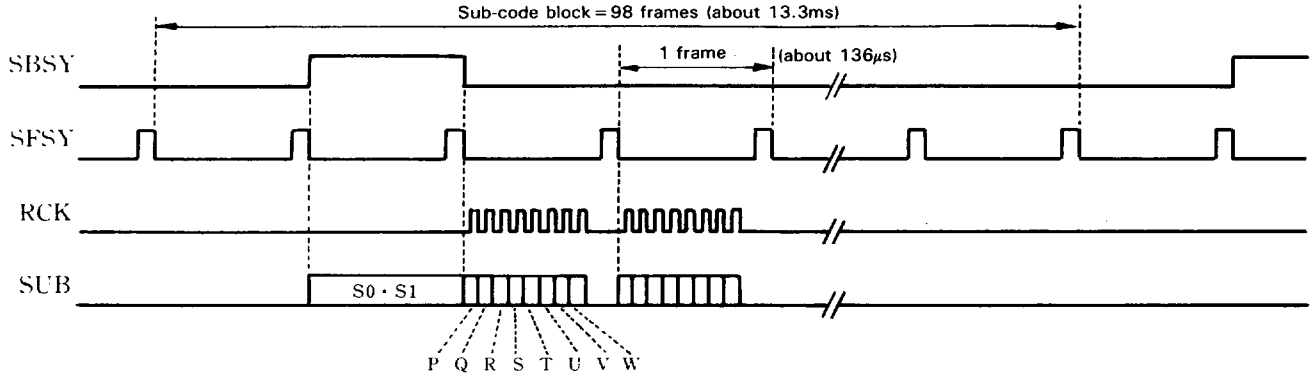
D1 ~ D8 : EFM demodulation signal
SE : RAM address setting signal
ATT : Sound volume 1/4 command
FM : 1st symbol of each frame
DCL : Sound volume 0 command
DEP : De-emphasis signal

6. Sub-code output SBSY, SFSY, RCK, SUB

These terminals output the sub-codes from the EFM signals for the system that uses the sub-codes conforming to EIAJ CP-309.

The SBSY terminal outputs the sub-code block synchronous signals and becomes 'H' during the sub-code frame 1(S1) period. The SFSY terminal outputs the sub-code frame synchronous signals that fall at the end of each frame. From the SUB terminal, a P code is output when the SFSY terminal falls and Q to W codes when clock signals to the RCK terminal rise respectively.

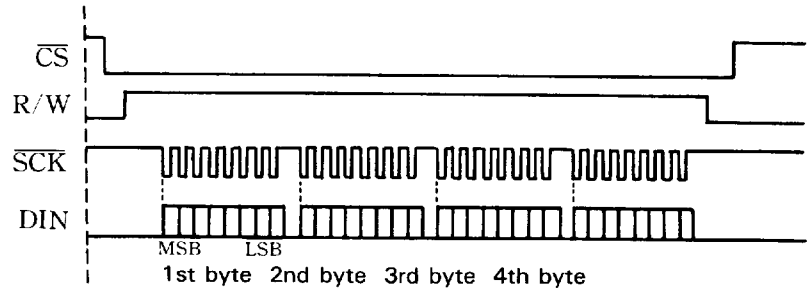
Also, at the P code period while SBSY is at 'H', a synchronous signal detection data ('H' when S0 and S1 are detected) is output. While SBSY is at 'H', S0 and S1 are output at P and R to W are not assured. The sub-code cannot be read while playing at the double speed.



7. Microprocessor interface /CS, R/W, /SCK, DIN, DOUT, WQ

7-1. Command input

Set R/W to 'H' and send the commands by the number of bytes specified follow to the DIN terminal, synchronously to /SCK. Commands are received only when /CS is 'L'.



• **Microprocessor Commands**

Code	Command		No. of bytes	Sound volume	Function
00H	STOP		1 Byte	0	Stop
01H	+1 TRACK KICK		1 Byte	0	1 track kick (outward)
11H	−1 TRACK KICK		1 Byte	0	1 track kick (inward)
08H	INITIAL SET		1 Byte	0	Software reset
20H	FEED FORWARD		1 Byte	0	Feed moving outward
30H	FEED RETURN		1 Byte	0	Feed moving inward
40H	FORCUS START		1 Byte	0	Focus search
5xH	EXTEND COMMAND	* 2	1 Byte	*3	Digital attenuator, setting for play at variable speed
60H	DISC START		1 Byte	0	Accelerating disc motor
70H	DISC BRAKE 1	* 4	1 Byte	0	Braking disc motor (by EFM pattern)
74H	DISC BRAKE 2	* 4	1 Byte	0	Braking disc motor (by Simulator)
80H	PLAY		1 Byte	1	Play
90H	PLAY MUTE		1 Byte	0	Play (Sound volume : 0)
A0H	FF		1 Byte	1/4	1 track fast forward
ACH	FF		1 Byte	0	1 track fast forward (Sound volume : 0)
B0H	FB		1 Byte	1/4	1 track fast backward
BCH	FB		1 Byte	0	1 track fast backward (Sound volume : 0)
C0H	FFF		1 Byte	1/4	10 tracks fast forward
CCH	FFF		1 Byte	0	10 tracks fast forward (Sound volume : 0)
D0H	FFB		1 Byte	1/4	10 tracks fast backward
DCH	FFB		1 Byte	0	10 tracks fast backward (Sound volume : 0)
E0H	SEARCH (PAUSE)	* 5	4 Bytes	0	ATIME auto search
F0H	TRACK COUNT	* 6	4 Bytes	0	Track count

*1 : Even if any command other than those listed above is inputted, the operation for that command is not assured.

*2 : EXTEND COMMAND

Code	Extend Command	Function
51H	VOLUME UP	Digital attenuator volume up (+0.4dB)
52H	VOLUME DOWN	Digital attenuator volume down (−0.4dB)
53H	VOLUME RESET	Resetting digital attenuator volume (0dB) (default)
54H	SOFT MUTE	Muting when upper 6 bits of both L and R channels all become '0' or '1'
55H	VOLUME FAST UP	Digital attenuator volume up (+6dB)
56H	VOLUME FAST DOWN	Diginal attenuator volume down (−6dB)
57H	MUTE OFF	Muting off (default)
59H	PITCH UP	Variable speed play pitch up (+0.1%) (effective when /VARI='L')
5AH	PICH DOWN	Variable speed play pitch down (−0.1%) (effective when /VARI='L')
5BH	PITCH RESET	Variable speed play pitch resetting (normal play) (default)
5CH	CAPTURE NARROW	DPLL narrow capture range (−6.6% to +6.6%)
5DH	CAPTURE WIDE	DPLL wide capture range (−15.5% to +17.7%)
5EH	CK4 OFF	CK4 terminal 'L' fixed, C1FLG output
5FH	CK4 ON	CK4 terminal clock output, C1C2FLG output (default)

*3 : Sound volume remains unchanged.

*4 : Judging parameters for stop vary. Use BRAKE1 normally.
DISC BRAKE 1 : Stop by means of FEM pattern check
DISC BRAKE 2 : Stop by means of motor simulator

*5 : For the SEARCH command, enter the target value (ATIME expressed with BCD codes) following E0H.

Bytes	1st	2nd	3rd	4th
Data	E0H	AMIN	ASEC	AFRAME

*6 : For the TRACK COUNT command, enter the target value (No. of tracks) following F0H.

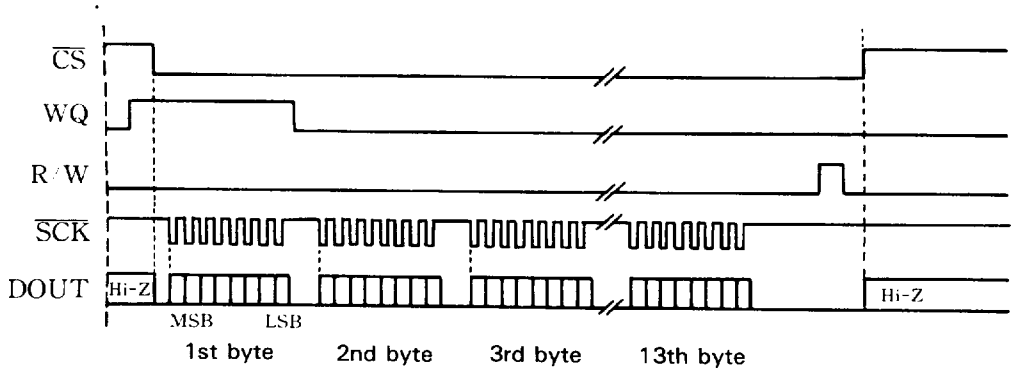
Bytes	1st	2nd	3rd	4th
Data	F0H	(No. of tracks)		00H

2nd Byte								3rd Byte							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
s	t7	t6	t5	t4	t3	t2	t1	t0	0	0	0	0	0	0	0

(No. of trackes)=16384•t7+8192•t6+4096•t5+2048•t4+1024•t3+512•t2+256•t1+128•t0
Direction : s=0 : Outward, s=1 : Inward

7-2. Internal status, Q code data output

When WQ='H' has been detected and /SCK is inputted with R/W as 'L', 1 to 13 byte data can be read from DOUT synchronously with that input.
DOUT output is available only when /CS='L'.
At WQ='H', it is necessary to read at least 1 byte of internal status and after that reading can be terminated at every 1 byte. Upon completion of reading, inform completion by setting the R/W signal up and down.
As a Q code occurs at every 13.3ms (every 6.67ms when double speed is used), data reading should be completed within this much time.
The internal status can be read even when WQ has not become 'H'. When in the AUTO SEARCH mode, completion of searching merely does not constitute a cause for WQ='H'. Therefore, it is necessary to monitor the internal status constantly.



- **Internal status, Q-code data**

Byte	Content
1	Internal status
2	CONT•ADR
3	TNO
4	X
5	E MIN
6	E SEC
7	E FRAME
8	P-CODE
9	A MIN
10	A SEC
11	A FRAME
12	Lch peak level
13	Rch peak level

- Data of the 2nd to 11th bytes except the 8th byte are in conformity with Q codes of RED BOOK.
- The 8th byte corresponds with the P code and becomes all '1' between songs and all '0' otherwise.
- The 12th and 13th bytes have the peak level of the L, R audio data absolute value in the upper 8 bits where no sign (MSB) is included. (Attenuator and internal de-empahsis are effective.) Only when DTFLG='L', SYEQ='H' and TSOF='L', comparison is performed by using the data inputted into the digital filter. The peak value is reset when these bytes are read.

• **Content of internal status (bit assignment for the 1st byte)**

	MSB	b6	b5	b4	b3	b2	b1	LSB
	MODE STATUS					MZ	FCO	NQ
NORMAL MODE	1	1	1	1	1			
SEARCH MODE (E0H)	SIGN	S2	S1	8F	4F			
AT TRACK COUNT(F0H) END	1	0	0	0	0			

MZ : Disc motor stop ('1' at stop)
FCO : Focus out ('1' at OUT)
NQ : New Q code detect ('1' when a new Q code is set. 2nd to 11th bytes are available.)

SIGN : Search direction
S2, S1 : Search mode
8F, 4F : Frame error

• **Conditions for WQ to become 'H'**

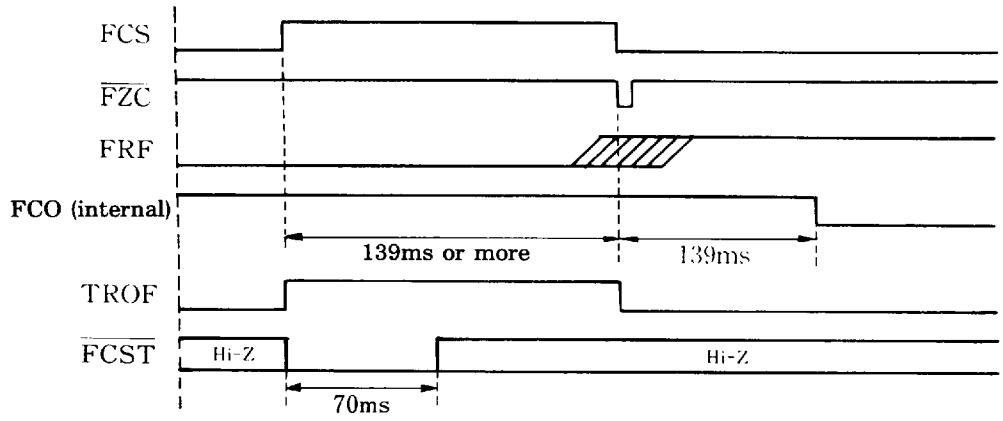
1) When the disc motor has started running or it has stopped
2) When focus is applied or it is dropped
3) When a new correct Q code is set in the internal register
4) When track counting has completed
5) When 1 track kick has completed

WQ is reset when 1 byte has been read.

8. **Related to focus servo /FZC, FRF, FCS, TROF, /FCST**

These terminals are used to lead in the focus servo.

When the command is sent, the instruction signal FCS for leading in the focus becomes 'H'. After that, when /FZC becomes "L" which occurs when the focus point has been reached, leading in operation is stopped (FCS='H'→'L') and that is informed to the microprocessor with the internal status FCO set to '0' by the FRF signal which has detected the mirror. Also, when the focus is led in, the TROF terminal becomes 'H' so that the tracking servo is turned OFF.



10μs or more is necessary for /FZC='L' time at the focus point. The /FZC terminal input is not sensed for 139ms after the FCS terminal became 'H'.

After FCO has become '0', if FRF becomes 'L', focussing is judged as being dropped and that is informed to the microprocessor by using FCO='1'.

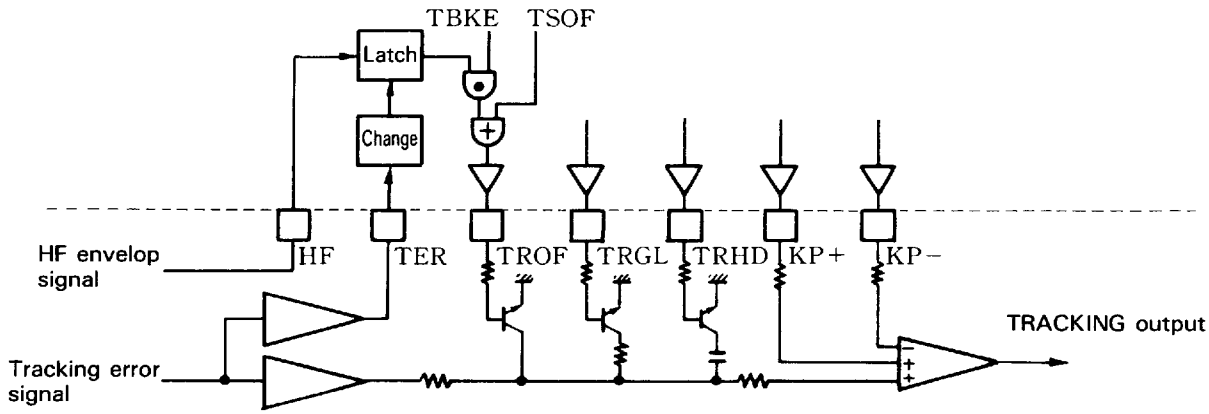
9. **Related to tracking servo HF, TER, TROF, TRGL, TRHD, KP+, KP−, SVOF, TRBK**

These terminals generate timing signals to execute a track jump according to commands.

While kick pulse signals KP+(forward) and KP−(rearward) are being output, TRHD becomes 'H' and the tracking error signal is held. TRGL outputs signals to raise tracking gain after kicking and it remains at 'H' during normal gain. TROF outputs signals to cut off the servo loop.

SVOF signals is used to turn OFF the tracking servo and feed servo. When it is 'H', TROF and FEOF become 'H' and TRHD, KP+ and KP− become 'L'.

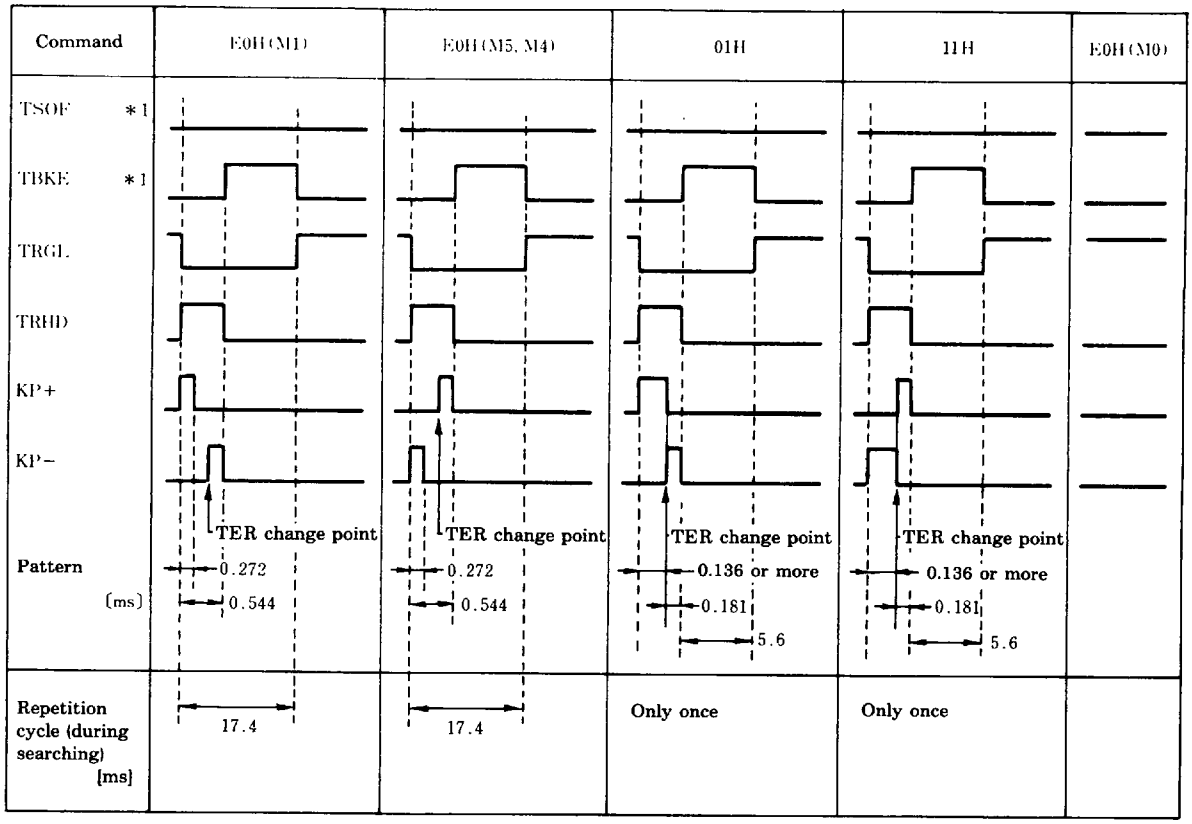
TRBK signals is used to apply tracking brake from outside. At 'H' input, TRGL becomes 'L' and internal control signal TBKE becomes 'H'.



• **Track jump timing (1)**

Command	A0H	B0H	C0H, E0H (M2)	D0H, E0H (M6)	E0H (M3) *2	E0H (M7) *2
TSOF *1						
TBKE *1						
TRGL						
TRHD						
KP+						
KP−						
Pattern [ms]	0.272 0.544 17.4	0.272 0.544 17.4	0.816 1.497	0.816 1.497	2.993 5.714	2.993 5.714
Repetition cycle [ns]	104	47.9	104	104		
Repetition cycle (during searching) [ns]			17.4	17.4	34.8	34.8

• **Track jump timing (2)**

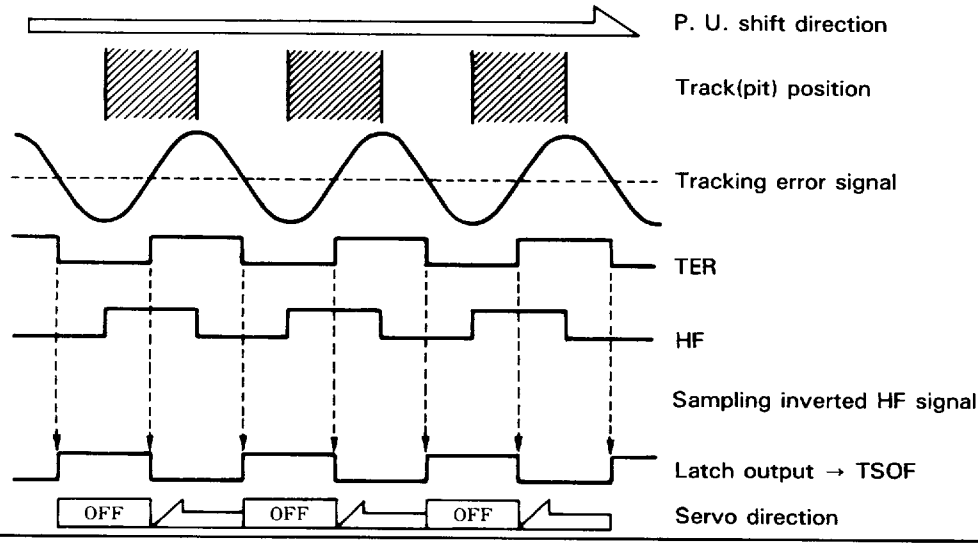


*1 : TSOF(Tracking Servo Off) and TBKE(Tracking Brake Enable) are internal signals.
*2 : FM+, FM− and FEOF outputs are shown in a separate diagram.

• **Tracking Brake Operation**

Changes in the amplitude of the HF signals generated when the track is crossed during searching are sampled at the zero cross point of tracking error signals (edge of TER signal) and using this signal the TROF signal is output.

Tracking servo is turned ON (TROF= 'L') and OFF(TROF= 'H') by this signal to operate the tracking brake so that the track can be grasped easily.



• **Auto search(E0H) operation**

The auto search command operates while selecting internally the optimum kick pulse according to the time difference between the target time attached to the command and the current time based on the Q code which has been read.

There are 8 types of kick pulses (M0 to M7) and they are called "search mode" respectively. According to the Q code which has been read immediately after the search command was started, the schedule of how often the kick pulse of each search mode is repeated is determined and its execution is started. When a new Q code is read during execution, the schedule is determined again. The search mode to be used is as follows.

(time difference)=(target ATIME)−(current ATIME)>0 : Search outward ; M3→M2→M1→M0
(time difference)=(+128)*N3/2+(+4)*N2+(+1/4)*N1 [S]

(time difference)=(target ATIME)−(current ATIME)<0 : Search inward ; M7→M6→M5→M4→M0
(time difference)=(+128)*N7/2+(−4)*N6+(−1/4)*N5 +N4 [S]

*1 : N7, N6, ... N1 indicate the number of times each search mode is repeated.
*2 : M4 is used to return to prior to the target time.

Since ATIME which is read by the microprocessor is used as a current time, even a new Q code is detected internally, neither its schedule is determined nor operation is started unless it is read. Even when the schedule is determined again or another command is received, operation is not terminated during the timing cycle of these search modes.

While searching takes place, which search mode is being executed and the frame difference can be known by the mode status.

SIGN	S2	S1	MODE	Time difference [s]
0	0	0	M0	~+1/4
0	0	1	M1	+1/4~+4
0	1	0	M2	+4~+128
0	1	1	M3	+128~
1	0	0	M4	~−1/4
1	0	1	M5	−1/4~−4
1	1	0	M6	−4~−128
1	1	1	M7	−128~

8F	4F	Frame difference
0	0	
0	1	4/75 seconds (4 frames)
1	0	8/75 seconds (8 frames)
1	1	12/75 seconds (12 frames)

Highly accurate kicking is possible for 1 track kick (E0H M1, M5) during auto searching and 1 track kick command (01H, 11H), because the TER signal edge is detedted.

• **Track count (F0H) operation**

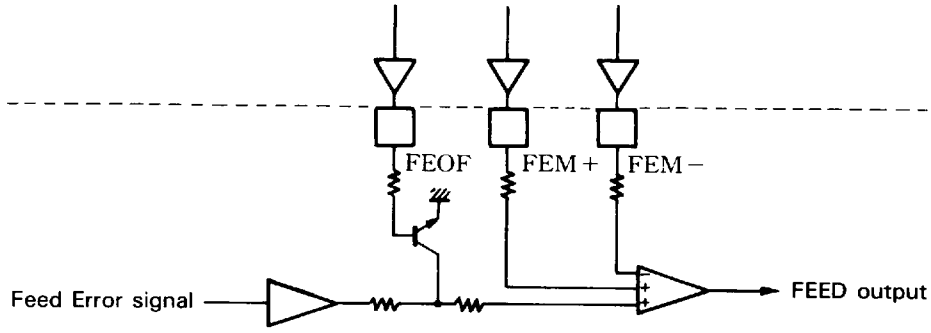
The track counting is a function to bring the search target to a higher speed by counting the rise edge of the TER signals which occur when the track is crossed by the pick-up which is moved by turning OFF the tracking servo and feeding the P.U.

When a command is given, FM+ or FM− signal is output at the same time as TROF becomes 'H'. Rising of the TER signal is counted and when the number counted becomes equal to the target value, counting is terminated and that is informed to the microprocessor. After that, the status is same as that of PLAY MUTE.

To interrupt track counting, the track count command with the track number '0' should be inputted. Note that after counting is over, the status is PLAY MUTE but WQ request by NQ is masked.

10. Related to Feed Servo FEOF, FM+, FM−

FM+ or FM− signals are output as feeding signals to move the pick-up and during this time, FEOF='H' is output to turn OFF the feed servo.



- **Feed output timing**

Command	00H, 40H, 60H, 70H	20H	30H	80H, 90H, A0H, B0H, C0H, D0H, E0H(M0~M2) E0H(M4~M6)	E0H(M3)	E0H(M7)
FEOF FM+ FM−						
Repetition cycle [ms]					34.8	34.8

11. Related to Disc Servo DM+, DM−

DM+ and DM− terminals are provided to control the disc motor speed. They PWM-output : DM+='H' during acceleration and DM-='H' during deceleration. Resolution of PWM is 1/144 of one frame and the maximum value is 128/144.

• Command and disc servo internal operation mode

The disc motor control operates while selecting the control mode according to the given commands and the internal conditions.

<table>
<tr><td colspan="2">Command</td><td>00H
20H
30H</td><td>40H</td><td>60H</td><td colspan="4">80H, 90H,
A0H, B0H, C0H, D0H,
E0H, F0H</td><td>70H</td></tr>
<tr><td rowspan="3">Internal signal *1</td><td>FCO</td><td rowspan="3">—</td><td rowspan="3">—</td><td rowspan="3">—</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="3">—</td></tr>
<tr><td>TSOF</td><td>0</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td>PLLE</td><td>0</td><td>1</td><td>—</td><td>—</td></tr>
<tr><td rowspan="4">Motor simulator output value</td><td>High speed</td><td colspan="7">OFF</td><td rowspan="3">BRK</td></tr>
<tr><td>Medium speed</td><td rowspan="2">OFF</td><td rowspan="2">HOLD</td><td rowspan="3">ACC</td><td>AFC</td><td>PLL</td><td rowspan="2">OFF</td><td rowspan="2">HOLD</td></tr>
<tr><td>Low speed</td><td colspan="2" rowspan="2">ACC</td></tr>
<tr><td>Reverse</td><td colspan="2">OFF</td><td colspan="2">OFF</td></tr>
</table>

*1 : Internal signal

FCO : Focus Out

TSOF : Tracking Servo OFF

PLLE : PLL Enable

Operation of each mode is as follows.

ACC : 128/144(maximum value) is output to DM+.

AFC : Frequency of EFM signal in the maximum inverting width is compared by /XFSY. 128/144(maximum value) or 0 is output to DM+, DM−.

PLL : Phase is compared with frame synchronous signal by /XFSY and VCO. PWM output is used for DM+ and DM−.

OFF : Both DM+ and DM− output 0.

HOLD : PWM output is used for DM+ and DM− so as to hold the current speed by means of the motor simulator.

BRK : 128/144(maximum value) is output to DM− till the stop condition is given.

12. **Crystal clock synchronous signal /XFSY**

/XFSY is a 7.35kHz(14.7kHz at double speed) frame synchronous signal generated from the XI clock.

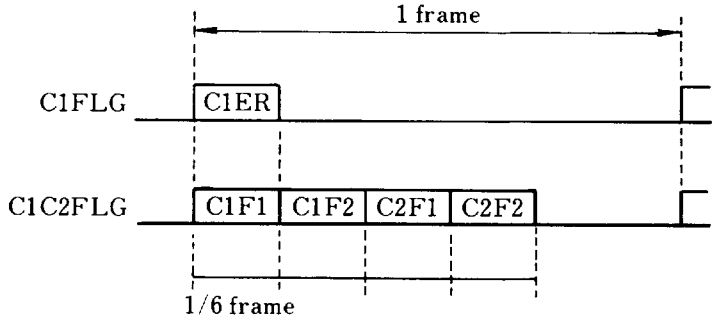
13. **C1, C2 error correction check signal DTFLG/CFLG,/TESTI**

The DTFLG/CFLG terminal outputs an error flag DTFLG signal which indicates that the SDO output has undergone interpolation or preceeding data hold processing. When the /TESTI terminal is set to 'L', it outputs a check signal C1FLG or C1C2FLG to indicate the operation condition of the C1, C2 correction circuit.

/TESTI	Command	DTFLG/CFLG terminal output
'H'	–	DTFLG signal
'L'	5EH	C1FLG signal
'L'	5FH	C1C2FLG signal

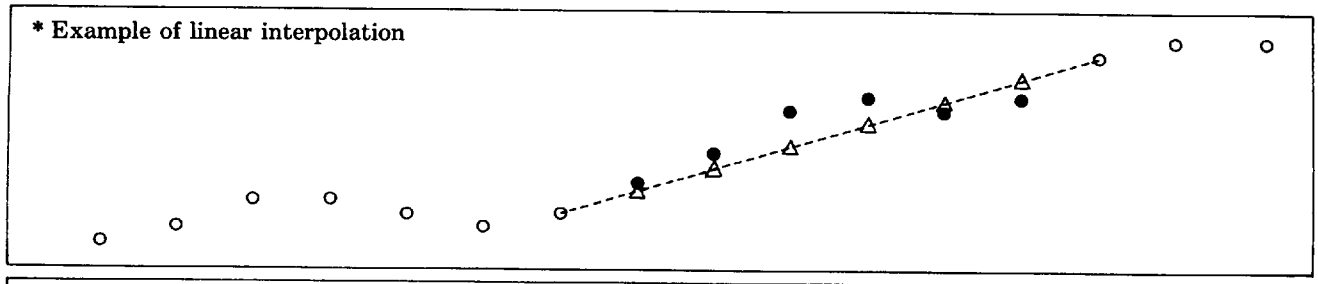
C1ER	C1 correction status
L	No C1 error
H	C1 error exists

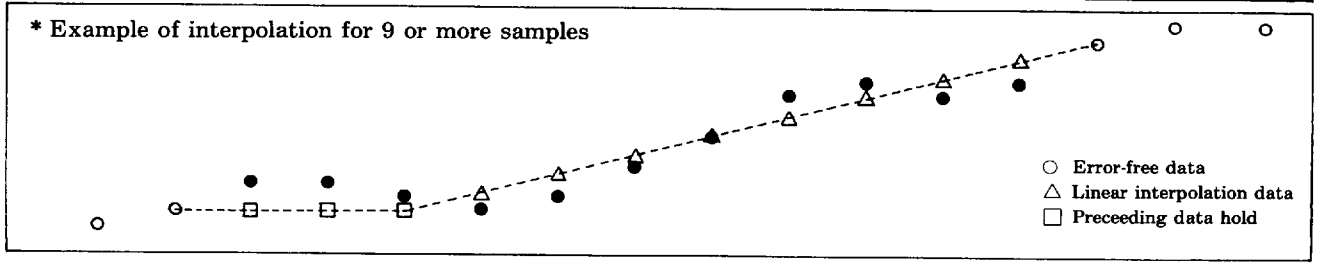
C1F2	C1F1	C1 correction status
L	L	No error
L	H	Single error corrected
H	L	Double error corrected
H	H	Uncorrectable



C2F2	C2F1	C2 correction status
L	L	No error
L	H	Single error corrected
H	L	Double error corrected
H	H	Uncorrectable

The data which could not be corrected by the C1 or C2 error correction circuit undergo linear interpolation processing if they are consecutive errors up to 8 and preceeding data hold processing if they are over 8 consecutive errors.





Whether interpolation has been executed or not can be monitored by using the DTFLG signal. If the 16-bit data which is output from the SDO has undergone interpolation, 'H' is kept during that time. In the CD-ROM and DSP modes, which are described later, however, if there are uncorrectable data among the upper and lower 8 bits of the 16-bit data of each sample which is output from the SDO, 'H' is kept during that time.

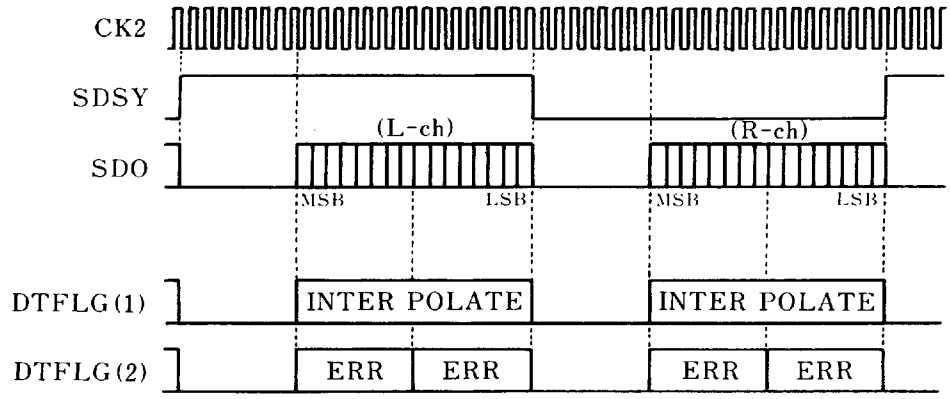
14. Audio Data Output **/MODE1, MODE0, CK2, SD0, SDSY, DEP, CK2I, SDSYI, SDI**
DAC Related **ZDT, AOLL, AOLH, AORL, AORH, LVDD, LVSS, RVDD, RVSS**

/MODE1 and /MODE0 are audio data output mode setting terminals.

/MODE1	/MODE0	Mode	SDO				DAC
			Command sound volume	Inter-polation	Attenuator	Zero cross mute	
'H'	'H'	NORMAL	○	○	○	○	Operation
'H'	'L'	DSP	△ *1	○	× *2	○	Operation (SDI signal is used)
'L'	'H'	EXDAC	○	○	○	○	No Operation
'L'	'L'	CD-ROM	×	×	×	×	No Operation

*1 : 1/4 sound volume is valid but 0 sound volume is invalid.
*2 : Attenuation processing is performed on the SDI input signals.

The MSB fast 16 bit serial data are output by CK2, SDO and SDSY signals.



Note) DTFLG(1) is used when in NORMAL and EXDAC modes and DTFLG(2) is used when in CD-ROM and DSP modes.

The de-emphasis data is output from the DEP terminal. This reflects the control bit of the Q code and it is renewed when CRC check of the Q code has resulted in PASS during operation with the sound volume set to other than "0".

This LSI has built-in 2 channels of the 3rd order noise shaping 1-bit DAC with 128fs operation. CK2I, SDSYI and SDI are DAC input terminals when in the DSP mode and the same format data as SDO are taken in through them.

Note that when in the DSP mode, digital attenuation processing is performed on the SDI input and is not reflected on the SDO output. When in any other mode, this terminal is not used and therefore the SDI terminal should be connected with VSS.

After the digital de-emphasis processing, the audio data undergoes oversampling by the 18-bit, 8-times digital filter and pulse density modulation by the 3-order noise shaper and then are stream output through the AOLL and AOLH terminals for the L channel and through the AORL and AORH terminals for the R channel.

The ZDT is a 1-bit DAC operation mode setting terminal.

The operation is determined according to the ZDT level at initial clear.

ZDT	1-bit DAC operation
'L'	Internal zero detect mute operation is performed.
'H'	Internal zero detect mute operation is not performed. The zero data is detected and output from the ZDT terminal ('H' when detected)

For power reinforcement, power supply pins are provided for the 1-bit DAC section. LVDD and LVSS pins are for the L channel and RVDD and RVSS pins are for the R channel. Due to the structural reason of the LSI, however, the same power supply should be used. The DAC does not operate in EXDAC and CD-ROM modes.

15. Digital Attenuator, Digital De-emphasis

A digital attenuator with 0.4dB resolution and 240 steps is built in. Its setting is done through the microprocessor interface.

When in NORMAL and EXDAC modes, attenuation processing is performed on the data immediately before the SDO output.

When in the DSP mode, attenuation processing is performed on the SDI input data.

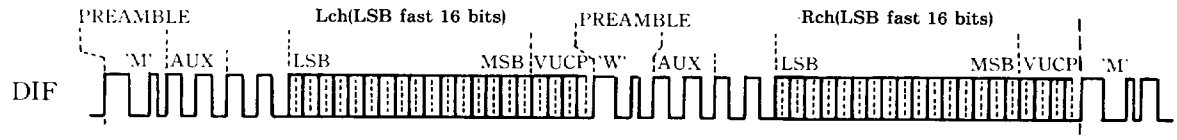
When in the CD-ROM mode, the digital attenuator becomes invalid.

Also, it does not operate for the DIF signals.

If the CONT data of the demodulated Q code is '***1', de-emphasis processing is performed immediately before the oversampling filter. De-emphasis processing is not reflected for the SDO output.

16. Digital Audio Interface Output DIF

The DIF terminal output is a digital audio interface format output which conforms to the EIAJ format and modulated bi-phase, including the C and U bit.



The audio data varies according to the sound volume and zero cross mute in the command. When the sound volume is "0" and muting is used, the audio data becomes all zero.
The category code for the C bit is '10000000' indicating CD.
When the sound volume command is other than '0', the control bits (4 bits) of the Q code are copied when the CRC check of the Q sub-code has resulted in PASS. The data remains unchanged for any other command.
The U bit includes sub-code data(Q to W).
When 80H or 90H command is used, the sub-code is output when it was received internally. The U bit data is not assured for any other command.
The V bit becomes '1' only when uncorrectable error data has occurred. It does not become '1' when the sound volume is 1/4 or 0, or when the data is muting.
When a Q sub-code error has occurred, C bit is sent out the preceeding data hold and U bit regardless of the error.
The DIF output becomes 'L' when playing at double speed.

17. Initial Clear /IC, /TESTE

This LSI requires initial clear processing when the power rises.
/IC should be set to 'L' for 400μs or longer after the clock is inputted to XIN with the VDD at a specified voltage.
/TESTE is an LSI test terminal and should be used with unconnected.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD}+0.5	V
Operating temperature	T_{op}	−20 ~ 75	°C
Storage temperature	T_{stg}	−50 ~ 125	°C

2. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{op}	0	25	70	°C

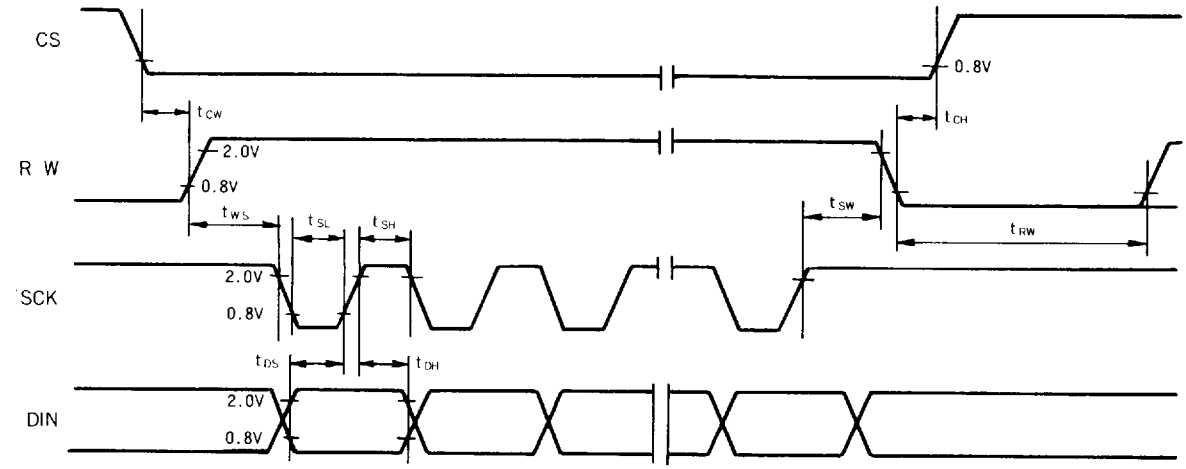
3. DC characteristics

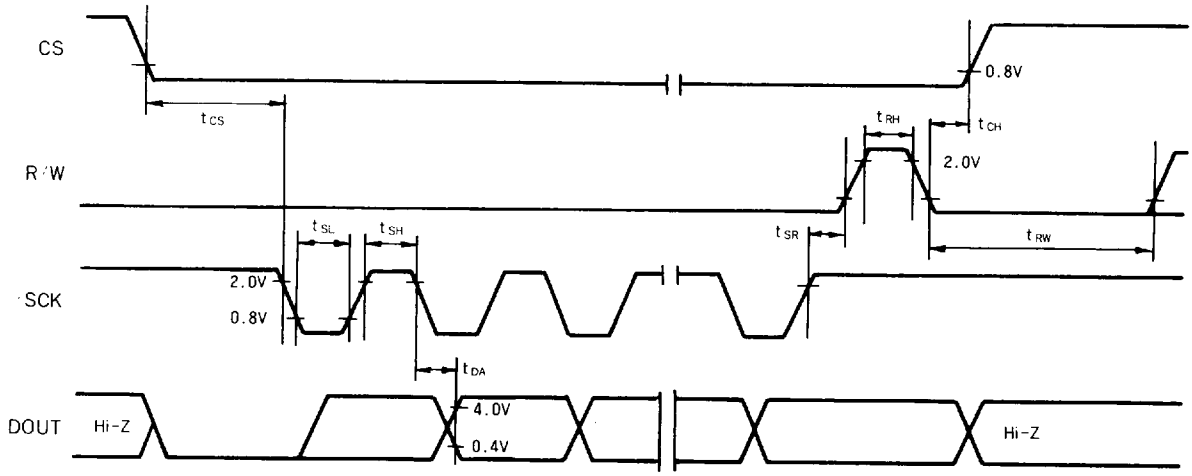
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{DD}	V_{DD}=5.0V		80	90	mA
Input voltage L level (1)	V_{IL1}	*1			0.8	V
Input voltage H level (1)	V_{IH1}	*1	2.0			V
Input voltage L level (2)	V_{IL2}	*2			1.0	V
Input voltage H level (2)	V_{IH2}	*2	3.5			V
Input leakage current	I_{LK}	V_I=5.0V, *3		0.1	1	μA
Input capacitance	C_I			5		pF
Output voltage L level	V_{OL}	I_{OL}=1mA, *4			0.4	V
Output voltage H level	V_{OH}	I_{OH}=−0.1mA, *4	4.0			V
Input capacitance	C_O			5		pF

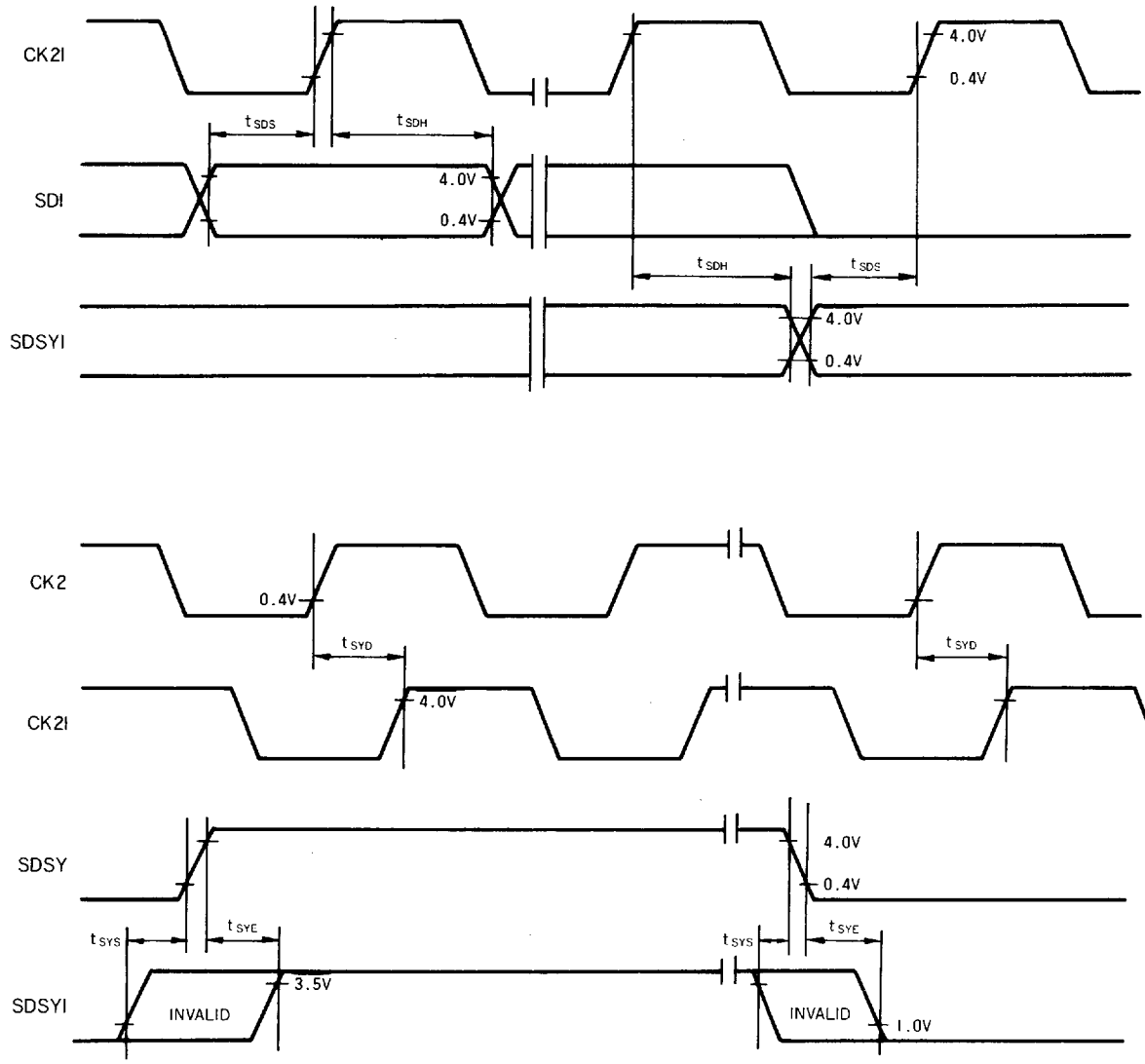
*1) Applicable to /CS, R/W, /SCK, DIN and SDI terminals.
*2) Applicable to input terminals excluding analog terminals and other than the above.
*3) Applicable to input terminals excluding terminals with a pull-up resistor.
*4) Applicable to all output terminals.

4. AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
XIN frequency	fXI		16.9344	33.9	MHz
/CS setup time 1	tCW	0.5			μs
/CS setup time 2	tCS	1			μs
/CS hold time	tCH	0.5			μs
R/W setup time 1	tWS	0.5			μs
R/W setup time 2	tSR	12		135	μs
R/W hold time 1	tSW	12			μs
R/W hold time 2	tRH	0.5			μs
R/W cycle time	tRW	408			μs
/SCK L level time	tSL	0.5		8	μs
/SCK H level time	tSH	0.5			μs
DIN setup time	tDS	0.4			μs
DIN hold time	tDH	0.4			μs
DOUT access time	tDA	0.4			μs
SDI, SDSYI setup time					
(at normal speed)	tSDS	80			ns
(at double speed)		80			ns
SDI, SDSYI hold time					
(at normal speed)	tSDH	80			ns
SDSYI CK2I delay time					
(at double speed)		80			ns
SDSYI CK2I delay time					
(at normal speed)	tSYD	0		250	ns
(at double speed)		0		30	ns
SDSY transition start time					
(at normal speed)	tSYS			4.5	μs
(at double speed)				2.1	μs
SDSY transition end time					
(at normal speed)	tSYE			3.5	μs
(at double speed)				1.7	μs





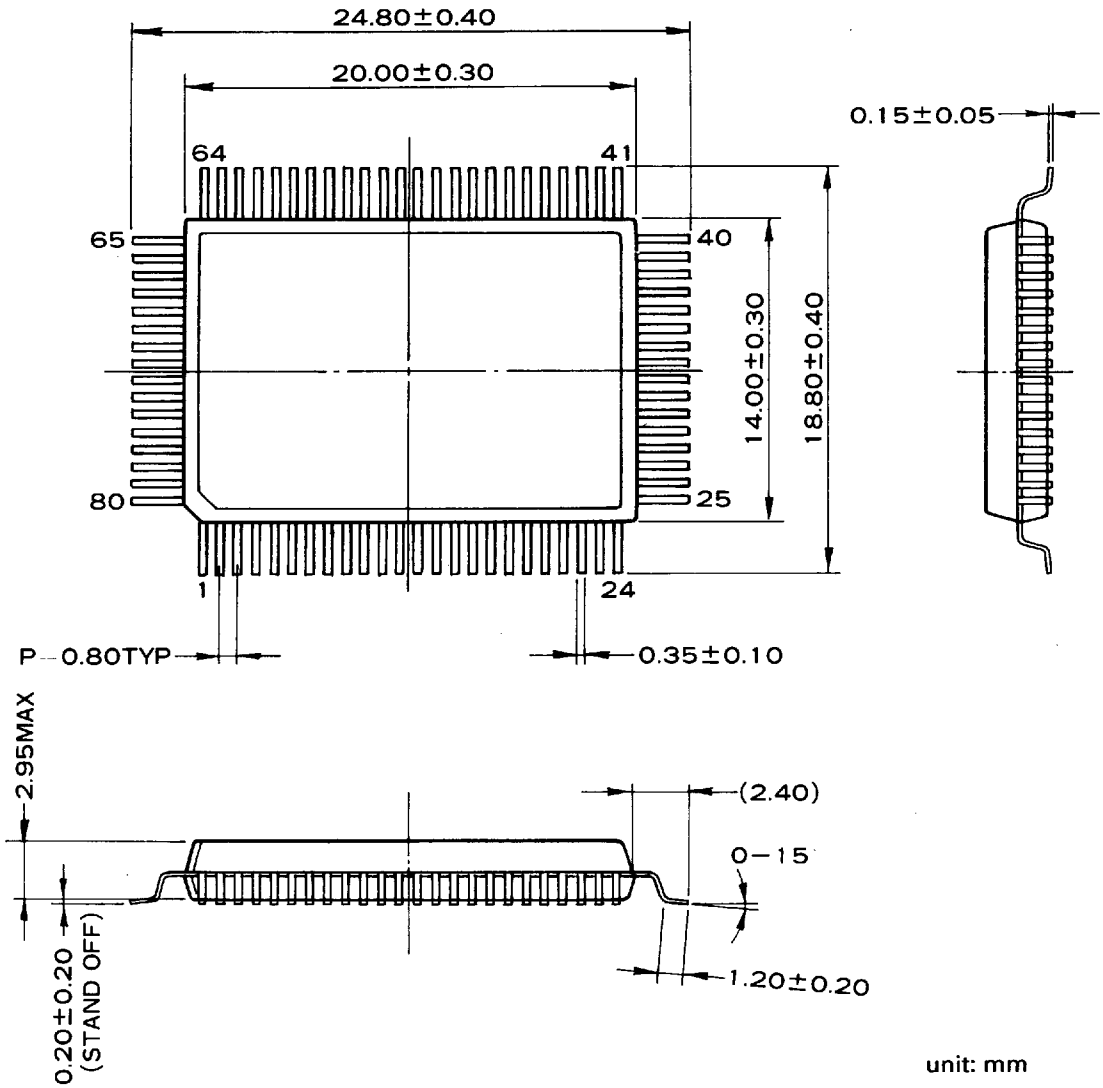


5. Analog Characteristics (Condition : V_{DD}=5.0V, Top=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VCO for DPLL driving clock						
VZM free run frequency	f_{VF}	V_{CNT}=2.5V, *1		18.8		MHz
Oscillation frequency (1)	f_{VCO1}	V_{CNT}=4.0V, *1		8.8	13.5	MHz
Oscillation frequency (2)	f_{VCO2}	V_{CNT}=1.0V, *1	20.3	26		MHz
Frequency conversion gain	G_{VCO}	V_{CNT}=2.5V, *1		−3.0		MHz/V
Op-amp. for SLC						
Open loop gain	G_{open}	RL=4.7kΩ	70	75		dB
Input offset voltage	V_{ofs}	RL=4.7kΩ			7.0	mV
Through rate	SR	RL=4.7kΩ	1.0	2.0		V/μs
DAC						
Total Harmonic Distortion	THD+N	1kHz, 0dB, *2		0.0025		%
Dynamic Range	DR	*2		95		dB
Signal to Noise ratio	S/N	*2		100		dB

*1 : RREF=15kΩ, 16M/33M='H'
*2 : On evaluation circuit of YAMAHA

■ DIMENSIONS



Note : The LSIs for surface mount need especial consideration on strage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

The specifications of this product are subject to improvement changes without prior notice.