YM7306C

Dolby Pro Logic Decoder (DPLD)

■ OUTLINE

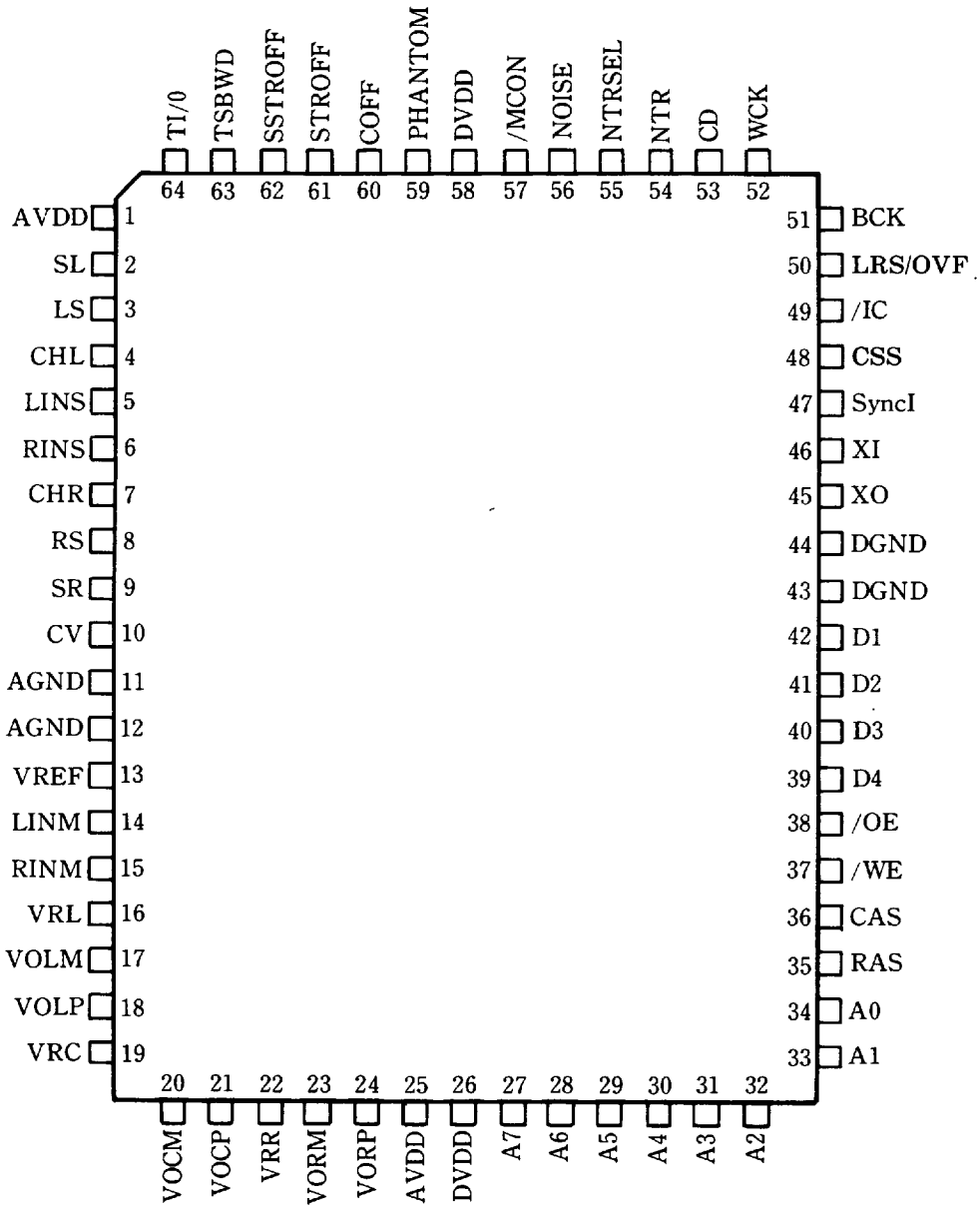
This LSI is a Dolby Pro Logic decoder based on latest Digital Signal Processing technology. The LSI is capable of digital signal processing for almost all functions needed in Pro Logic. This allows construction of a highly reliable decoder with a small quantity of components.
This LSI also has a sound field simulation circuit with 12 digital delay lines (370 ms at max.), which allows you to design a 2in-4out surround system easily.

■ FEATURES

- Highly accurate signal processing with internal operation word length of 32 bits
- Adaptive matrix, noise sequencer, 7 KHz low pass filter, modified B-type N.R. decoder and A/D & D/A converter are built-in.
- Sound field simulation function using digital delay (maximum delay time: 370 ms)
- External 256K DRAM interface for 16 bits linear digital delay (page mode access)
- Serial interface with microprocessor for parameter control.
- Analog signal processing for the front three channels.
- Master clock frequency is 8.46 MHz and sampling frequency is 44.1 KHz.
- Interface signal output for Automatic Balance Control.
- Dolby reference operate level 300 mVr.m.s.
- 64 pin QFP package, silicon gate CMOS, 5V power supply.

(Note)
Dolby is a trademark of Dolby Laboratories Licensing Corporation. This IC is available only to licensees of Dolby Laboratories Licensing Corporation.

■ PIN CONFIGURATION



■ PIN DESCRIPTIONS

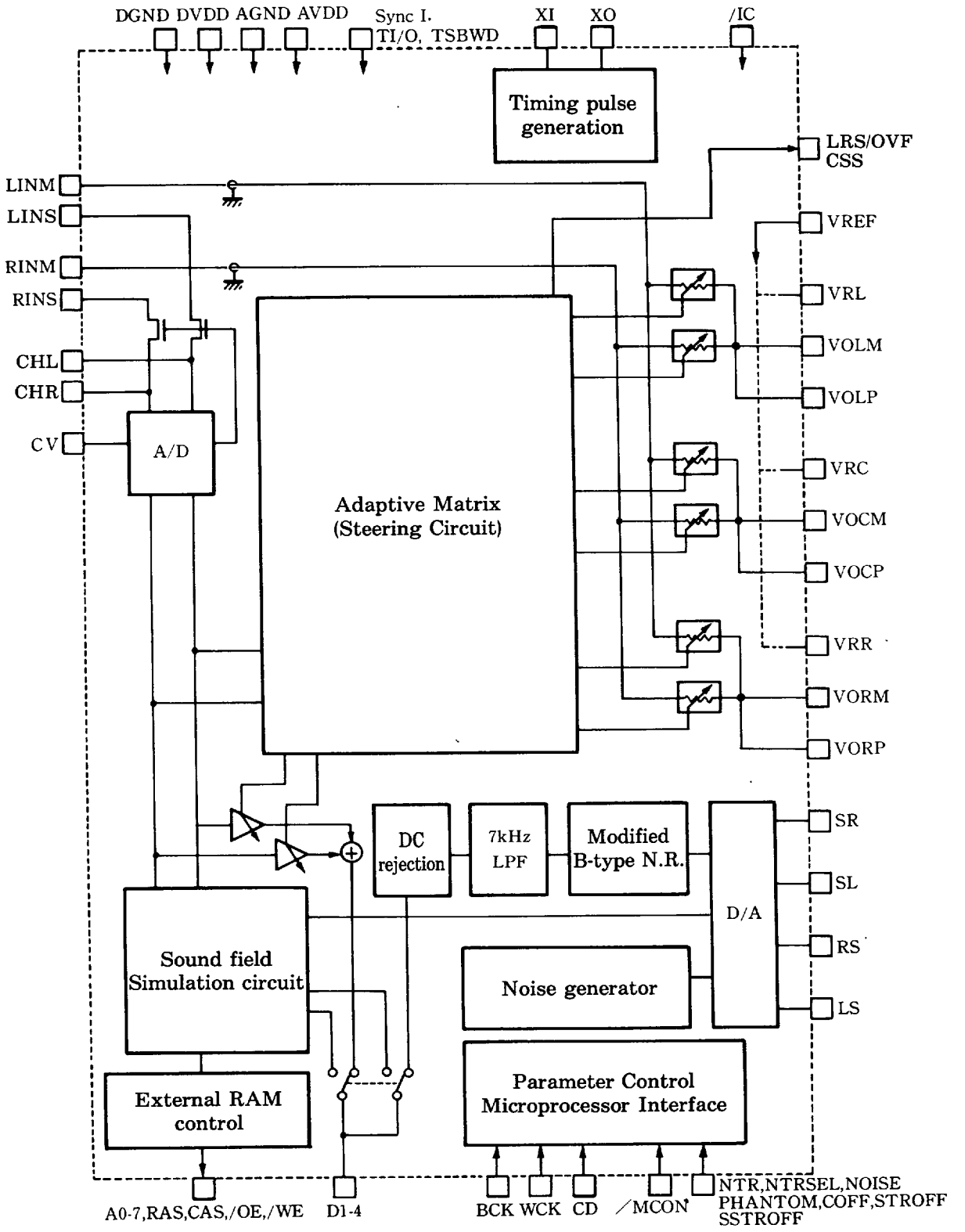
Pin	I/O	Pin name	Description
1	A–	AVDD	+5V power supply (for D/A & A/D converter)
2	AO	SL	SL channel, D/A output
3	AO	LS	LS channel, D/A output
4	A–	CHL	Sample/hold capacitor terminal for LINS input
5	AI	LINS	L channel, A/D input
6	AI	RINS	R channel, A/D input
7	A–	CHR	Sample/hold capacitor terminal for RINS input
8	AO	RS	RS channel, D/A output
9	AO	SR	SR channel, D/A output
10	AO	CV	Center voltage of A/D, multiplying DAC
11	A–	AGND	Ground (for D/A & A/D converter)
12	A–	AGND	Ground (for multiplying DAC)
13	AI	VREF	Reference voltage input of multiplying DAC
14	AI	LINM	L channel, Multiplying DAC input
15	AI	RINM	R channel, Multiplying DAC input
16	AI	VRL	Reference voltage input of multiplying DAC
17	AO	VOLM	Connected to L channel, Operational amplifier, – terminal
18	AO	VOLP	Connected to L channel, Operational amplifier, + terminal
19	AI	VRC	Reference voltage input of multiplying DAC
20	AO	VOCM	Connected to C channel, Operational amplifier, – terminal
21	AO	VOCP	Connected to C channel, Operational amplifier, + terminal
22	AI	VRR	Reference voltage input of multiplying DAC
23	AO	VORM	Connected to R channel, Operational amplifier, – terminal
24	AO	VORP	Connected to R channel, Operational amplifier, + terminal
25	A–	AVDD	+5V power supply (for multiplying DAC)
26	–	DVDD	+5V power supply (for digital processing circuit)
27	O	A7	Address 7 for external delay RAM
28	O	A6	Address 6 for external delay RAM
29	O	A5	Address 5 for external delay RAM
30	O	A4	Address 4 for external delay RAM
31	O	A3	Address 3 for external delay RAM
32	O	A2	Address 2 for external delay RAM
33	O	A1	Address 1 for external delay RAM
34	O	A0	Address 0 for external delaly RAM
35	O	RAS	RAS for external delay RAM
36	O	CAS	CAS for external delay RAM
37	O	/WE	WE for external delay RAM, write enable terminal
38	O	/OE	OE for external delay RAM, output enable terminal
39	I/Ot	D4	Data 4 for external delay RAM
40	I/Ot	D3	Data 3 for external delay RAM
41	I/Ot	D2	Data 2 for external delay RAM
42	I/Ot	D1	Data 1 for external delay RAM
43	–	DGND	Ground (for digital circuit)

Pin	I/O	Pin name	Description
44	–	DGND	Ground (for digital circuit)
45	O	XO	X'tal oscillator terminal (8.4672 MHz)
46	I	XI	X'tal oscillator terminal (8.4672 MHz)
47	It	Sync I	Test terminal to be usually connected to DVDD
48	O	CSS	Auto input balance enable signal out
49	Ics	/IC	Initial clear terminal (power on resetting is required).
50	O	LRS/OVF	Dolby-Pro-Logic mode; Auto input balance L, R steering signal out Sound field simulation mode; LSI test terminal (overflow detect)
51	Its	BCK	Bit clock for parameter data input
52	Its	WCK	Word clock for parameter data input
53	Its	CD	Serial data for parameter data input
54	Its	NTR	Noise switch pulse input (pulled up) When this terminal shifts from H to L, noise output channel switches as L→C→R→S
55	Its	NTRSEL	Noise change mode select (pulled up) "H" to use NTR, "L" to use AUTO change
56	Its	NOISE	Noise on/off select (pulled up) "L"=on, "H"=off
57	Its	/MCON	Control mode select (pulled up) "L"=Dolby-Pro-Logic mode "H"=Parameters can be controlled by microprocessor
58	–	DVDD	+5V power supply (for digital circuit)
59	Its	PHANTOM	Phantom mode select (pulled up) "L"=Phantom is on (With center output is off) "H"=Phantom is off
60	Its	COFF	Center output select (pulled up) "L"=Center output is off "H"=Center output is on
61	Its	STROFF	Steering select (pulled up) "L"=Steering is off "H"=Steering is on
62	Its	SSTROFF	Surround steering select (pulled up) "L"=Surround steering is off (3 channel logic) "H"=Surround steering is on
63	Ic	TSBWD	LSI test terminal, to be usually connected to DVDD
64	Ic	TI/O	LSI test terminal, to be usually connected to DVDD

Note 1) Meaning of column I/O symbol:
I : Input terminal O : Output terminal A : Analog terminal
t : TTL level c : CMOS level s : Schmidt input

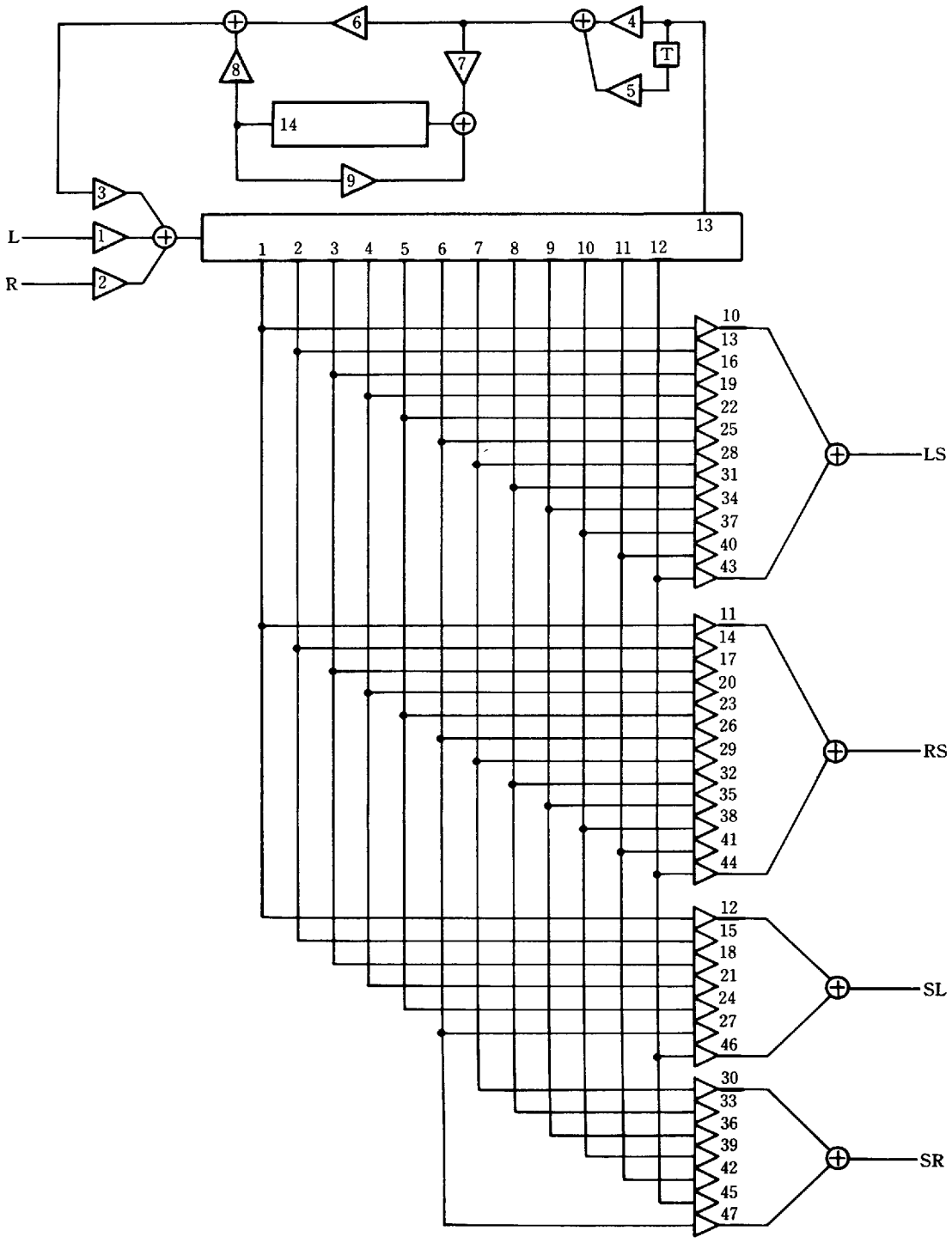
Note 2) Terminals NTR, NTRSEL and NOISE perform the reversed operations of the bits NOISE SWITCH PULSE, NOISE SWITCH SEL, and NOISE ON in the control register 2 respectively.
Terminals PHANTOM, COFF, STROFF, and SSTROFF perform the reversed operations of the corresponding bits in the control register 1 respectively.
Terminals shall be set to "H" when not in use.

■ BLOCK DIAGRAM



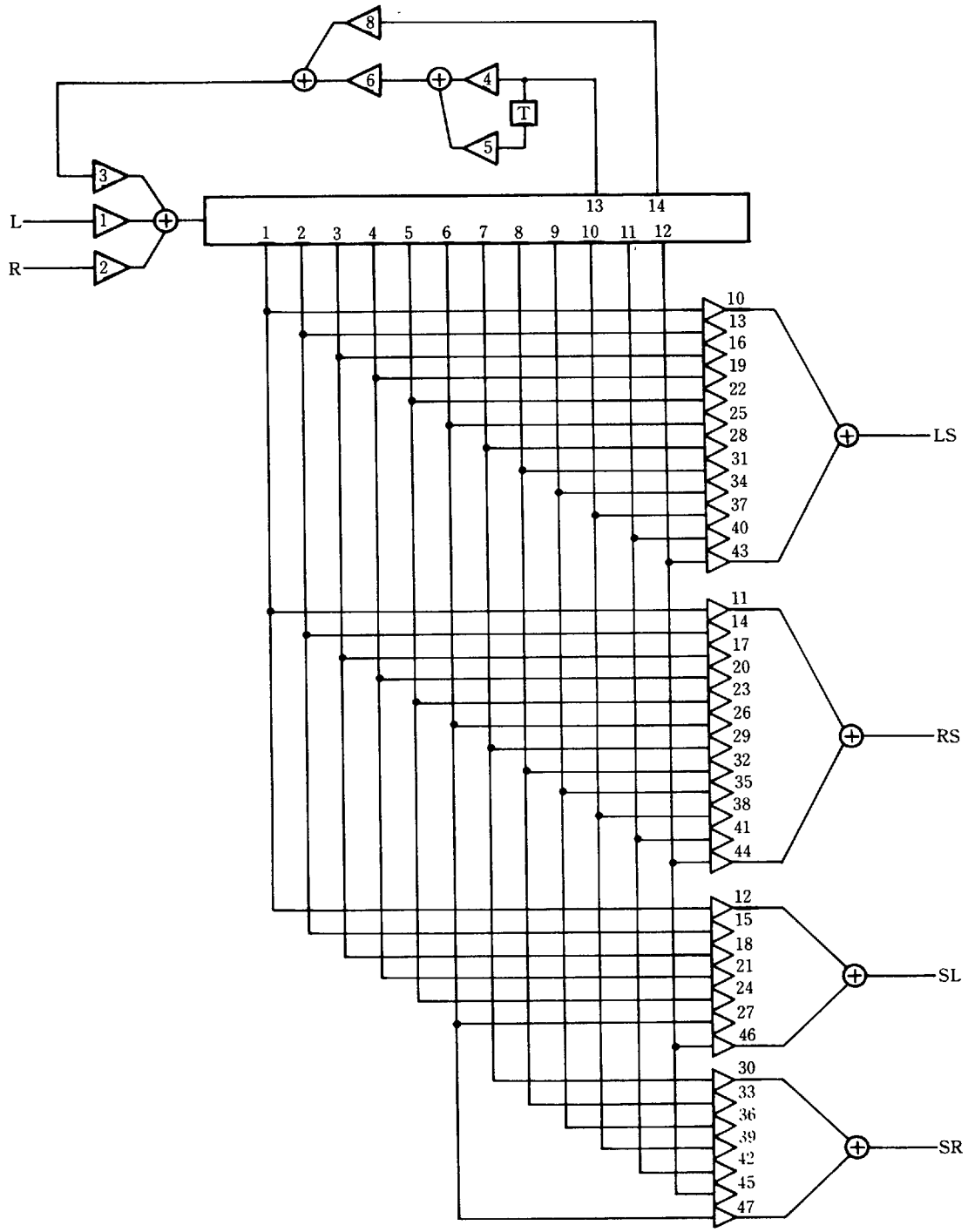
■ SOUND FIELD SIMULATION CIRCUIT BLOCK DIAGRAM

(1) When FULL DELAY is off



* T is a delay of 1/44100s.

(2) When FULL DELAY is on



* T is a delay of 1/44100s.

■ EXTERNAL DRAM INTERFACE

External memory for this LSI is assumed to be a 256 Kbit dynamic RAM for reading and writing in page mode. The LSI accesses four-bit data from D1 to D4 for four times to obtain 16 bit data. Use a DRAM with a capacity of 256 Kbit capable of accessing within 150 ns and processing in page mode.

■ Automatic Balance Control Interface

When Dolby Pro Logic mode is set, CSS and LRS/OVF terminal output signals from steering circuit. When Input signals are center steering, CSS terminal becomes "H". And, when R ch input level is higher than L ch level, LRS/OVF terminal outputs "H", and else "L".

When Sound Field Simulation mode is set, CSS terminal remains "L", and , LRS/OVF terminal outputs overflow status of internal calculation.

■ Outline of Control

(1) When microprocessor is not used

When /MCON terminal is set to "L", internal parameters are all set according to Dolby Pro Logic. Terminals NTR, NTRSEL, NOISE, PHANTOM, COFF, STROFF, and SSTROFF are used for control.

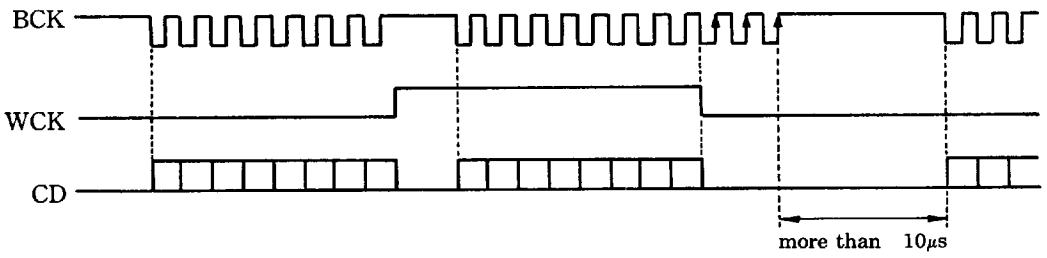
SL and SR are for surround channel output. LS and RS are used for noise generator output of L and R channels when NOISE is on.

(2) When microprocessor is used

When /MCON terminal is set to "H", internal parameters can be set with microprocessor. Terminals NTR, NTRSEL, NOISE, PHANTOM, COFF, STROFF, and SSTROFF shall be set to "H" (or no connection).

■ MICROPROCESSOR INTERFACE

(1) Timing chart



- When register address and data are sent from the microprocessor to this LSI, data is written to control registers.
- 3 clock pulses are required for BCK after the MSB of data is input and WCK falls.
- For writing to the registers, 10μs is at least required between the last BCK rise and next BCK fall. (see timing chart.)

(2) Control register map

ADDR	Name	Bit assignment							
HEX		LSB	1	2	3	4	5	6	MSB
00	MASTER CONTROL REGISTER	IC	CL MUTE	×	×	×	×	×	×
01	CONTROL REGISTER 1	DOLBY SURROUND ON	CENTER OFF	STEERING OFF	SURROUND STEERING OFF	PHANTOM ON	×	×	FULL DELAY
02	CONTROL REGISTER 2	NOISE ON	NOISE SWITCH SEL	NOISE SWITCH PULSE	×	×	×	×	×
03	STEERING GAIN	(Do not write)							
05 06 07	TESTT TEST1 TEST2								
40 : 7F	MAIN CHANNEL MANUAL MIX CONTROL								
80 : AF	COEFFICIENT REGISTER								
CD : FF	DELAY TIME REGISTER								

Note1) ×; Don't Care

Note2) Don't write to the other Address

(3) Data description

- **MASTER CONTROL REGISTER**

IC	"1"=Initial clear (initializes internal circuit)
CL	"1"=Initial data clear
MUTE	(Delay data in external RAM and internal filter RAM can be cleared to "0")

- **CONTROL REGISTER 1**

DOLBY SURROUND ON	"1"=Dolby Pro Logic mode "0"=Sound field simulation mode (set to "1" with IC)
CENTER OFF	"1"=Center channel off "0"=Center channel on (set to "0" with IC)
STEERING OFF	"1"=Steering off for all channels "0"=Steering on for all channels It must be set to '1' for Sound field simulation mode or '0' for Dolby Pro Logic mode. (set to "0" with IC)
SURROUND STEERING OFF	"1"=Steering off for surround channel "0"=Steering on for surround channel When this bit is set to "1", steering is not passed to S channel. This bit shall be set to "1" for 3 channel logic (set to "0" with IC)
PHANTOM ON	"1"=PHANTOM on "0"=PHANTOM off PHANTOM on shall be used with CENTER off (set to "0" with IC)
FULL DELAY	"1"=Unit delay time 1.45125 ms "0"=Unit delay time 0.7256 ms (set to "0" with IC)

- **CONTROL REGISTER 2**

NOISE ON	"1"=Noise output to LS and RS "0"=Noise off (set to "0" with IC)
NOISE SWITCH SEL	"1"=AUTO change (L→C→R→S in every 2 seconds) "0"=NOISE SWITCH PUISE causes switching as L→C→R→S. (set to "0" with IC)
NOISE SWITCH PULSE	When this bit is changed from "0" to "1", noise output channel switches as L→C→R→S. (set to "0" with IC)

Note) If NOISE is turned on when NOISE SWITCH SEL=0 and NOISE SWITCH PULSE=0, noise will start from S channel.

- **MAIN CHANNEL MANUAL MIX CONTROL**

Address								Data								Channel
MSB	6	5	4	3	2	1	LSB	MSB	6	5	4	3	2	1	LSB	
0	1	D2	D1	D0	0	0	0	D10	D9	D8	D7	D6	D5	D4	D3	L input→L output
0	1	D2	D1	D0	0	0	1	D10	D9	D8	D7	D6	D5	D4	D3	R input→L output
0	1	D2	D1	D0	0	1	0	D10	D9	D8	D7	D6	D5	D4	D3	L input→R output
0	1	D2	D1	D0	0	1	1	D10	D9	D8	D7	D6	D5	D4	D3	R input→R output
0	1	D2	D1	D0	1	0	0	D10	D9	D8	D7	D6	D5	D4	D3	L input→C output
0	1	D2	D1	D0	1	0	1	D10	D9	D8	D7	D6	D5	D4	D3	R input→C output

Note 1) Data is in sign-magnitude form. D10 represents sign and D9 to D0 represents magnitude (0 to 1023).
Note 2) Two multiplying DACs connected to one output (for example, L input→L output and R input→L output) cannot have negative values at the same time.
Note 3) This register is effective only when DOLBY is off.

• **COEFFICIENT REGISTER**

Address								Coefficient No.	Data							
MSB	6	5	4	3	2	1	LSB		MSB	6	5	4	3	2	1	LSB
1	0	0	0	0	0	0	1	1	Max. 127 to Min. −128 2's complement form							
			⋮					⋮								
1	0	1	0	1	1	1	1	47								

Note 1) Above coefficient numbers correspond to those shown in SOUND FIELD SIMULATION CIRCUIT BLOCK DIAGRAM.

Note 2) This register is effective only when DOLBY SURROUND is off.

• **DELAY TIME REGISTER**

Address								Tap No.	Data							
MSB	6	5	4	3	2	1	LSB		MSB	6	5	4	3	2	1	LSB
1	1	×	×	0	0	0	1	1	1 ~ 255							
			⋮					⋮								
1	1	×	×	1	1	1	0	14								

Note 1) Tap numbers correspond to those in SOUND FIELD SIMULATION CIRCUIT BLOCK DIAGRAM.
Available setting:
When FULL DELAY is off, 185 ms max. with increment of 0.7256 ms;
When FULL DELAY is on, 370 ms max. with increment of 1.45125 ms.
Data 0 means no delay for Tap No. 1, and max, delay for Tap 2 to 14. The data 0 should not be used, normaly. When delay is not required, use MANUAL MIX CONTROL to let analog signals go through.
To be precise, to delay data of LS, RS, SL and SR, delay of two samples (about 44 μs) will be added for A/D and D/A conversion from analog through signal.
Difference by 1 sample (about 22 μs) may be caused due to timing adjustment for reading/writing to external DRAM.

Note 2) When DOLBY SORROUND is on, data in the register of address $C2 only is effective as surround channel delay time.
When /MCON="L", data $1C (20.3 ms) is forcibly set to the register $C2.
When /MCON="H" and DOLBY SURROUND is on, ensure to write needed delay time to the register $C2.

Note 3) When FULL DELAY of the CONTROL REGISTER 1 is set to "1", at least one of the taps 1 to 14 shall be set as follows in order to refresh the external DRAM:
Delay data

MSB	6	5	4	3	2	1	LSB
×	×	×	×	×	×	1	0

Usually, the following setting at tap 14 is preferable for easy use.

Address								Data							
MSB	6	5	4	3	2	1	LSB	MSB	6	5	4	3	2	1	LSB
1	1	×	×	1	1	1	0	×	×	×	×	×	×	1	0

■ ELECTRICAL CHARACTERISTICS

• ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	VDD	−0.3	+7.0	V
Input voltage	VI	−0.3	VDD +0.5	V
Input current	II		10	mA
Operating temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

• RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VDD	4.75	5.0	5.25	V
Operating temperature	Top	0	25	70	°C

• ELECTRICAL CHARACTERISTICS (CONDITIONS : Ta=25°C, VDD=5.0±0.25V)

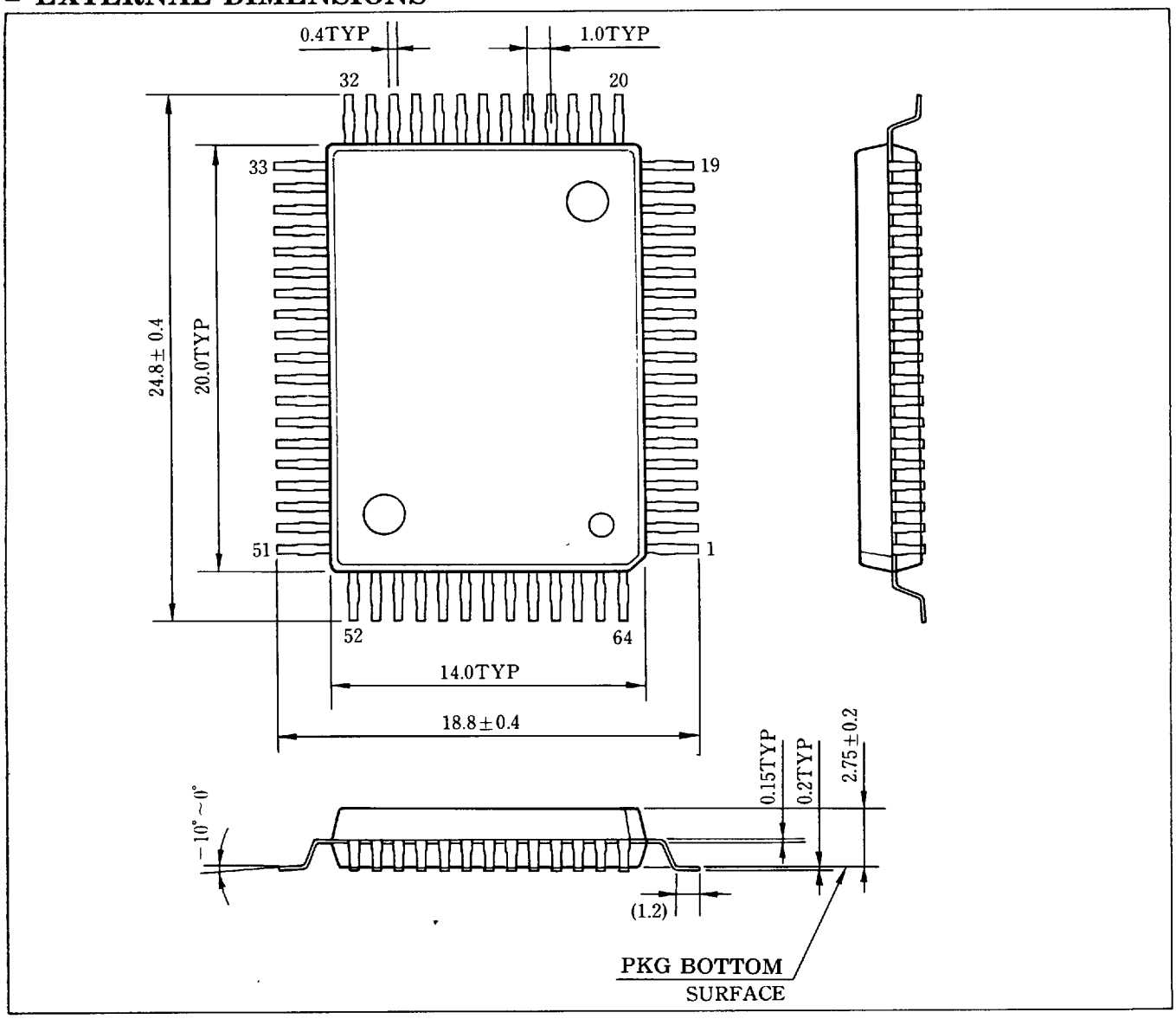
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption	W	VDD=5.0V		200	300	mW
Input Voltage H level	VIH					V
TTL level			2.7		VDD	
CMOS level			3.5		VDD	
Input Voltage L level	VIL					V
TTL level			0		0.4	
COMS level			0		1.0	
Input leakage current	IIL				10	μA
Output voltage L level	VOL	IOL=−2mA	0		0.4	V
Output voltage H level	VOH	IOH=200μA	3.0		VDD	V
XI frequency	XIN		8.0	8.46	9.0	MHz
XI clock duty			40	50	60	%
BCI frequency					2.0	MHz

• ANALOG CHARACTERISTICS (CONDITIONS : VDD=+5V, Ta=25°C, XIN=8.4672MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Multipying DAC impedance	RM		8.0	9.6	11.5	KΩ
Output Distortion						
Main channel	Dmmax	Output		0.03	0.1	%
Surround channel	Dsmax	300mVr.m.s.		0.25	0.7	
Output S/N						dB
Main channel	S/N m		85			
Surround channel		CCIR-ARM				
Dolby prologic mode	S/N SD		70	77		
Sound field simulation mode *1	S/N SS	(0dB=300mVr.m.s.)	65	70		
Frequency response						dB
Main channel	Frm	50~20K Hz			±0.2	
Surround channel	Frs	50~6K Hz			±0.5	
Modified B-type N.R. decording accuracy	N.R.a	0dB=300mVr.m.s.			±1.0	dB
Noise sequencer output level	Nout			85		mV r.m.s.
Dolby Pro Logic steering Separation	STsep			30		dB
max input level	Smax	0dB=300mVr.m.s.			+15	dB

Note) Main channel indicates L, R, and C channel.
Surround channel indicates LS, SL, RS, and SR channel.
* Unity gain

■ EXTERNAL DIMENSIONS



The specifications of this product are subject to improvement changes without prior notice.

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