YAMAHA LSI

YMF704C OPL™

OPL4-ML

FM+Wave Table Synthesizer LSI

Preliminary

■ OVERVIEW

YMF704C(OPL4-ML) is a Wave table synthesizer LSI that integrates OPL3, General MIDI processor and Wave table ROM into one chip, and complies with GM system level 1.

YMF704C makes a low cost system with high quality tone when it is used in the multimedia personal computers and sound boards.

The LSI is able to operate normally at power voltage of 3.3V. These features make this LSI suitable for notebook type personal computers that require low power consumption.

■ FEATURES

- Complies with GM system Level 1.
- MIDI signal can be transmitted either through serial input or parallel input.
- Contains an interface that is compatible with MPU-401 UART mode.
- FM synthesis is register compatible with OPL3.
- Wabe table synthesis is able to generate up to 24 voices simultaneously.
- Contains 8-Mbit Wave table ROM.
- All registers are readable.
- Master clock frequency is 33.8688MHz.
- Power supply voltage is 5V or 3.3V.
- Silicon gate CMOS process.
- 100-pin QFP(YMF704C-F) or 100-pin SQFP(YMF704C-S).

OPL™ is the trademark of YAMAHA Corporation which represents a full register compatibility with YAMAHA YM3812(OPL2).

The contents of this catalog are target specifications and are subject to change without prior notice. When using this device, please recheck the specifications.

YAMAHA CORPORATION

December 18, 1996

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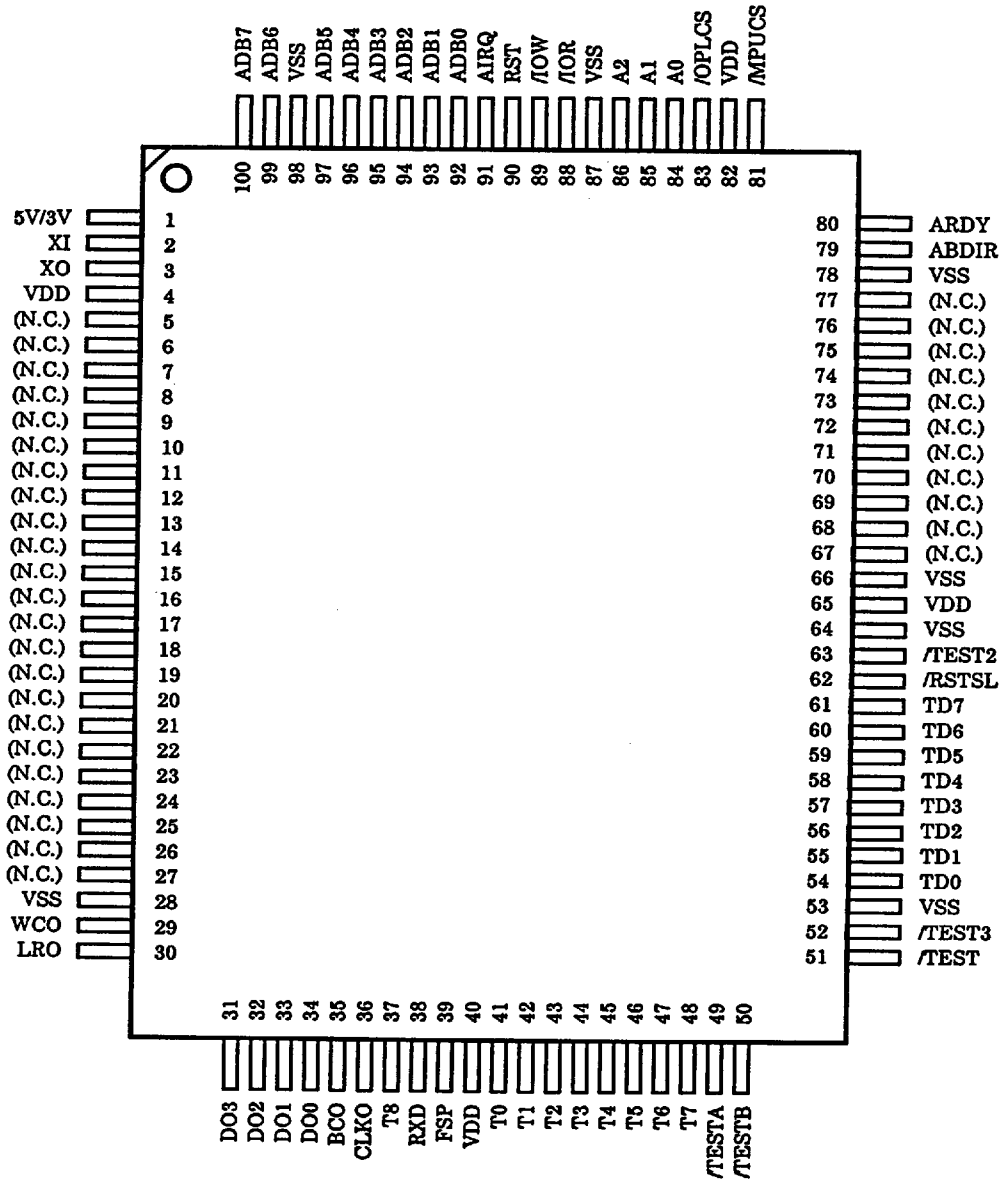
■ PIN LAYOUT

YMF704C-F



100 Pin QFP Top View

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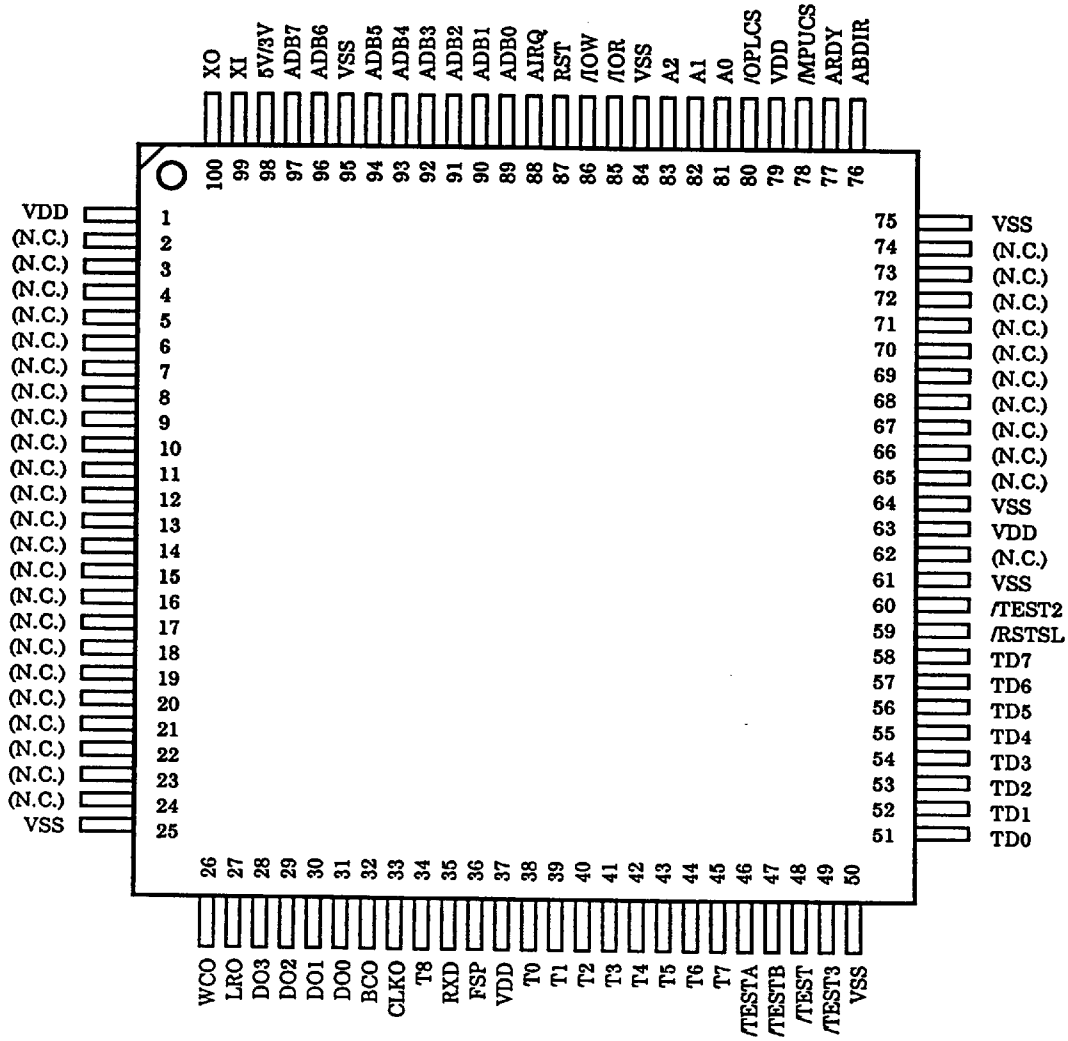
YMF704C-S



100 Pin SQFP Top View

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■ PIN DESCRIPTION

No.		Name	I/O	Function
QFP	SQFP			
1	98	5V/3V	I	Power supply voltage selection ('H' : 5V, 'L' : 3.3V)
2	99	XI	I	Crystal oscillator or master clock input (33.8688MHz)
3	100	XO	O	Crystal oscillator connection pin
4	1	VDD	-	+5V or 3.3V Power supply
28	25	VSS	-	Ground
29	26	WCO	O	Audio interface Word clock output
30	27	LRO	O	Audio interface L/R clock output
31	28	DO3	O	Audio interface effect send output
32	29	DO2	O	Audio interface MIX(FM+PCM)
33	30	DO1	O	Audio interface PCM-EXT output
34	31	DO0	O	Audio interface FM-EXT output
35	32	BCO	O	Audio interface Bit clock output
36	33	CLKO	O	Clock output (16.9344MHz)
37	34	T8	O	LSI test pin (To be open at normal operation)
38	35	RXD	I	MIDI serial data input
39	36	FSP	I	MIDI serial/parallel switching ('H': Parallel, 'L': Serial)
40	37	VDD	-	+5V or 3.3V Power supply
41	38	T0	O	LSI test pin (To be open at normal operation)
42	39	T1	O	LSI test pin (To be open at normal operation)
43	40	T2	O	LSI test pin (To be open at normal operation)
44	41	T3	O	LSI test pin (To be open at normal operation)
45	42	T4	O	LSI test pin (To be open at normal operation)
46	43	T5	O	LSI test pin (To be open at normal operation)
47	44	T6	O	LSI test pin (To be open at normal operation)
48	45	T7	O	LSI test pin (To be open at normal operation)
49	46	/TESTA	I+	LSI test pin (To be open at normal operation)
50	47	/TESTB	I+	LSI test pin (To be open at normal operation)
51	48	/TEST	I+	LSI test pin (To be open at normal operation)
52	49	/TEST3	I+	LSI test pin (To be open at normal operation)
53	50	VSS	-	Ground
54	51	TD0	O	LSI test pin (To be open at normal operation)
55	52	TD1	O	LSI test pin (To be open at normal operation)
56	53	TD2	O	LSI test pin (To be open at normal operation)
57	54	TD3	O	LSI test pin (To be open at normal operation)
58	55	TD4	O	LSI test pin (To be open at normal operation)

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No.		Name	I/O	Function
QFP	SQFP			
59	56	TD5	O	LSI test pin (To be open at normal operation)
60	57	TD6	O	LSI test pin (To be open at normal operation)
61	58	TD7	O	LSI test pin (To be open at normal operation)
62	59	/RSTSL	I+	RST signal select pin ('H' : RST is 'H' active)
63	60	/TEST2	I+	LSI test pin (To be open at normal operation)
64	61	VSS	-	Ground
65	63	VDD	-	+5V or 3.3V Power supply
66	64	VSS	-	Ground
78	75	VSS	-	Ground
79	76	ABDIR	O	ADB direction switching ('L' : OPL4-ML→ATBUS)
80	77	ARDY	OD	CPU interface I/O channel READY ('H' : READY)
81	78	/MPUCS	I	CPU interface MPU chip select
82	79	VDD	-	+5V or 3.3V Power supply
83	80	/OPLCS	I	CPU interface (OPL + GMP) chip select
84	81	A0	I	CPU interface address 0
85	82	A1	I	CPU interface address 1
86	83	A2	I	CPU interface address 2
87	84	VSS	-	Ground
88	85	/IOR	I	CPU interface read enable
89	86	/IOW	I	CPU interface write enable
90	87	RST	I	Initial clear input *1
91	88	AIRQ	O	Interrupt signal ('H' : interrupt)
92	89	ADB0	I/O	CPU interface data
93	90	ADB1	I/O	CPU interface data
94	91	ADB2	I/O	CPU interface data
95	92	ADB3	I/O	CPU interface data
96	93	ADB4	I/O	CPU interface data
97	94	ADB5	I/O	CPU interface data
98	95	VSS	-	Ground
99	96	ADB6	I/O	CPU interface data
100	97	ADB7	I/O	CPU interface data

Note : Other pins than the above are (N.C.) pins that must be open at normal operation.

I+ : Input pin with built-in pull-up resistor. OD : Open drain output pin.

*1 : When /RSTSL pin is 'H' level or no connection, RST is 'H' active.
When /RSTSL pin is 'L' level, RST is 'L' active.

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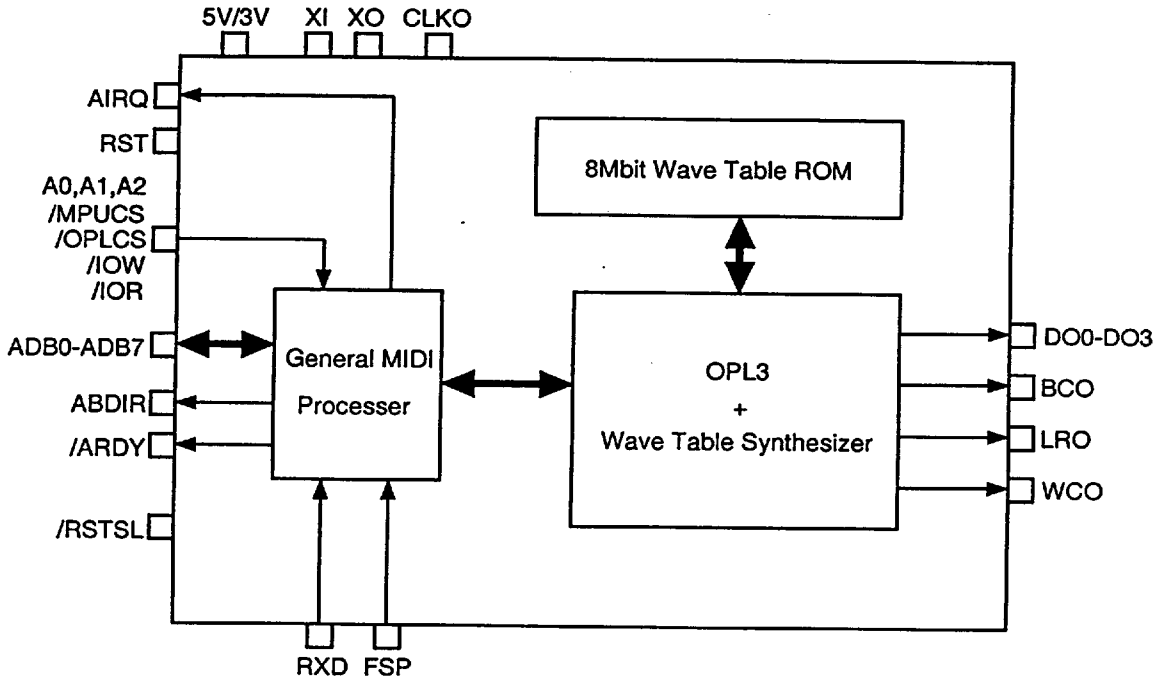
■ BLOCK DIAGRAM



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■ FUNCTIONS

1. CPU Interface

YMF704C has an 8-bit parallel interface for register access.
A0 to A2 pins are for inputting address signals.
ADB0 to ADB7 pins are I/O data bus.
Control of the data bus is made by signals inputted to /MPUCS, /OPLCS, /IOW and /IOR pins.
Mode of the data bus is determined according to combination of states of these signals as shown below.

/MPUCS	/OPLCS	/IOW	/IOR	A2	A1	A0	MODE
L	H	L	H	X	L	L	MPU401 data write
L	H	L	H	X	L	H	MPU401 command write
L	H	H	L	X	L	L	MPU401 acknowledge (FEH)
L	H	H	L	X	L	H	MPU401 status read
H	L	L	H	H	H	L	GMP command write
H	L	L	H	H	H	H	GMP control write
H	L	H	L	H	H	L	GMP response read
H	L	H	L	H	H	H	GMP status read
H	L	H	L	L	L	L	OPL4 FM status read
H	L	L	H	L	H/L	L	OPL4 FM address write
H	L	L	H	L	X	H	OPL4 FM data write
H	L	H	L	L	X	H	OPL4 FM data read
H	L	H	L	H	L	L	OPL4 PCM status read
H	L	L	H	H	L	L	OPL4 PCM address write
H	L	L	H	H	L	H	OPL4 PCM data write
H	L	H	L	H	L	H	OPL4 PCM data read
H	L	H	H	X	X	X	Non-operating state or UART mode
H	H	X	X	X	X	X	Non-operating state or UART mode

X: Don't care

Wait needed is 0 ns at address write or data write in PCM section after address write in FM section.
Wait needed is 0 ns at address write or data write in FM section after address write in PCM section.

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■ FUNCTIONS OF REGISTERS

MPU Data

	D7	D6	D5	D4	D3	D2	D1	D0
Write	MPU Data							
Read	MPU Data (FEh)							

MPU Data : Write MIDI data.
Returns acknowledge(FEh) of MPU at read.

MPU Command / MPU Status

	D7	D6	D5	D4	D3	D2	D1	D0
Write	MPU Command							
Read	DSR	DRR						

MPU Command : Data written in this register is ignored. DSR bit is set to '0'.
DSR : '1' at MPU data read, and '0' at MPU command write.
DRR : '1' at MPU write.

GMP Command / GMP Response

	D7	D6	D5	D4	D3	D2	D1	D0
Write	GMP Command							
Read	GMP Response							

GMP Command : Write GMP command.
GMP Response : Output response to GMP command.

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GMP Control / GMP Status

	D7	D6	D5	D4	D3	D2	D1	D0
Write						GMPR	'0'	'1'
Read				BSEL		RESP	GBUSY	GDRQ

GMPR : MIDI data interpreter is initialized when this bit is '0'. This bit becomes '1' when the interpreter has been initialized.

BSEL : '1' shows that OPL4 is connected with MIDI data interpreter. '0' shows that OPL4 is connected with ISA-bus.

RESP : Shows that there is a response to GMP command.

GBUSY : This is a BUSY flag bit. '1' shows busy state and '0' shows that data can be written into GMP command register.

GDRQ : This is a READY flag bit. '1' shows ready state and '0' shows not to read data from GMP response register.

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PCM Register map

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
00H~01H	LSI TEST							
02H	Device ID			Wave table header			Memory type	Memory access
				2	1	0		
03H			Memory address register					
			MA21	MA20	MA19	MA18	MA17	MA16
04H	Memory address register							
	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8
05H	Memory address register							
	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
06H	Memory data register							
08H~1FH	Wave table number							
	7	6	5	4	3	2	1	0
20H~37H	F-NUM							wavetable number 8
	f6	f5	f4	f3	f2	f1	f0	
38H~4FH	Octave				Pseudo-reverb	F-NUM		
	3	2	1	0		f9	f8	f7
50H~67H	Total level							Level direct
	6	5	4	3	2	1	0	
68H~7FH	KEY ON	DAMP	LFO RST	CH	Panpot			
					3	2	1	0
80H~97H	Chorus send level		LFO			VIB		
			S2	S1	S0	V2	V1	V0
98H~AFH	AR				D1R			
	3	2	1	0	3	2	1	0
B0H~C7H	DL				D2R			
	3	2	1	0	3	2	1	0
C8H~DFH	Rate correction				RR			
	3	2	1	0	3	2	1	0
E0H~F7H	Reverb send level					AM		
						2	1	0
F8H			MIX control (FM-R)			MIX control (FM-L)		
			2	1	0	2	1	0
F9H			MIX control (PCM-R)			MIX control (PCM-L)		
			2	1	0	2	1	0
FAH								ATC
FBH								

Note1 : Initialization sets the value of FM MIX at F8H to default -15dB(2DH) and clears all the other registers.

Note2 : Be sure to set 'LSI TEST' bits and the shaded bits to '0'.

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FM Register map

ADDRESS	REGISTER ARRAY 0 (A1='L')								REGISTER ARRAY 1 (A1='H')							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
00H~ 01H	LSI TEST								LSI TEST							
02H	TIMER 1															
03H	TIMER 2															
04H	RST	MT1	MT2				ST2	ST1					CONNECTION SEL			
05H														NEW3	NEW2	NEW
08H		NTS														
20H~ 35H	AM	VIB	EGT	KSR	MULT				AM	VIB	EGT	KSR	MULT			
					3	2	1	0					3	2	1	0
40H~ 55H	KSL		TL						KSR		TL					
	1	0	T5	T4	T3	T2	T1	T0	1	0	T5	T4	T3	T2	T1	T0
60H~ 75H	AR				DR				AR				DR			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
80H~ 95H	SL				RR				SL				RR			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
A0H~ A8H	F-NUMBER(L)								F-NUMBER(L)							
	F7	F6	F5	F4	F3	F2	F1	F0	F7	F6	F5	F4	F3	F2	F1	F0
B0H~ B8H			KON	BLOCK			F-NUM(H)				KON	BLOCK			F-NUM(H)	
				B2	B1	B0	F9	F8				B2	B1	B0	F9	F8
BDH	DAM	DVB	RHY	BD	SD	TOM	TC	HH								
C0H~ C8H	CHD	CHC	CHB	CHA	FB			CNT	CHD	CHC	CHB	CHA	FB			CNT
					2	1	0						2	1	0	
E0H~ F5H						WS								WS		
						W2	W1	W0						W2	W1	W0

Note : 1. All registers are readable.

2. Be sure to set 'LSI TEST' bits and those shaded bits to '0'.

3. Initialization clears all bits except CHA and CHB bits of $C0H to $C8H.

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■ DAC INTERFACE

Data outputted from YMF704C is 16 bit 2's complement digital data.
The data is outputted with MSB first, and the sampling frequency is 44.1kHz.
Data outputted from each pin is as follows.

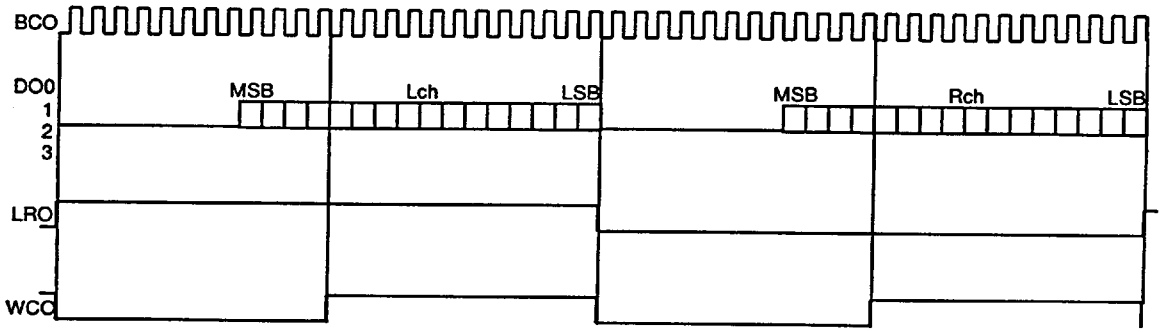
DO0.....Outputs data in FM synthesis.(data at channels that have been set by CHC and CHD of FM registers $C0H to C8H.)

DO1.....Outputs data in PCM synthesis.(data at channels that have been set to CH='1' of PCM registers $68H to 7FH.)

DO2.....Outputs mixture of data in the FM synthesis and PCM synthesis.(data at channels that have been set by CHA and CHB of FM registers $C0H to C8H and data at channels that have been set to CH='0' of PCM registers $68H to 7FH.)

DO3.....Output data in PCM synthesis which effect send level has been adjusted.

Output Timing



Frequency of BCO is 48 fs (sampling frequency) and duty cycle of this signal is 50 % (fs = 44.1kHz).
Fs of DO0 to DO3 is 44.1kHz.
Frequency of LRO is 1 fs and duty cycle of this signal is 50 %.
Frequency of WCO is 2 fs and duty cycle of this signal is 50 %.

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■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum rating

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3～7.0	V
Input voltage	V_{IN}	-0.3～V_{DD}+0.5	V
Operating temperature	T_{OP}	0～70	℃
Storage temperature	T_{STG}	-50～125	℃

2. Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	5V/3V='H'	4.75	5.00	5.25	V
		5V/3V='L'	3.00	3.30	3.60	V
Operating temperature	T_{OP}		0	25	70	℃

3. DC Characteristics (under recommended operating conditions)

Item	Symbol	Condition	Min.	Max.	Unit
Power consumption	P_D	V_{DD}=5.25V at operation		300	mW
		V_{DD}=3.60V at operation		150	mW
Input voltage 'H' level (1)	V_{IH1}	Input pins except XI, 5V/3V	2.0		V
Input voltage 'L' level (1)	V_{IL1}	and ADB0 to ADB7		0.8	V
Input voltage 'H' level (2)	V_{IH2}	XI, 5V/3V	0.7V_{DD}		V
Input voltage 'L' level (2)	V_{IL2}			0.2V_{DD}	V
Input leakage current	I_{LI}	$0V \leqq V_{IN} \leqq V_{DD}$	-10	10	μA
Input capacitance	C_I			10	pF
Output voltage 'H' level (1)	V_{OH1}	I_{OH}=-80 μA (5V/3V='L')	2.4		V
Output voltage 'L' level (1)	V_{OL1}	I_{OL}=2mA *1		0.4	V
Output voltage 'H' level (2)	V_{OH2}	I_{OH}=-80 μA (5V/3V='H')	V_{DD}-1.0		V
Output voltage 'L' level (2)	V_{OL2}	I_{OL}=2mA *1		V_{SS}+0.4	V
Output voltage 'L' level (3)	V_{OL3}	I_{OL}=4mA (5V/3V='L') *2		0.4	V
Output voltage 'L' level (4)	V_{OL4}	I_{OL}=12mA (5V/3V='H') *2		0.4	V
Output capacitance	C_O			10	pF
Pull up resistance	R_U	Input pins with built-in pull up resistor	50	400	kΩ

Note : *1 : Applicable to output pins except XO and ARDY.
*2 : Applicable to ARDY pin.

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4. AC Characteristics (under recommended operating conditions)

(1) CPU interface

Item	Symbol	Fig.	Min.	Typ.	Max.	Unit
Master clock frequency	fM1	Fig.1		33.8688		MHz
Duty cycle	D		40		60	%
Output clock frequency	fM2	Fig.2		16.9344		MHz
Duty cycle	D			50		%
Reset pulse width	tICW	Fig.3	100			ms
Address setup time	tAS	Fig.4,5	30			ns
Address hold time	tAH		10			ns
Chip select setup time	tCS	Fig.4,5	5			ns
Chip select hold time	tCH		10			ns
Write pulse width	tWW	Fig.4	50			ns
Data setup time	tWDS		10			ns
Write data hold time	tWDH		10			ns
Read pulse width	tRW	Fig.5	80			ns
Read data access time	tACC				60	ns
Read data hold time	tRDH		10			ns

Note: Output pin load capacitance CL=50(pF).

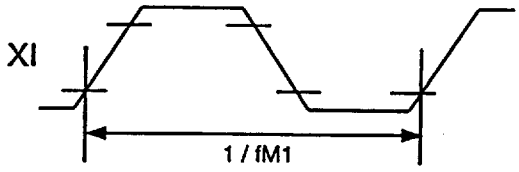

Fig.1 Input clock timing

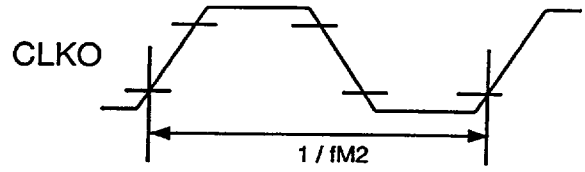

Fig.2 Output clock timing

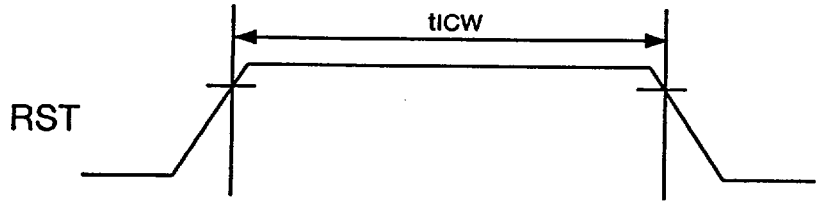

Fig.3 Reset pulse timing

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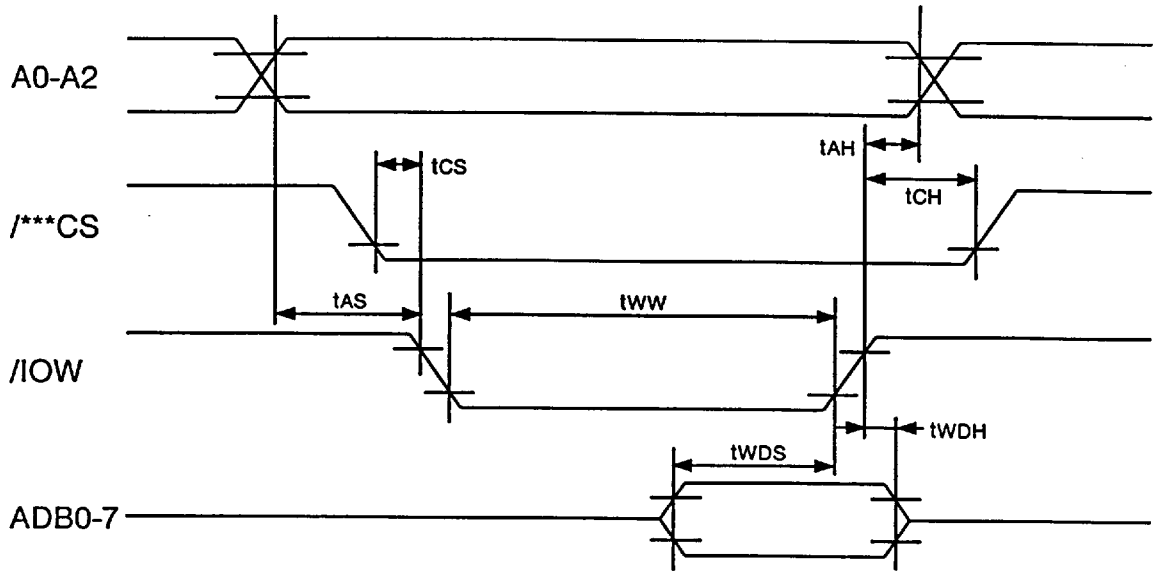

Fig.4 Data write timing

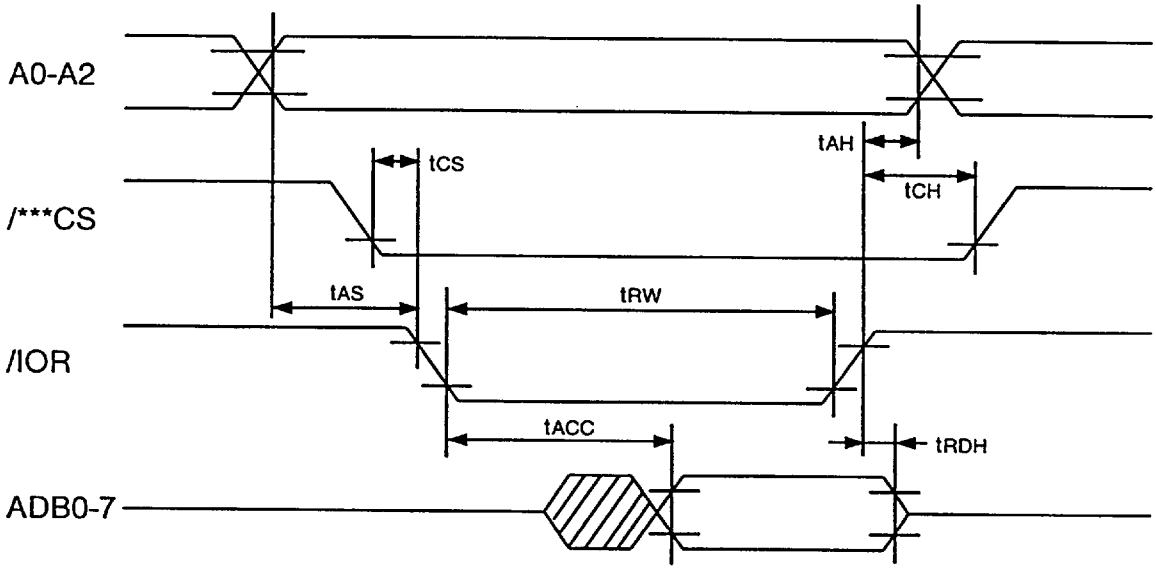

Fig.5 Data read timing

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(2) Audio interface

Item	Symbol	Fig.	Typ.	Unit	Remarks
Bit clock frequency	fBC	Fig.6	2.11680	MHz	Bit clock frequency : 48fs
Data out setup time	tDOS	Fig.6	118	ns	
Data out hold time	tDOH	Fig.6	118	ns	
LR clock setup time	tLRS	Fig.6	118	ns	LR clock frequency : fs
LR clock hold time	tLRH	Fig.6	118	ns	
Word clock setup time	tWCS	Fig.6	118	ns	Word clock frequency : 2fs
Word clock hold time	tWCH	Fig.6	118	ns	

Note: fs=44.1kHz

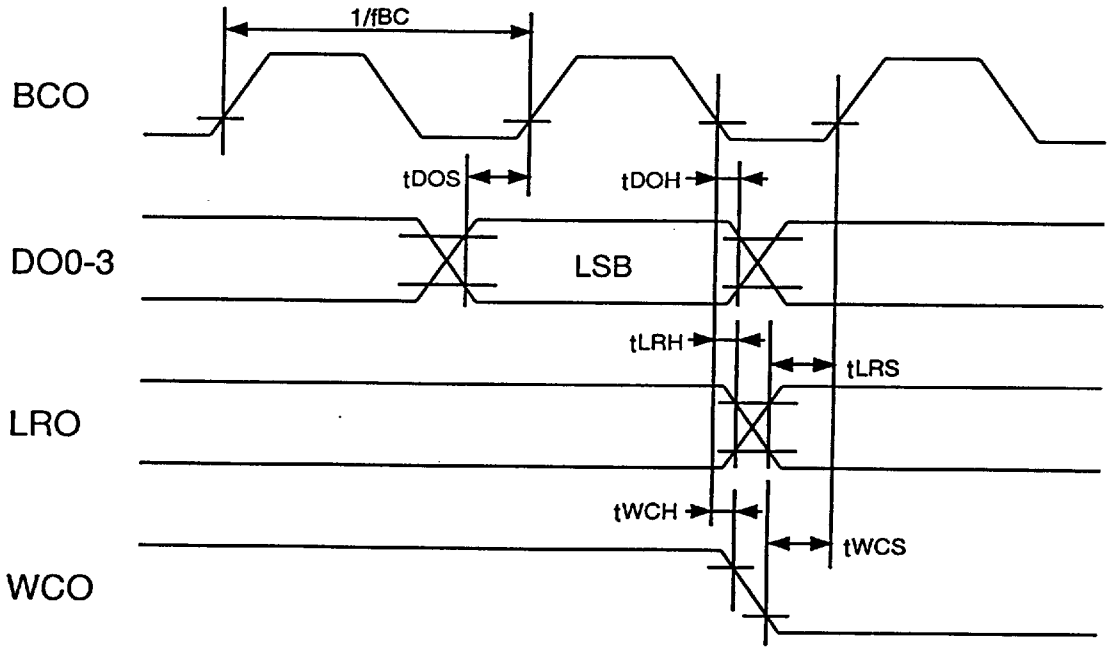

Fig.6 Audio interface timing

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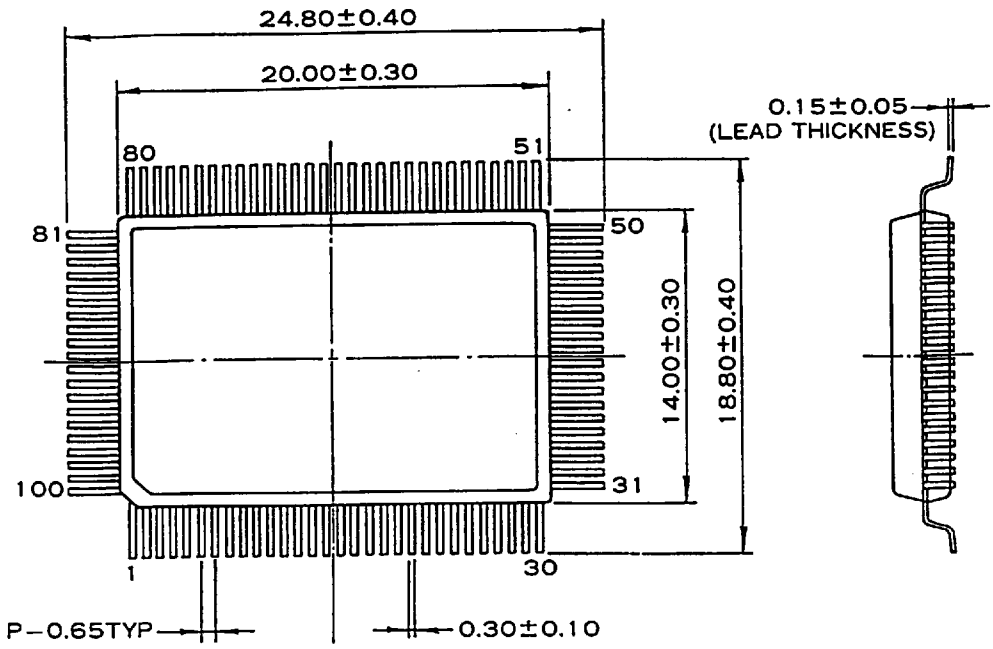
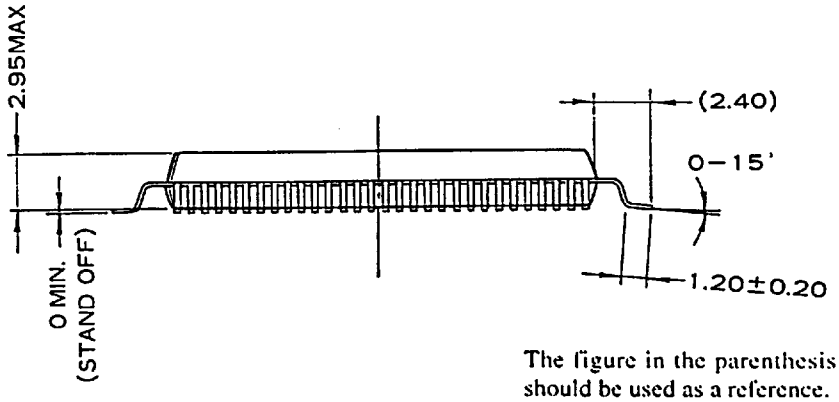
■ EXTERNAL DIMENSIONS

YMF704C-F





The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note : The LSIs for surface mount need especial consideration on storage and soldering conditions.
For detailed information, please contact your nearest agent of yamaha.

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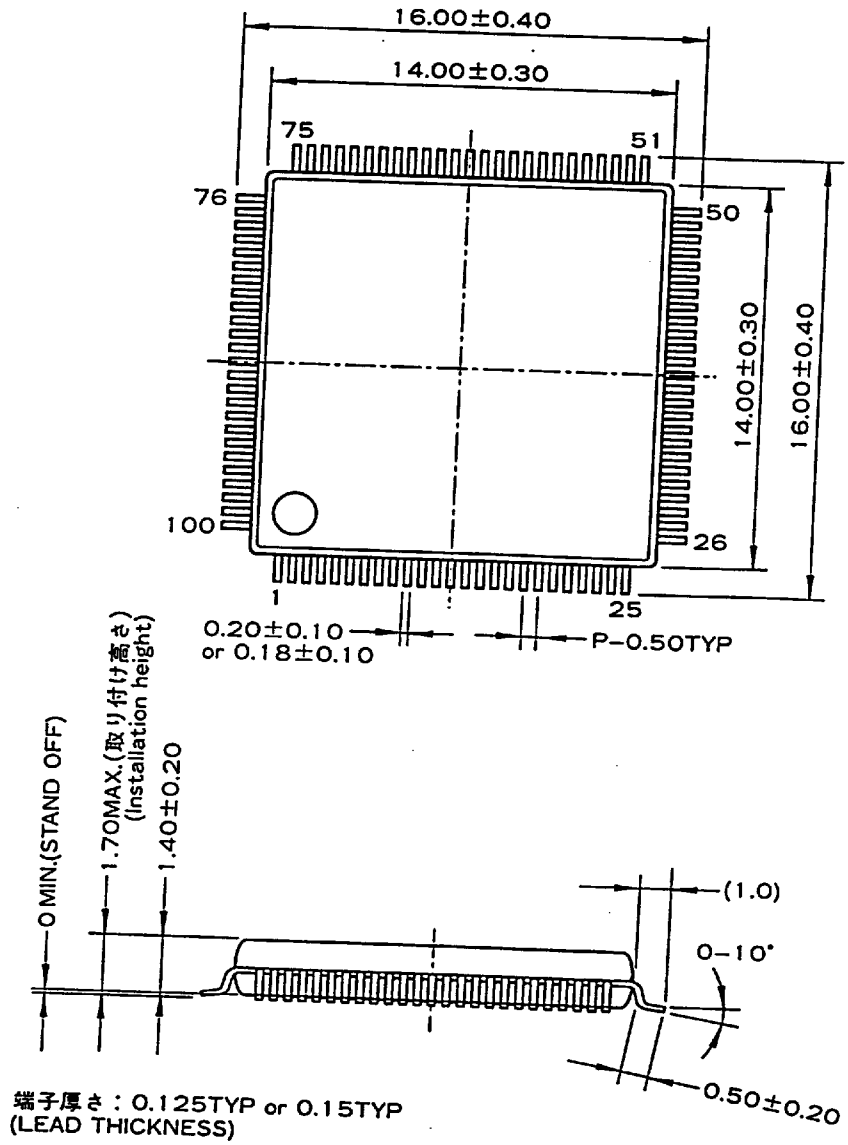

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note : The LSIs for surface mount need especial consideration on storage and soldering conditions.
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