Preliminary
1996. 6. 17

YSS243

AC3F

AC-3 5.1ch Full decoder

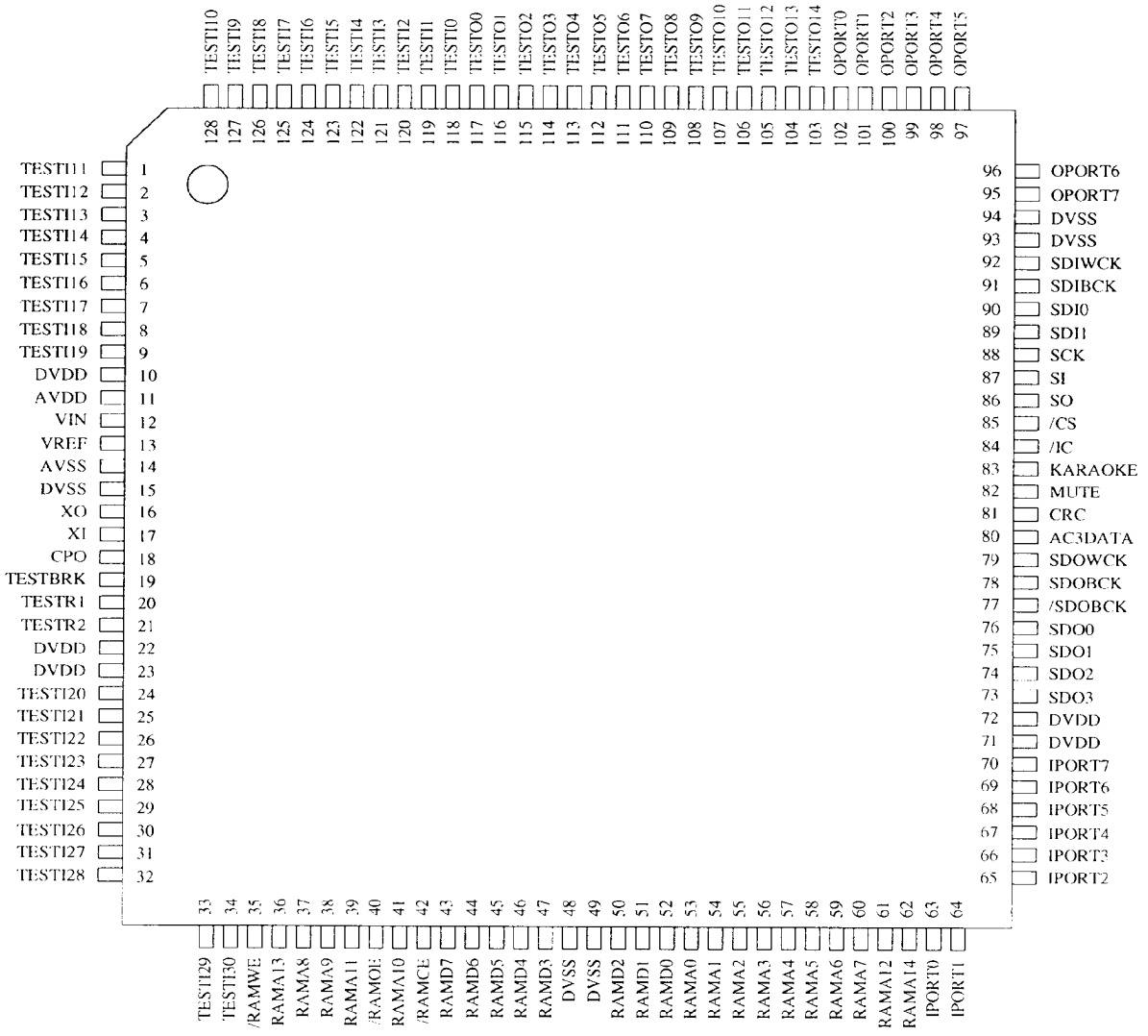
■OUTLINE

The YSS243(AC3F) is a Dolby AC-3 5.1ch full decoder which decodes AC-3 data stream in IEC958 interface and outputs PCM data.
It uses 24bit DSP for decoding and high accurate PCM data can be obtained.
The low operating clock (20MHz) contributes low power consumption. Heat problem free AC-3 decoding system can be made.

■FEATURES

- Supports every input/output channel mode ; 1 to 5.1ch. Supports every downmixing mode.
- Supports every bit rate ; 32kbps to 640kbps.
- Supports AC-3 karaoke mode.
- Built in input buffer. One external 256Kbit SRAM for output buffer.
- Built in PLL clock multiplier circuit. Capable of choosing input clock frequency from 2.5M to 40MHz.
- Supports 3 input/output data interface formats.
- Decodes multi-language data. (possible to decode by data-stream-number)
- Supports Dolby-specified shaped noise as well as white noise.
- Provides 2 mixing output channels, in addition to 6 output channels (L, C, R, LS, RS, LFE).
- Supports time delay control of center and surround.
- Supports user original mode as well as Dolby-recommended 4 compression modes.
- Supports dynamic range compression.
- Capable of reading AC-3 bitstream information through microprocessor interface.
- AC-3 decode latency is 3 audio block (768 samples) constant.
- 5V single power supply. Si-gate CMOS process.
- 128 pin QFP (YSS243-F).

■PIN CONFIGURATION



< 128 pin QFP top view >

■PIN FUNCTION

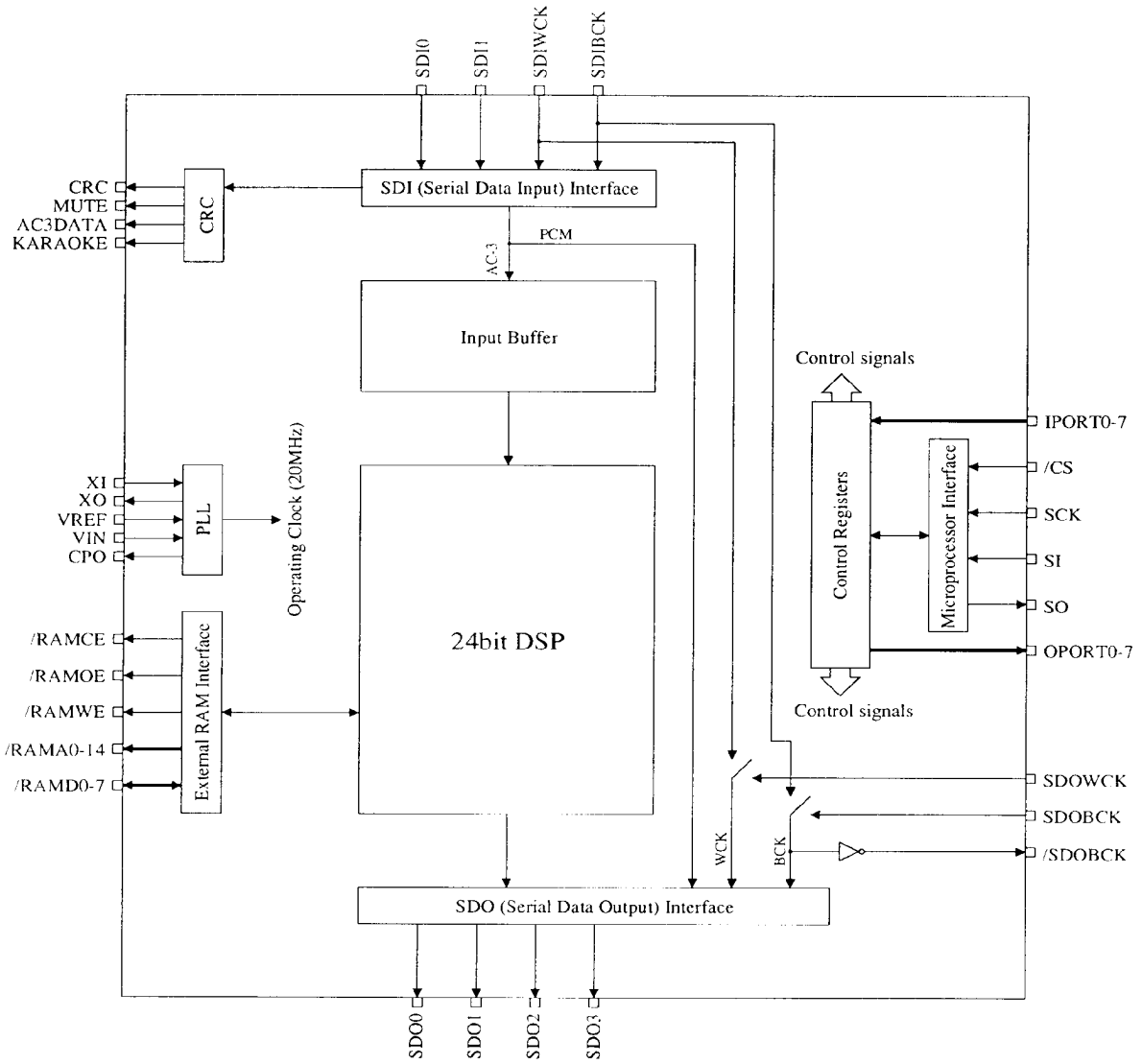
No.	NAME	I/O	FUNCTION
1	TESTI11	I+	LSI test terminal (To be open in use)
2	TESTI12	I+	LSI test terminal (To be open in use)
3	TESTI13	I+	LSI test terminal (To be open in use)
4	TESTI14	I+	LSI test terminal (To be open in use)
5	TESTI15	I+	LSI test terminal (To be open in use)
6	TESTI16	I+	LSI test terminal (To be open in use)
7	TESTI17	I+	LSI test terminal (To be open in use)
8	TESTI18	I+	LSI test terminal (To be open in use)
9	TESTI19	I+	LSI test terminal (To be open in use)
10	DVDD	-	+5V power supply (for digital circuit)
11	AVDD	-	+5V power supply (for PLL circuit)
12	VIN	AI	Input terminal for PLL circuit Connect with CPO terminal through the external analog filter.
13	VREF	AI	Input terminal for PLL circuit Connect with AVDD through the external analog filter.
14	AVSS	-	Ground (for PLL circuit)
15	DVSS	-	Ground (for digital circuit)
16	XO	O	Connect with crystal oscillator
17	XI	I	Connect with crystal oscillator or input external clock (2.5M ~ 40.0MHz)
18	CPO	AO	Output terminal for PLL circuit Connect with VIN terminal through the external analog filter.
19	TESTBRK	I+	LSI test terminal (To be open in use)
20	TESTR1	I+	LSI test terminal (To be open in use)
21	TESTR2	I+	LSI test terminal (To be open in use)
22	DVDD	-	+5V power supply (for digital circuit)
23	DVDD	-	+5V power supply (for digital circuit)
24	TESTI20	I+	LSI test terminal (To be open in use)
25	TESTI21	I+	LSI test terminal (To be open in use)
26	TESTI22	I+	LSI test terminal (To be open in use)
27	TESTI23	I+	LSI test terminal (To be open in use)
28	TESTI24	I+	LSI test terminal (To be open in use)
29	TESTI25	I+	LSI test terminal (To be open in use)
30	TESTI26	I+	LSI test terminal (To be open in use)
31	TESTI27	I+	LSI test terminal (To be open in use)
32	TESTI28	I+	LSI test terminal (To be open in use)
33	TESTI29	I+	LSI test terminal (To be open in use)
34	TESTI30	I+	LSI test terminal (To be open in use)
35	/RAMWE	O	External SRAM Interface /WE
36	RAMA13	O	External SRAM Interface address
37	RAMA8	O	External SRAM Interface address
38	RAMA9	O	External SRAM Interface address
39	RAMA11	O	External SRAM Interface address
40	/RAMOE	O	External SRAM Interface /OE
41	RAMA10	O	External SRAM Interface address
42	/RAMCE	O	External SRAM Interface /CE
43	RAMD7	I/O	External SRAM Interface data
44	RAMD6	I/O	External SRAM Interface data
45	RAMD5	I/O	External SRAM Interface data
46	RAMD4	I/O	External SRAM Interface data
47	RAMD3	I/O	External SRAM Interface data

No.	NAME	I/O	FUNCTION
48	DVSS	-	Ground (for digital circuit)
49	DVSS	-	Ground (for digital circuit)
50	RAMD2	I/O	External SRAM Interface data
51	RAMD1	I/O	External SRAM Interface data
52	RAMD0	I/O	External SRAM Interface data
53	RAMA0	O	External SRAM Interface address
54	RAMA1	O	External SRAM Interface address
55	RAMA2	O	External SRAM Interface address
56	RAMA3	O	External SRAM Interface address
57	RAMA4	O	External SRAM Interface address
58	RAMA5	O	External SRAM Interface address
59	RAMA6	O	External SRAM Interface address
60	RAMA7	O	External SRAM Interface address
61	RAMA12	O	External SRAM Interface address
62	RAMA14	O	External SRAM Interface address
63	IPORT0	I+	Input port for general purpose
64	IPORT1	I+	Input port for general purpose
65	IPORT2	I+	Input port for general purpose
66	IPORT3	I+	Input port for general purpose
67	IPORT4	I+	Input port for general purpose
68	IPORT5	I+	Input port for general purpose
69	IPORT6	I+	Input port for general purpose
70	IPORT7	I+	Input port for general purpose
71	DVDD	-	+5V power supply (for digital circuit)
72	DVDD	-	+5V power supply (for digital circuit)
73	SDO3	O	PCM output terminal (MIX0, MIX1)
74	SDO2	O	PCM output terminal (C, LFE)
75	SDO1	O	PCM output terminal (LS, RS)
76	SDO0	O	PCM output terminal (L, R)
77	/SDOBCK	O	Output terminal of inverted SDOBCK
78	SDOBCK	I+	Bit clock for SDO output
79	SDOWCK	I+	Word clock for SDO output
80	AC3DATA	O	Detection of AC-3 bitstream data
81	CRC	O	Detection of CRC error (when AC-3 bitstream data is decoded)
82	MUTE	O	Detection of output data mute
83	KARAOKE	O	Detection of AC-3 karaoke data
84	/IC	Is	Initial clear
85	/CS	Is	Microprocessor interface Chip select
86	SO	O	Microprocessor interface Serial data output
87	SI	Is	Microprocessor interface Serial data input
88	SCK	Is	Microprocessor interface Clock
89	SDI1	I	AC-3 bitstream (or PCM) data input terminal
90	SDI0	I	AC-3 bitstream (or PCM) data input terminal
91	SDIBCK	I	Bit clock for SDI input
92	SDIWCK	I	Word clock for SDI input
93	DVSS	-	Ground (for digital circuit)
94	DVSS	-	Ground (for digital circuit)
95	OPORT7	O	Output port for general purpose
96	OPORT6	O	Output port for general purpose
97	OPORT5	O	Output port for general purpose
98	OPORT4	O	Output port for general purpose
99	OPORT3	O	Output port for general purpose

No.	NAME	I/O	FUNCTION
100	OPORT2	O	Output port for general purpose
101	OPORT1	O	Output port for general purpose
102	OPORT0	O	Output port for general purpose
103	TESTO14	O	LSI test terminal (To be open in use)
104	TESTO13	O	LSI test terminal (To be open in use)
105	TESTO12	O	LSI test terminal (To be open in use)
106	TESTO11	O	LSI test terminal (To be open in use)
107	TESTO10	O	LSI test terminal (To be open in use)
108	TESTO9	O	LSI test terminal (To be open in use)
109	TESTO8	O	LSI test terminal (To be open in use)
110	TESTO7	O	LSI test terminal (To be open in use)
111	TESTO6	O	LSI test terminal (To be open in use)
112	TESTO5	O	LSI test terminal (To be open in use)
113	TESTO4	O	LSI test terminal (To be open in use)
114	TESTO3	O	LSI test terminal (To be open in use)
115	TESTO2	O	LSI test terminal (To be open in use)
116	TESTO1	O	LSI test terminal (To be open in use)
117	TESTO0	O	LSI test terminal (To be open in use)
118	TESTI0	I+	LSI test terminal (To be open in use)
119	TESTI1	I+	LSI test terminal (To be open in use)
120	TESTI2	I+	LSI test terminal (To be open in use)
121	TESTI3	I+	LSI test terminal (To be open in use)
122	TESTI4	I+	LSI test terminal (To be open in use)
123	TESTI5	I+	LSI test terminal (To be open in use)
124	TESTI6	I+	LSI test terminal (To be open in use)
125	TESTI7	I+	LSI test terminal (To be open in use)
126	TESTI8	I+	LSI test terminal (To be open in use)
127	TESTI9	I+	LSI test terminal (To be open in use)
128	TESTI10	I+	LSI test terminal (To be open in use)

NOTE) Is : Schmidt input terminal
I+ : Input terminal with a pull-up resistor
AI : Analog input terminal
AO : Analog output terminal

■BLOCK DIAGRAM



■FUNCTION DESCRIPTION

1. Clocks **XI, XO, VIN, VREF, CPO**

XI and XO terminals are used to make a crystal oscillator circuit. Clock signal generated by an external source can be input to XI terminal. The oscillation frequency of clock signal can be selected from 2.5MHz to 40MHz.
When the low frequency clock signal is input to XI terminal, it is necessary to generate the clock of 40MHz by using internal PLL circuit. For construct the PLL circuit, the simple analog filter must be added to VIN, VREF and CPO terminals.
On the inside of YSS243, it is operated by the clock of 20MHz that divide the clock of 40MHz by 2,

2. Data Interface **SDIBCK, SDIWCK, SDI0, SDI1, SDOBCK, SDOWCK, /SDOBCK, SDO0-3**

AC-3 bitstream or PCM data that synchronized to SDIBCK(bit clock) and SDIWCK(word clock) terminals is input from either SDI0 or SDI1 terminal.
PCM data is output from each terminals of SDO0 to SDO3. For the PCM data output, either synchronized to SDIBCK and SDIWCK terminals or synchronized to SDOBCK and SDOWCK terminals is selected by the control register.
Either SDI0 or SDI1 terminal, phase of bit clock and word clock, the format, the bit number of input and output data are selected by the control register.
The interface format of serial data is described at the item of INPUT/OUTPUT DATA FORMAT.

3. Input Data Status **AC3DATA, MUTE, CRC, KARAOKE**

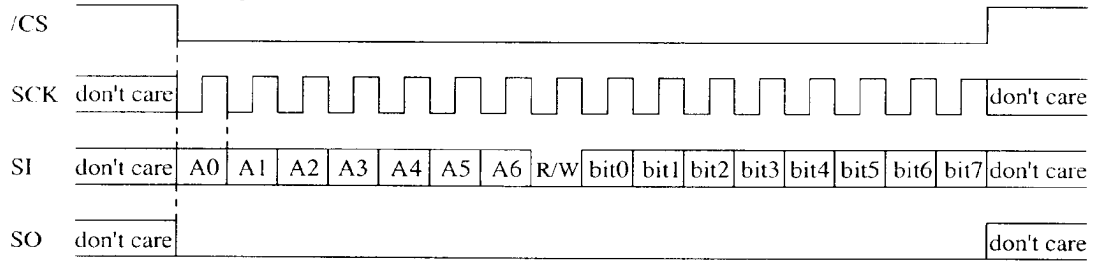
The state of SDI input signal is seen by checking the outputs of AC3DATA, MUTE, CRC and KARAOKE. These information can be read from the register of address $5F.

AC3DATA	Detect whether SDI input signal is AC-3 bitstream data.
MUTE	Detect whether output signals of SD0 to 3 are muted.
CRC	Detect whether AC-3 bitstream data includes CRC error.
KARAOKE	Detect whether SDI input signal is AC-3 karaoke data.

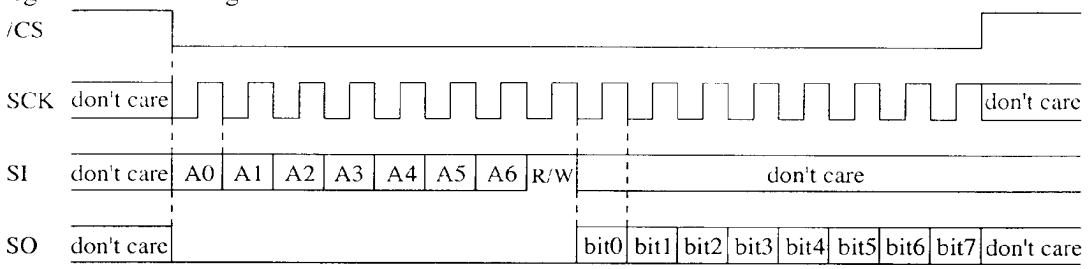
4. Microprocessor Interface **/CS, SCK, SI, SO**

The control registers can be read and written via the microprocessor interface. Four terminals of /CS, SCK, SI and SO are used for this interface.

○Register Write Timing



○Register Read Timing



After setting address (A0 to 6) to SI terminal, data (bit0 to 7) can be written to the designated address via SI terminal by setting R/W = "0". After address, data (bit0 to 7) of the designated address can be read via SO terminal by R/W = "1". Note that both address and data should be sent with LSB first.

5. General Purpose I/O ports **OPORT7-0, IPORT7-0**

OPORT7 to 0 terminals are output ports for general purpose. The data written to the register of address $06 is output from these terminals.
IPORT7 to 0 terminals are input ports for general purpose. The data input to these terminals is read from the register of address $07.

6. External RAM Interface **/RAMCE, /RAMOE, /RAMWE, RAMA0-14, RAMD0-7**

For the output PCM data, one 256Kbit (32Kword×8bit) SRAM with 35nsec or less access time is necessary.

7. Initial Clear **/IC**

This LSI requires initial clear when turning on the power.

8. LSI Test Terminals **TESTI0-30, TESTO0-14, TESTR1-2, TESTBRK**

TESTI0-30, TESTO0-14, TESTR1-2 and TESTBRK are LSI test terminals. They must be open in normal use.

■CONTROL REGISTER

The AC-3 decoding system is controlled by reading and writing the control registers through microprocessor interface (/CS, SCK, SI, SO).

※ All bits are set to "0" by initial clear except for PLL0 (bit 3) of PLL register ($00).

REGISTER MAP (1)

The following addresses ($00～$47) are registers which can read and write.

addr	NAME	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$00	PLL register	PLLUSE	PLL3 - 0				AC3/PCM	AMOFF	SDISEL
$01	DSN register	don't care				DSNIGN	DSN2 - 0		
$02	Mute register	LMUTEN	CMUTEN	RMUTEN	RSMUTEN	LSMUTEN	LFEMUTEN	M0MUTEN	M1MUTEN
$03	SDI register	don't care		SDIFMT1 - 0		SDIBIT1 - 0		SDIWP	SDIBP
$04	SDO register	SDOCKSEL	don't care	SDOFMT1 - 0		SDOBIT1 - 0		SDOWP	SDOBP
$05	SDO3 register	KROKON	don't care	SDO3FMT1 - 0		SDO3BIT1 - 0		SDO3WP	don't care
$06	OPORT register	OPORT7 - 0							
$07	IPORT register	IPORT7 - 0 (Unable to write to this register)							
$08 : $1D	(not used)	These registers are not assigned. (All "0" out when read)							
$1E	Test register 0	This register is for LSI test. Do not write.							
$1F	Test register 1	This register is for LSI test. Do not write.							
$20	Noise register	NOISE	PN/WN	NFS1 - 0		don't care			
$21	Noise Level register	NOISELEV7 - 0							
$22	MIX0 L register	MIX0L7 - 0							
$23	MIX1 L register	MIX1L7 - 0							
$24	MIX0 C register	MIX0C7 - 0							
$25	MIX1 C register	MIX1C7 - 0							
$26	MIX0 R register	MIX0R7 - 0							
$27	MIX1 R register	MIX1R7 - 0							
$28	MIX0 LS register	MIX0LS7 - 0							
$29	MIX1 LS register	MIX1LS7 - 0							
$2A	MIX0 RS register	MIX0RS7 - 0							
$2B	MIX1 RS register	MIX1RS7 - 0							
$2C	MIX0 LFE register	MIX0LFE7 - 0							
$2D	MIX1 LFE register	MIX1LFE7 - 0							
$2E	Center Delay register	don't care				CDELAY3 - 0			
$2F	Surround Delay register	don't care				SRDELAY3 - 0			
$30 : $3F	(not used)	These registers are not assigned. (All "0" out when read)							
$40	Compression register	don't care				P11OFF	DIALOFF	COMPMOD1 - 0	
$41	HDYNRNG register	HDYNRNG7 - 0							
$42	LDYNRNG register	LDYNRNG7 - 0							
$43	Output Mode register	don't care			DUALMOD1 - 0		OUTMOD2 - 0		
$44	PCM register H	PCMSFH7 - 0							
$45	PCM register L	PCMSFL7 - 0							
$46	Dither register	don't care							DITHOFF
$47	(not used)	don't care							

REGISTER MAP (2)

The following addresses ($48 ~ $7F) are read only registers. Unable to write to these registers.

addr	NAME	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$48	Bitstream register 0	fscod		frmsizecod					
$49	Bitstream register 1	bsid					bsmod		
$4A	Bitstream register 2	acmod			cmixlev		surmixlev		lfeon
$4B	Bitstream register 3	dsurmod		copyrightb	origbs	0	0	0	0
$4C	Bitstream register 4	0	0	0	dialnorm				
$4D	Bitstream register 5	0	0	0	dialnorm2				
$4E	Bitstream register 6	audprodie	mixlevel					roomtyp	
$4F	Bitstream register 7	audprodi2e	mixlevel2					roomtyp2	
$50	Bitstream register 8	timecod1e	0	timecod1					
$51	Bitstream register 9	timecod1							
$52	Bitstream register 10	timecod2e	0	timecod2					
$53	Bitstream register 11	timecod2							
$54	Bitstream register 12	langcode	langcod2e	compre	compr2e	0	0	0	0
$55	Bitstream register 13	langcod							
$56	Bitstream register 14	langcod2							
$57	Bitstream register 15	compr							
$58	Bitstream register 16	compr2							
$59	Bitstream register 17	dynrng							
$5A	Bitstream register 18	dynrng2							
$5B : $5E	(not used)	These registers are not assigned. (All "0" out when read)							
$5F	Status register	0	0	0	0	KARAOKE	MUTE	CRC	AC3DATA
$60 : $7F	(not used)	These registers are not assigned. (All "0" out when read)							

■ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	-0.5 ~ 7.0	V
Input Voltage	V_I	-0.5 ~ V_{DD} + 0.5	V
Operating Temperature	Top	-20 ~ 75	℃
Storage Temperature	Tstg	-50 ~ 125	℃

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Operating Temperature	Top	0	25	70	℃

3. DC Characteristics (Conditions : V_{DD} = 5.0±0.25V, Ta = 25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Consumption	W	V_{DD} = 5.0V		500		mW
Input Voltage H Level (1)	V_{IH1}	*1)	3.5			V
Input Voltage H Level (2)	V_{IH2}	*2)	2.0			V
Input Voltage L Level (1)	V_{IL1}	*1)			1.0	V
Input Voltage L Level (2)	V_{IL2}	*2)			0.8	V
Output Voltage H Level	V_{OH}	I_{OH} = 80μA	V_{DD}-1.0			V
Output Voltage L Level	V_{OL}	I_{OL} = 1.6mA			0.4	V
Input Leakage Current	I_{LI}		-10		10	μA
Pull-up Resistor	R_P		50		400	kΩ

*1) Applicable to XI and /IC terminals.
*2) Applicable to input terminals except XI and /IC terminals.