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Chapter 1

INTRODUCTION

1.1 General Description

YTD421B (IDR) is an analog driver/receiver LSI for the ISDN BRI S/T interface. Since YTD421B can be used on both TE (Terminal Equipment) side and NT (Network Termination) side, with connecting TTL interface LSI for TE (YTD418 or YTD423B), or that for DSU (YTD426B), each chip set allows layer 1 function conforming to ITU-T Recommendation I.430.

1.2 Features

1. Compatible with ITU-T Recommendation I.430 [1992 edition] and TTC Standard JT-I430 [1993 edition]
2. Connects directly to the Yamaha YTD418, YTD423B or YTD426B using TTL interface
3. Allows direct connection to +3.3 volt supply operation LSI(YTD418C)
4. Neither external relay nor common mode choke is required
5. 1:2 pulse transformer interface
6. Low power consumption
7. CMOS technology
8. 20-pin SSOP
9. Operates on single +5 volt supply

Chapter 2

BLOCK DIAGRAM

2.1 YTD421B Internal Block Diagram

YTD421B internal block diagram is shown in Figure 2.1.

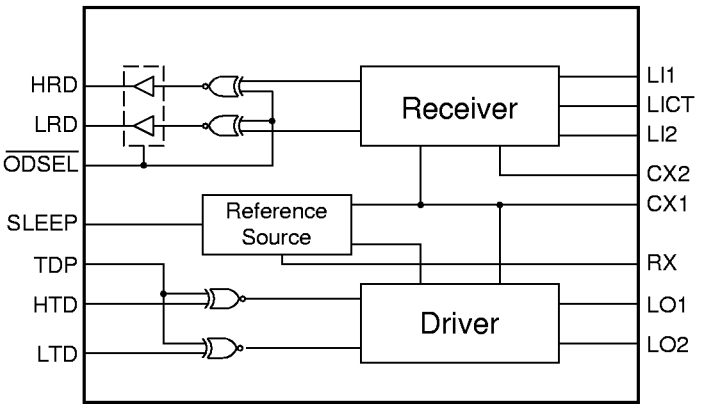


Figure 2.1: YTD421B Internal Block Diagram

2.2 System Block Diagram

YTD421B can be used as the ISDN BRI S/T interface driver/receiver on both TE side and NT side. Some examples of the system block diagram using YTD421B are shown in Figure 2.2 and Figure 2.3.

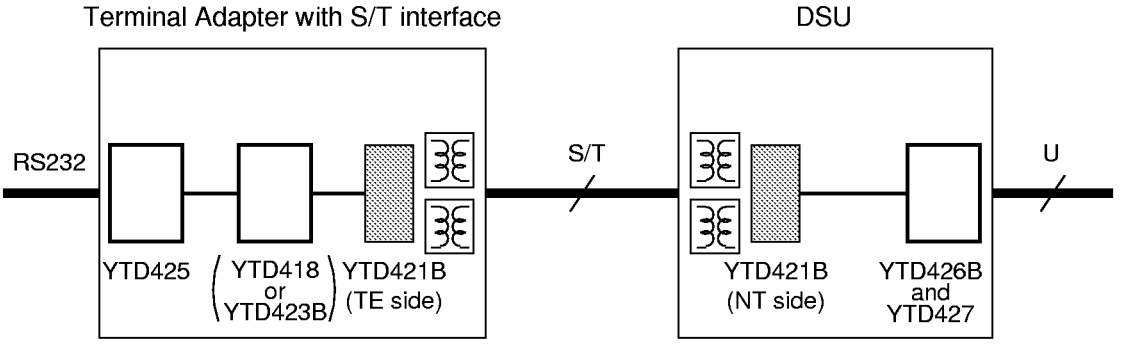


Figure 2.2: Example 1 : Terminal Adapter with S/T Interface and NT1

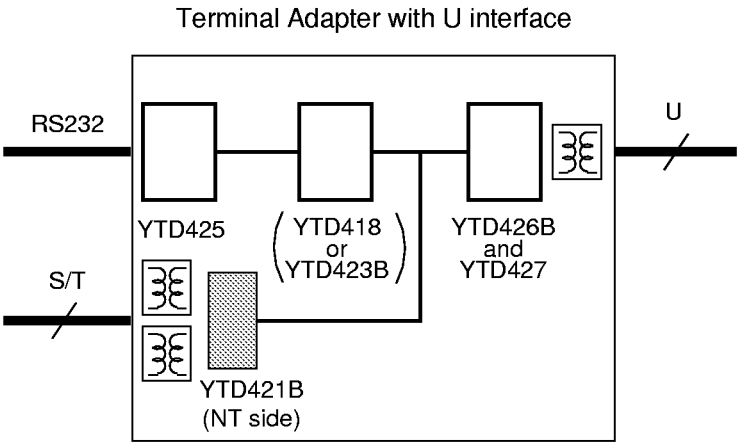


Figure 2.3: Example 2 : Terminal Adapter with U Interface

Chapter 3

PIN DESCRIPTIONS

3.1 Pin Assignments

The pin assignments of YTD421B are shown in Figure 3.1.

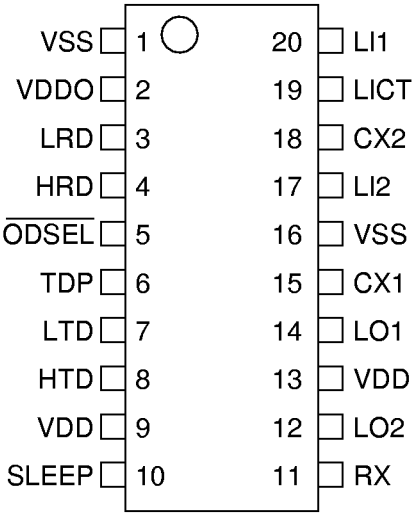


Figure 3.1: YTD421B-E (20-pin SSOP) Pin Assignments [Top View]

3.2 Pin Functions

3.2.1 Common Section

Pin No.	Pin Name	I/O	Function	Remarks
9,13	V_{DD}	PWR	+5V±5% Power supply	
1,16	V_{SS}	GND	Ground	
11	RX	–	Connect via a 27 kΩ resistor to Ground	
15	CX1	–	Connect via a 22 μF condenser to Ground	
18	CX2	–	Connect via a 0.1 μF condenser to Ground	
10	SLEEP	IN	Sleep Mode "H": Standby (Low power consumption) mode "L": Active mode	**Note 1**

Note 1: When making SLEEP pin "H", connects it to VDDO power source pin.

3.2.2 Receiver Section

Pin No.	Pin Name	I/O	Function	Remarks
4	HRD	OUT	High Pulse of Receive Data Outputs the high pulse of received AMI signal TTL interface	**Note 2**
3	LRD	OUT	Low Pulse of Receive Data Outputs the low pulse of received AMI signal TTL interface	**Note 2**
20	LI1	IN	S/T Line Input (positive) Inputs S/T interface data through a pulse transformer	
17	LI2	IN	S/T Line Input (negative) Inputs S/T interface data through a pulse transformer	
19	LICT	OUT	S/T Line Reference Source Output Connects to the pulse transformer's center tap	
5	$\overline{\text{ODSEL}}$	IN	HRD, LRD Output Select "H": HRD pin, LRD pin normal output (positive polarity) "L": HRD pin, LRD pin open drain (negative polarity)	**Note 3** **Note 4**
2	VDDO	PWR	Power Source for HRD, LRD Connects to the power source of the circuit which HRD pin and LRD pin are connected to. It enables the interface with +3.3V circuit.	

Note 2: When pulling HRD pin and LRD pin up via pull-up resistors, pulls them up to VDDO power source pin.

Note 3: When making $\overline{\text{ODSEL}}$ pin "H", connects it to VDDO power source pin.

Note 4: "positive polarity" means the condition that voltage level = "H" when logic = binary "0". "negative polarity" means the condition that voltage level = "L" when logic = binary "0".

3.2.3 Driver Section

Pin No.	Pin Name	I/O	Function	Remarks
8	HTD	IN	High Pulse of Transmit Data Inputs the high pulse of transmitting AMI signal TTL interface	**Note 5**
7	LTD	IN	Low Pulse of Transmit Data Inputs the low pulse of transmitting AMI signal TTL interface	**Note 5**
14	LO1	OUT	S/T Line Output (positive) Connects to pulse transformer which drives S/T bus	
12	LO2	OUT	S/T Line Output (negative) Connects to pulse transformer which drives S/T bus	
6	TDP	IN	HTD, LTD Input Select "H" : HTD pin, LTD pin positive polarity "L" : HTD pin, LTD pin negative polarity	**Note 6** **Note 7**

Note 5: When pulling HTD pin and LTD pin up via a pull-up resistor, pulls them up to VDDO power source pin.

Note 6: When making TDP pin "H", connect it to VDDO power source pin.

Note 7: "positive polarity" means the condition that voltage level = "H" when logic = binary "0". "negative polarity" means the condition that voltage level = "L" when logic = binary "0".

Chapter 4

FUNCTIONS

4.1 Receiver Section

The receiver section receives signal from the S/T bus through the external pulse transformer and converts it to the logic level signal.

The voltage threshold level for the receiver is properly adapted automatically according to the receiving signal level.

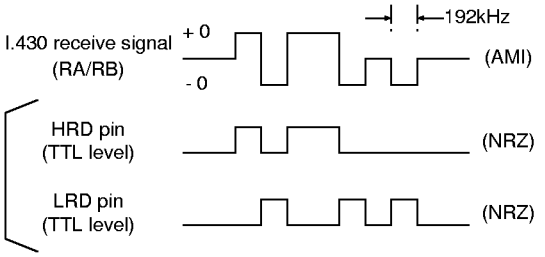


Figure 4.1: Receive signal

4.2 Driver Section

The driver section drives the 2:1 turn ratio transformer according to the logic level transmitting signal.

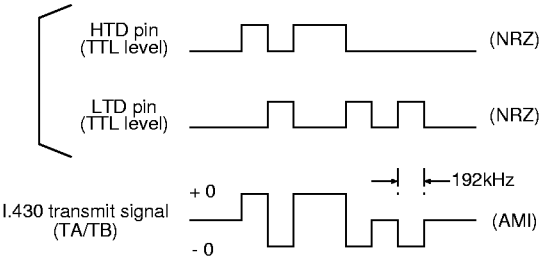


Figure 4.2: Transmit signal

4.3 Reference Source Section

The reference source section generates the reference voltage and electric current, and supplies them to the receiver section and the driver section.

Chapter 5

ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	−0.3	+7.0	V
Input Voltage	V_{IN}	−0.3	V_{DD} + 0.3	V
Operating Temperature	T_{OP}	0	+70	°C
Storage Temperature	T_{ST}	−50	+125	°C

(Based on V_{SS} = 0.0 V)

5.2 Recommended Operating Conditions

Supply Voltage	5 V± 5% (Based on V_{SS} = 0.0 V)
Operating Temperature Range	0 - 70 °C

5.3 DC Characteristics

(V_{DD} = 5 V± 5%, T_{OP} = 0 - 70 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage (CMOS)	V_{IH}	**Note 1**	$0.8V_{DD}$			V
Low-Level Input Voltage (CMOS)	V_{IL}	**Note 1**			$0.2V_{DD}$	V
High-Level Input Voltage (TTL)	V_{IH}	**Note 2**	2.2			V
Low-Level Input Voltage (TTL)	V_{IL}	**Note 2**			0.8	V
High-Level Output Voltage (TTL)	V_{OH}	**Note 3**	2.7			V
Low-Level Output Voltage (TTL)	V_{OL}	**Note 3**			0.4	V
Low-Level Output Voltage (Open-D)	V_{OL}	**Note 4**			0.4	V
Leakage Current	I_L		−10		10	μA
Off-State Leakage Current	I_{LZ}		−10		10	μA
Power Supply Current	I_{DD}	**Note 5**		10		mA
	I_{DD}	**Note 6**		5		mA
	I_{DD}	**Note 7**		0.4		mA

Note 1: With respect to TDP, $\overline{\text{ODSEL}}$, SLEEP pins.

Note 2: With respect to HTD, LTD pins.

Note 3: With respect to HRD, LRD pins ($\overline{\text{ODSEL}}$="H"). Test Conditions : I_{OH} = -0.4 mA, I_{OL}=1.2mA

Note 4: With respect to HRD, LRD pins ($\overline{\text{ODSEL}}$="L").
Test Conditions : I_{OL} = 1.2 mA

Note 5: Active mode (SLEEP pin = "L")
Test Conditions : D-channel and two B-channels = ALL "0", V_{IH}=V_{DD}, V_{IL}=V_{SS}

Note 6: Active mode (SLEEP pin = "L")
Test Conditions : one B-channel = ALL "0", V_{IH}=V_{DD}, V_{IL}=V_{SS}

Note 7: Stand-by mode (SLEEP pin = "H")
Test Conditions : input pins = V_{DD} or V_{SS}, output pins = "Open"

5.4 AC Characteristics

(V_{DD} = 5 V ± 5%, T_{OP} = 0 - 70 °C, C_L = 50 pF)

5.4.1 Receiver Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
HRD Delay Time	t_{RDR}				700	ns
HRD Delay Time	t_{RDL}				200	ns
LRD Delay Time	t_{RDH}				700	ns
LRD Delay Time	t_{RDF}				700	ns
HRD, LRD Rise Time	t_{RR}	**Note 1**			30	ns
HRD, LRD Fall Time	t_{RF}	**Note 2**			30	ns

Note 1: With respect to HRD, LRD pins ($\overline{\text{ODSEL}}$= "H").

Note 2: With respect to HRD, LRD pins.

Note 3: Figure 5.1 shows the receiver timing under the condition that $\overline{\text{ODSEL}}$ = "H".
If $\overline{\text{ODSEL}}$ = "L", the polarity of each output signal from HRD, LRD pin is reversed.

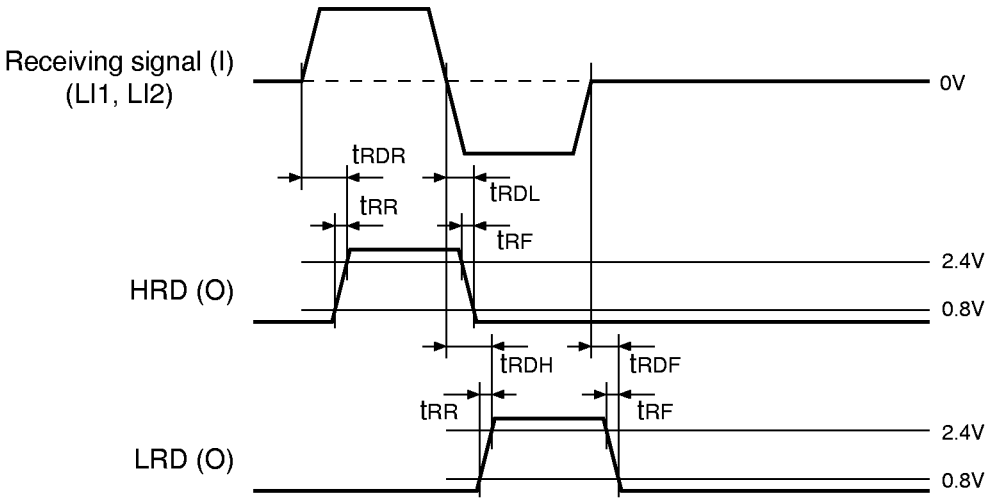


Figure 5.1: Receiver Timing

5.4.2 Driver Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
HTD, LTD Pulse Period	t_{SW}		4.95		5.45	μs
HTD, LTD Pulse Gap	t_{GAP}		0		260	ns
HTD, LTD Rise Time	t_{SR}				260	ns
HTD, LTD Fall Time	t_{SF}				30	ns
Transmitting Signal Delay Time	t_{SRL}	**Note 1**	0		490	ns
Transmitting Signal Delay Time	t_{SRH}	**Note 1**	490		1010	ns
Transmitting Singal Delay Time	t_{SFH}	**Note 1**	0		165	ns
Transmitting Singal Delay Time	t_{SFL}	**Note 1**	165		685	ns
Zero cross Delay Time	t_{SDZ}	**Note 1**	490		1010	ns

Note 1: Measured under the condition shown in Figure 5.3.

Note 2: Figure 5.2 shows the driver timing under the condition that TDR = "High".
When TDR = "Low", the polarity of each input signal to HTD, LTD pin is reversed.

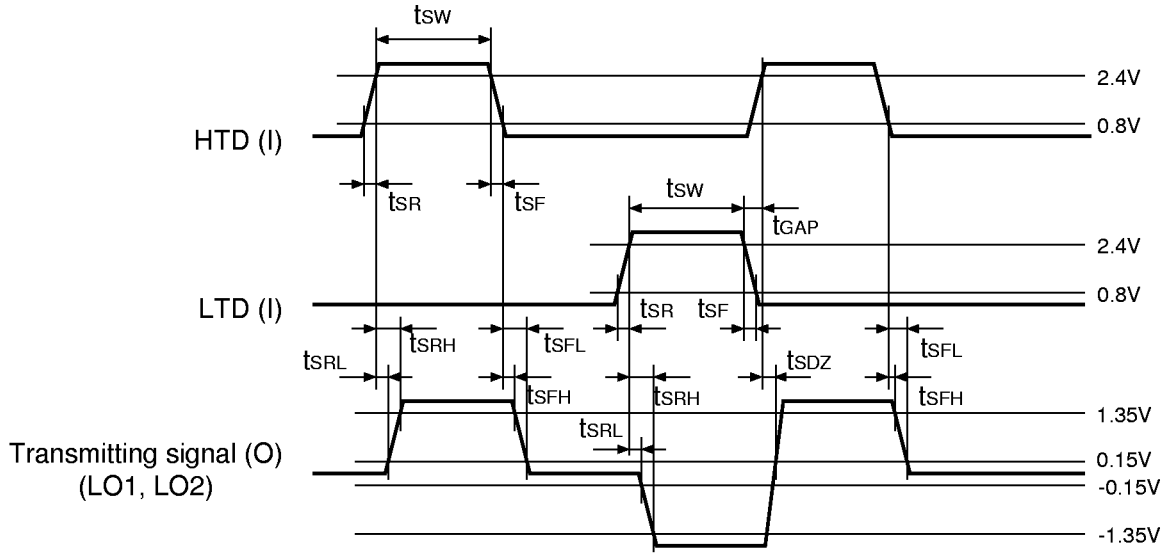


Figure 5.2: Driver Timing

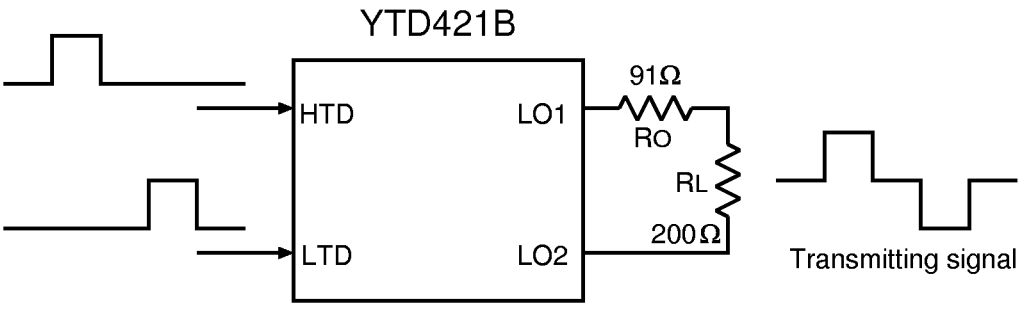


Figure 5.3: Driver Testing Circuit

5.4.3 Driver, Receiver I/O Impedance

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Receiver Input Impedance	Z_{LI}	LI1 — LI2	50			kΩ
Driver Output Impedance	Z_{LO1}	LO1 — LO2 **(Note 1)**	50			kΩ
Driver Output Impedance	Z_{LO0}	LO1 — LO2 **(Note 2)**		15		Ω

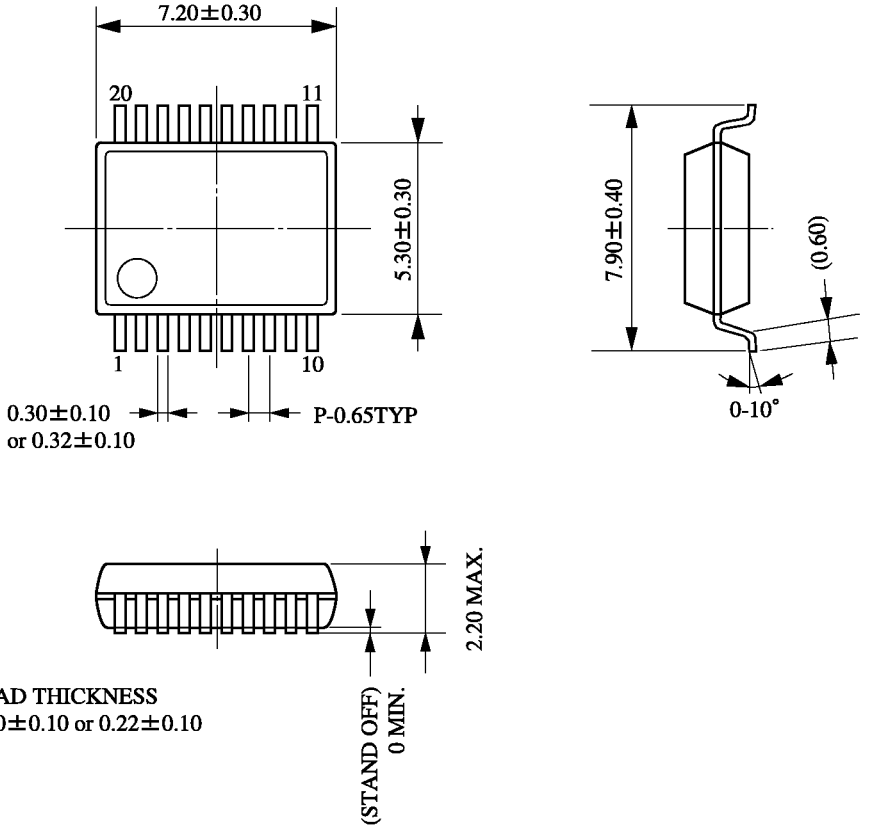
Note 1: When no pulse is output.

Note 2: When pulse is output.

Chapter 6

PACKAGE OUTLINE

C-PK20EP-1



The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

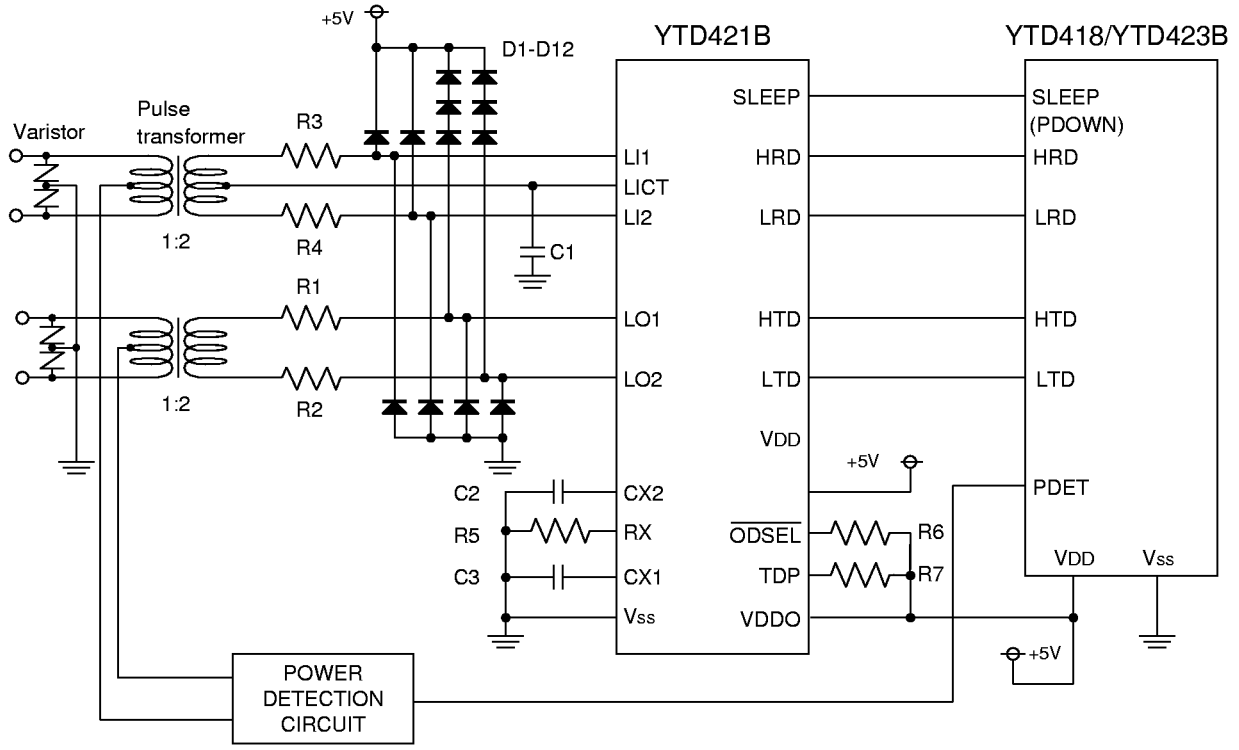
Note : The LSIs for surface mount need special consideration on storage and soldering conditions. For detailed information, please contact your nearest Yamaha agent.

Appendix A

EXAMPLE OF APPLICATIONS

A.1 Example of Application Circuits

An example circuit for connecting YTD421B to YTD418 or YTD423B is shown in Figure A.1.



(Note) If each data output pin bitween YTD421B and YTD418 or YTD423B (HRD, LRD, HTD, LTD) is set to "open drain", it requires pull-up resistor.

Figure A.1: An Example Circuit for ISDN Terminal Equipment

An example circuit for connecting YTD421B to NT1 chip is shown in Figure A.2.

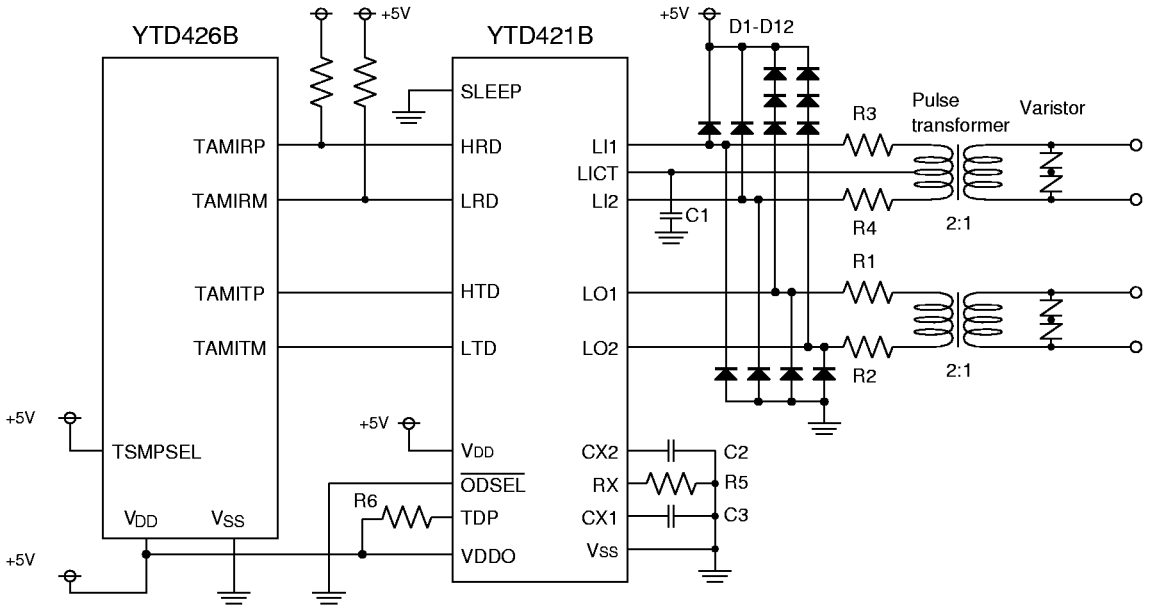


Figure A.2: An Example Circuit for NT1

Peripheral Parts :

Pulse transformer	Tokin	DDP001
	TDK	TRTEPC9.8–0386A etc.
Resistors	$R_1 = R_2 = 39\Omega$	
	$R_3 = R_4 = 8.2k\Omega$	
	$R_5 = 27k\Omega$	
	$R_6 = 10k\Omega$	
Condensers	$C_1 = C_2 = 0.1\mu F$	
	$C_3 = 22\mu$ F	
Diodes	$D_{1-12} = 1S953$	

(Note) Each resistor values (R_1, R_2, R_3 and R_4) shown here are the reference values when using one of the listed-up pulse transformers. These resistor values should be adjusted according to the peripheral parts such as pulse transformer and choke.