YAMAHA LSI

YTD426B

APPLICATION MANUAL

ITCM ISDN U Interface (TCM mode)

YAMAHA

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Contents

Chapter 1

INTRODUCTION

1.1 General Description

YTD426B is a communication LSI which provides the ISDN subscriber line interface (two-wire metaric time compression multiplexing operation) and the NT side of the ISDN Basic Rate user-network interface function (digital four-wire time-division full-duplex operation). It also provides the electric characteristics conforming to TTC Standard JT-G961 and JT-I430.

A DSU (Digital Service Unit) can easily be constructed by combining with YTD427 (Analog Front End).

It is equipped with a B channel interface circuit and can easily realize the time-division multiplexing of the B channel data on multiple ISDN lines.

In addition, with the Master/Slave function, leased lines and other lines which do not use the D channel can be directly controlled (call origination, B channel control, loopback control) without using the S/T reference point interface LSI (YTD418, YTD423B, etc.).

1.2 Features

1. Circuit Termination(CT)
   - Conforms to TTC Standard JT-G961 and JT-I430
     - Two-wire metaric time compression multiplexing operation
     - Digital four–wire time–division full–duplex operation
     - Transmission rate at U reference point: 320 kbps, at T reference point: 192 kbps
     - Frame assembling and disassembling function
     - State transition control
     - Loopback function
     - U reference point driver control
     - T reference point timing control (switch between short passive bus and long passive bus, point–to–point)
2. Line Termination(LT)
   - Conforms to TTC Standard JT-G961
     - $\sqrt{f}$ equalizer
     - Bridged Tap (BT) equalizer
   - AFE (Analog Front End) Interface
     - AGC (Automatic Gain Control)
     - Data interface
3. B channel interface section
   - B channel multiplexing circuit (LSI external clock 128k to 2,048 kHz)

- B channel connection/switching function
- Loopback function

4. Other
   - Master/Slave function
     - Ability to control a circuit without the D channel (call origination, B channel control, loopback control)
   - CMOS technology
   - 144-pin SQFP
   - Single +5V supply

Chapter 2

BLOCK DIAGRAM

2.1 YTD426B Internal Block Diagram

YTD426B internal block diagram is shown in Figure 2.1.

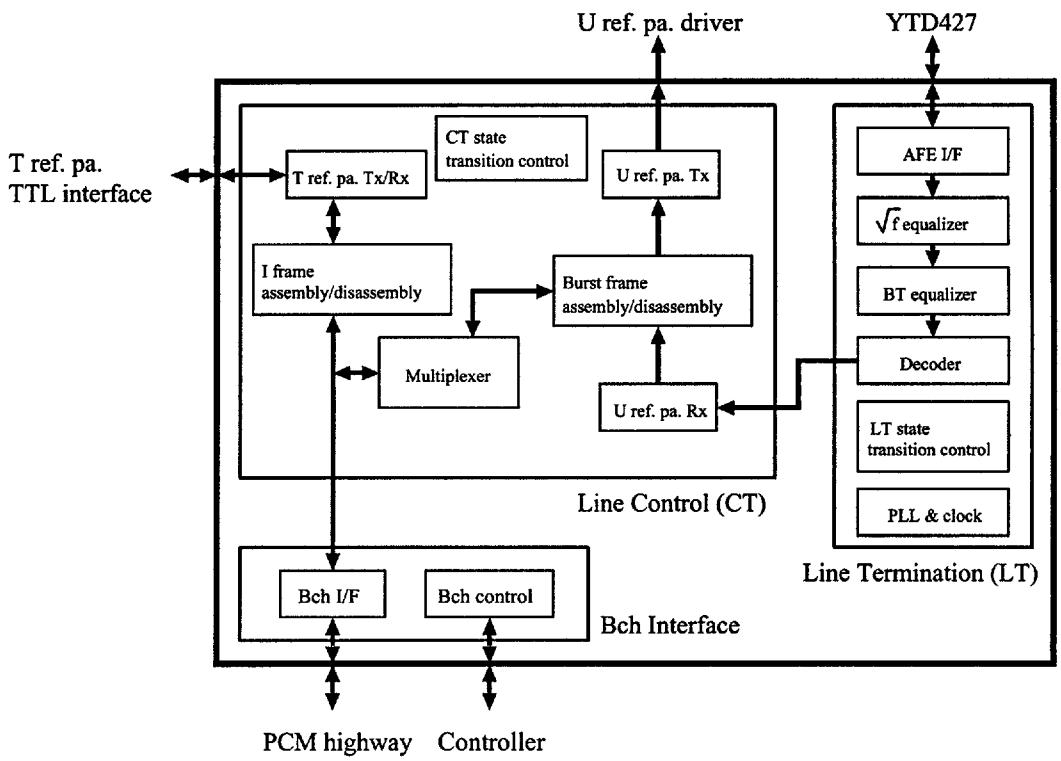


Figure 2.1: YTD426B Block Diagram

2.2 DSU Block Diagram

A DSU (Digital Service Unit) can easily be constructed by using YTD426B and YTD427 together. The DSU block diagram example is shown below.

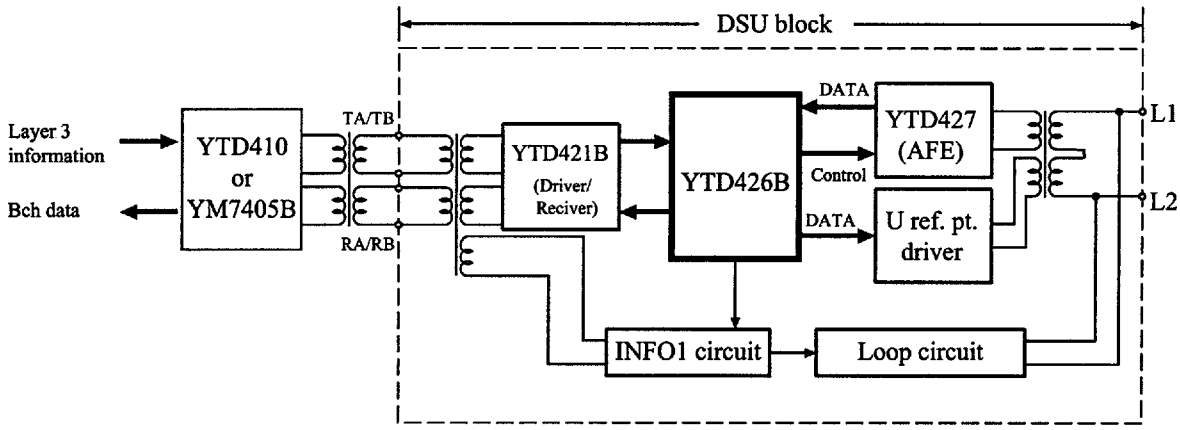


Figure 2.2: General DSU Block Diagram Example

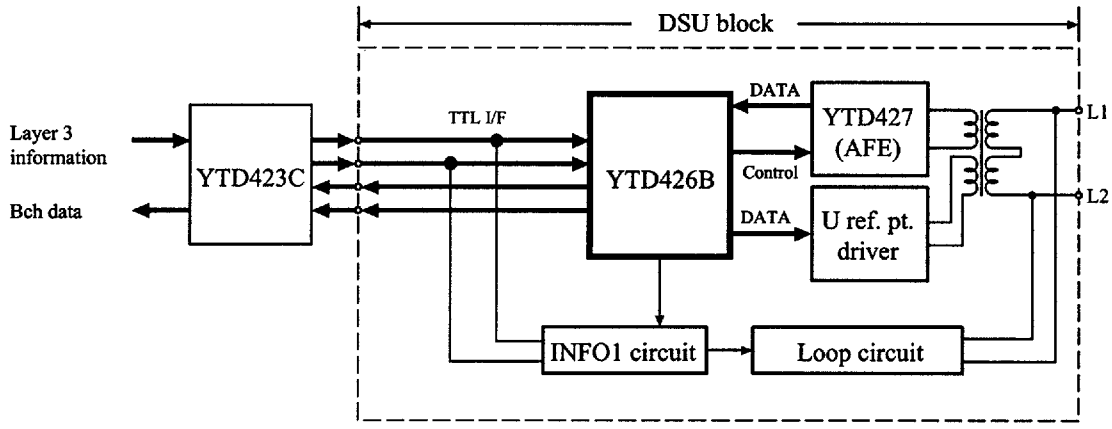


Figure 2.3: TTL Interface DSU Block Diagram Example

Chapter 3

PIN DESCRIPTIONS

3.1 Pin Assignments

The pin assignments of YTD426B are shown in Figure 3.1.

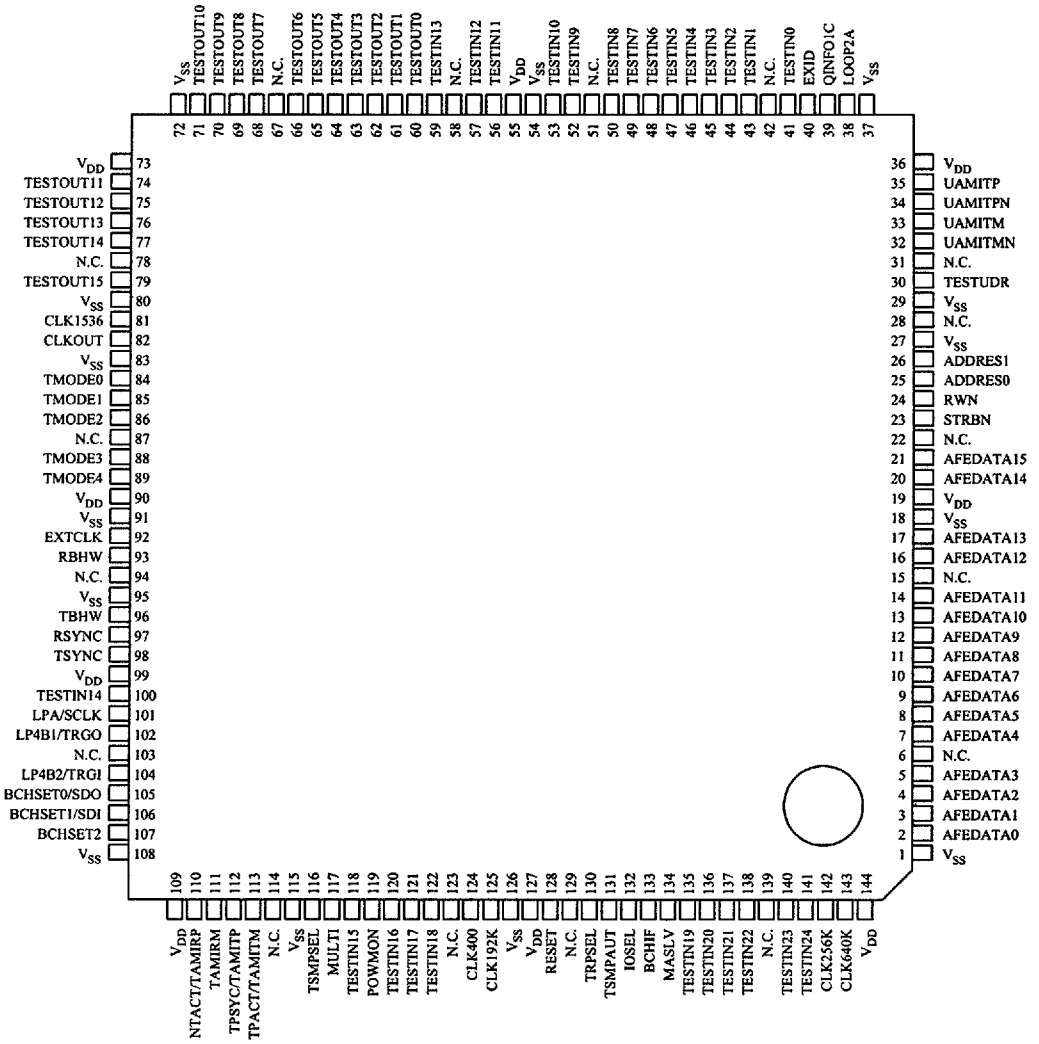


Figure 3.1: YTD426B-S (144-pin SQFP) Pin Assignments [Top View]

3.2 Pin Functions

3.2.1 Common Section

Pin No.	Pin name	I/O	Function	Remarks
19,36,55 73,90,99 109,127,144	V_{DD}	PWR	+5V power supply±10%	All pins must be joined together.
1,18,27 29,37,54 72,80,83 91,95,108 115,126	V_{SS}	GND	ground	All pins must be joined together.
81	CLK1536	IN	Master clock or crystal oscillator input. (15.36MHz ±50ppm or less)	
82	CLKOUT	OUT	Crystal oscillator output	
119	POWMON	IN	Power supply monitor pin of the equipment on the T reference point side "H": Power supply OFF "L": Power supply ON	
128	RESET	IN	Hardware reset Apply the reset pulse for 1 ms or more after the clock oscillation reset YTD426B. If the pulse is less than 1 ms, the operation is unpredictable. During the voltage polarity of U reference point is positive, input "L" to this pin.	

3.2.2 AFE Interface

Pin No.	Pin name	I/O	Function	Remarks
2	AFEDATA0	OUT	8-bit output bus to the AFE section (3 states) Connect to the D7 to D0 pins of YTD427.	with pull-up resistor
3	AFEDATA1	OUT		with pull-up resistor
4	AFEDATA2	OUT		with pull-up resistor
5	AFEDATA3	OUT		with pull-up resistor
7	AFEDATA4	OUT		with pull-up resistor
8	AFEDATA5	OUT		with pull-up resistor
9	AFEDATA6	OUT		with pull-up resistor
10	AFEDATA7	OUT		with pull-up resistor
11	AFEDATA8	IN	8-bit input bus from the AFE section Connect to the D15 to D8 pins of YTD427.	with pull-up resistor
12	AFEDATA9	IN		with pull-up resistor
13	AFEDATA10	IN		with pull-up resistor
14	AFEDATA11	IN		with pull-up resistor
16	AFEDATA12	IN		with pull-up resistor
17	AFEDATA13	IN		with pull-up resistor
20	AFEDATA14	IN		with pull-up resistor
21	AFEDATA15	IN		with pull-up resistor
23	STRBN	OUT	Strobe signal (Becomes "L" during external read/write) During read: Read the data on the rising edge. During write: The external device acquires the data on the rising edge. Connects to the STRBN pin of YTD427.	
24	RWN	OUT	Read/Write signal During write: Becomes "L" level. During all other times, it is "H". Connects to the RWN pin of YTD427.	
25	ADDRES0	OUT	YTD426B controls the AFE section for the read/write operation.	
26	ADDRES1	OUT	Connects to the A0 and A1 pins of YTD427.	
143	CLK640K	OUT	A/D sampling clock (640 kHz) Connects to the ADCK pin of YTD427.	

3.2.3 U Reference Point Interface

Pin No.	Pin name	I/O	Function	Remarks
32	UAMITMN	OUT	Negative pulse driving signal (see 5.1.2 "Transmit signal")	
33	UAMITM	OUT	Negative pulse driving signal (see 5.1.2 "Transmit signal")	
34	UAMITPN	OUT	Positive pulse driving signal (see 5.1.2 "Transmit signal")	
35	UAMITP	OUT	Positive pulse driving signal (see 5.1.2 "Transmit signal")	
38	LOOP2A	OUT	When "L": Normal operation When "H": Loopback 2 is being requested.	
39	QINFO1C	OUT	When "L": Normal operation When "H": Call control signal during loopback 2 operation	
40	EXID	IN	When "L": Transmits ID1=0. Loopback 2A is initiated for AP=1 also. When "H": Transmits ID1=1. (Extended loopback 2 supported)	with pull-up resistor

3.2.4 T Reference Point Interface

Master mode: MASLV pin = "H"

Pin No.	Pin name	I/O	Function	Remarks
110	TAMIRP	IN	T reference point receive signal (positive)	
111	TAMIRM	IN	T reference point receive signal (negative)	
112	TAMITP	OUT	T reference point transmit signal (positive)	
113	TAMITM	OUT	T reference point transmit signal (negative)	

Slave mode: MASLV pin = "L"

Pin No.	Pin name	I/O	Function	Remarks
110	NTACT	IN	DSU activation request (equivalent to INFO1 signal) "H": DSU activation Make sure the NTACT pin back to "L" after confirming the T reference point synchronization (TPSYC="H").	
111	TAMIRM	IN	This pin is not used during Slave mode. Sets to "L".	
112	TPSYC	OUT	T reference point synchronization indication "H": T reference point synchronization	
113	TPACT	OUT	T reference point activation indication "H": T reference point activation	

3.2.5 T Reference Point Option Setting

Pin No.	Pin name	I/O	Function	Remarks
116	TSMPSEL	IN	Selects the receive data sampling timing at the T reference point. "L": Adaptive timing "H": Fixed timing Usually fixed to "L".	with pull-up resistor
117	MULTI	IN	Sets the multiframe support on the T reference point side. "L": Do not support multiframe (Use of the Qbit is impossible.) "H": Support multiframe (Use of the Qbit is possible.) Usually fixed to "H".	with pull-up resistor
130	TRPSEL	IN	Sets the receive signal polarity on the T reference point †. "L": TAMIRP and TAMIRM pins are positive polarity. "H": TAMIRP and TAMIRM pins are negative polarity.	with pull-up resistor
131	TSMPAUT	IN	Usually fixed to "H".	with pull-up resistor

† "positive polarity" means the condition that voltage level = "High" when logic = binary "0". (See 5.2 T Reference Point Interface)

3.2.6 Mode Setting

Pin No.	Pin name	I/O	Function	Remarks
132	IOSEL	IN	Selects the Serial/Port control. "L": Serial control "H": Port control	with pull-up resistor
133	BCHIF	IN	Sets B channel data input/output I/F "L": Inputs/Outputs the B channel data through the B channel interface. "H": Inputs/Outputs the B channel data according to TTC Standard JT-I430 format. Sets the BCHIF pin to "L" during Slave mode.	with pull-up resistor
134	MASLV	IN	Selects Master/Slave mode. "H": Master mode (Connects the T reference point) "L": Slave mode (Disconnects the T reference point) Sets the BCHIF pin to "L" during Slave mode.	with pull-up resistor

3.2.7 B Channel Interface

Effective only when BCHIF pin = "L".

Pin No.	Pin name	I/O	Function	Remarks
92	EXTCLK	IN	B channel clock (128k to 2,048kHz)	with pull-down resistor
93	RBHW	OUT (O.D.)	B channel receive data output	
96	TBHW	IN	B channel transmit data input	with pull-down resistor
97	RSYNC	IN	8kHz T reference point synchronization pulse for the B channel receive data	with pull-down resistor
98	TSYNC	IN	8kHz T reference point synchronization pulse for the B channel transmit data	with pull-down resistor

IOSEL pin= "L" (during Serial control)

Pin No.	Pin name	I/O	Function	Remarks
101	SCLK	IN	Serial data synchronization clock	with pull-down resistor
102	TRGO	IN	Serial output trigger	with pull-down resistor
104	TRGI	IN	Serial input trigger	with pull-down resistor
105	SDO	OUT	Serial data output	with pull-down resistor
106	SDI	IN	Serial data input	with pull-down resistor
107	BCHSET2	IN	This pin is not used during the Serial mode. Sets to "L".	with pull-down resistor

IOSEL pin= "H" (during Port control)

Pin No.	Pin name	I/O	Function	Remarks
101	LPA	IN	Executes loopback A. "H": During loopback A "L": Normal mode	with pull-down resistor
102	LP4B1	IN	Executes the B1 Loopback on Loopback 4. "H": During B1 loopback "L": Normal mode	with pull-down resistor
104	LP4B2	IN	Executes the B2 Loopback on Loopback 4. "H": During B2 loopback "L": Normal mode	with pull-down resistor
105	BCHSET0	IN	Switches B channel connection data (See 5.3.2).	with pull-down resistor
106	BCHSET1	IN	B channel interface TB1/RB1 time slot connection (See 5.3.2)	with pull-down resistor
107	BCHSET2	IN	B channel interface TB2/RB2 time slot connection (See 5.3.2)	with pull-down resistor

3.2.8 Other

Pin No.	Pin name	I/O	Function	Remarks
124	CLK400	IN	This pin outputs 400 Hz clock. (Synchronized with U interface line clock.)	
125	CLK192K	IN	This pin outputs 192 kHz clock. (Synchronized with T interface line clock.)	
142	CLK256K	OUT	This pin outputs 256 kHz clock.	

3.2.9 Testing

These are not used during normal operation.

Pin No.	Pin name	I/O	Function	Remarks
41,43~50 52,53 56,59 118,120 121	TESTIN 0~11,13 15,16,17	IN	These are test pins. Sets to "H".	with pull-up resistor
57,100	TESTIN 12,14	IN	These are test pins. Sets to "L".	with pull-down resistor
122	TESTIN18	IN	This is a test pin. Sets to "H".	with pull-down resistor
135~137 141	TESTIN 19,20,21,24	IN	These are test pins. Sets to "L".	
138,140	TESTIN 22,23	IN	These are test pins. Sets to "L".	
60~66 68~71 74~77,79	TESTOUT 0~15	OUT	These are test pins. These pins must be left unconnected.	
84~86 88,89	TMODE 0~4	IN	These are test pins. Sets to "H".	with pull-up resistor
30	TESTUDR	IN	This is a test pin. Sets to "H".	with pull-up resistor
6,15,22 28,31,42 51,58,67 78,87,94 103,114 123,129 139	N.C.	–	These pins must be left unconnected.	

Chapter 4

FUNCTIONS

4.1 Circuit Termination Block

The circuit termination consists of the following functions:

- Rate adaptation and frame assembly/disassembly at the U and T reference points
- State transition control
- Loopback control
- U reference point drive control
- T reference point receive timing control

It provides the necessary functions for TTC Standard JT-G961 (TCM operation) and the NT function described in TTC Standard JT-I430.

4.2 Line Termination Block

The line termination provides the $\sqrt{f}$ equalization which compensates the DLL(Digital Local Line) loss and the amplitude distortion, and the BT equalization which compensates the waveform distortion caused by the bridged tap.

4.3 B Channel Interface Block

The B channel interface function is enabled or disabled with the BCHIF pin.

By using the B channel interface function, B channel data can be inputed and outputted without going through the S/T reference point LSI (YTD418, YTD423B, etc.).

The time division multiplexing of the B channel data on multiple ISDN lines can be realized by inputting or outputting the data in synchronous with the 128k to 2,048kHz external clock.

4.4 Master/Slave Function

The Master/Slave mode is set with the MASLV pin.

4.4.1 Master Mode

The Master mode is for configuring a normal DSU which exchanges the signals comforming to TTC Standard JT-I430 frame (TTL interface).

The Master mode can be used with the B channel interface function (BCHIF pin = "L") in the Master mode. In this case, the B channel data output to the T side become all "1"s. Note that, the B channel data which received from the T side are ignored, and a T reference point interface LSI must be used for the D channel control.

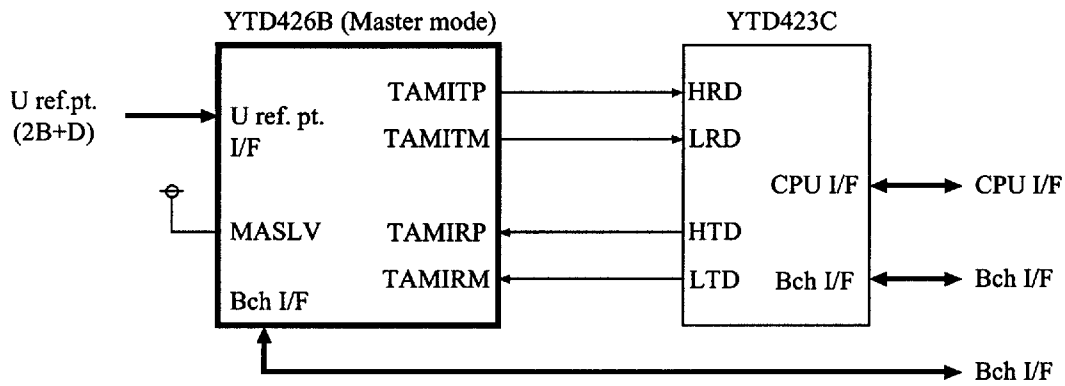


Figure 4.1: Master Mode Connection Example (TTL Interface)

4.4.2 Slave Mode

The Slave mode is for directly controlling the line (call origination, B channel control, loopback control) without using the T reference point interface when connecting to such a line which does not use the D channel function as a leased line. The B channel interface function is always used in the Slave mode. (BCHIF pin = "L")

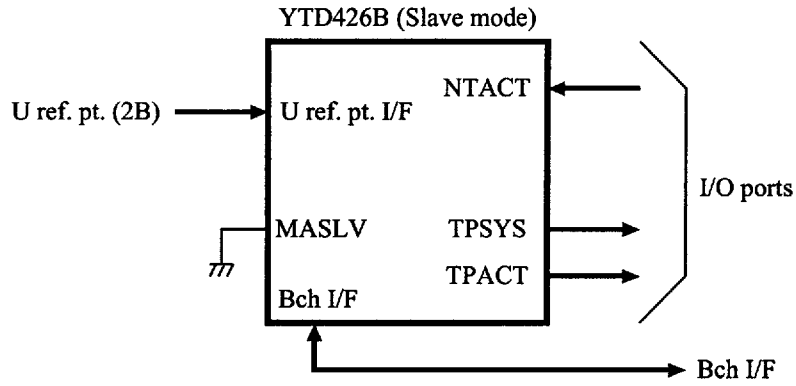


Figure 4.2: Slave Mode Connection Example
(BCHIF pin = "L")

A call is initiated with the NTACT pin.
There are two methods used for controlling the B channel and the loopback.

1. Serial control
2. Port control

The control method is switched with the IOSEL pin.
For Serial control, the control data is input or output by synchronizing to the 128k to 2,048kHz external clock.
For Port control, the loopback is controlled by setting LPA, LP4B1 and LP4B2 pins. The B channel is controlled by setting BCHSET0, BCHSET1 and BCHSET2 pins.

Chapter 5

HARDWARE INTERFACE

5.1 U Reference Point Interface

5.1.1 Receive Signal

The receive signal from the U reference point is converted to 8-bit data by YTD427 and passed to YTD426B. YTD426B also controls YTD427. The time chart of the interface signal to the AFE (Analog Front End) is shown in Figure 5.1.

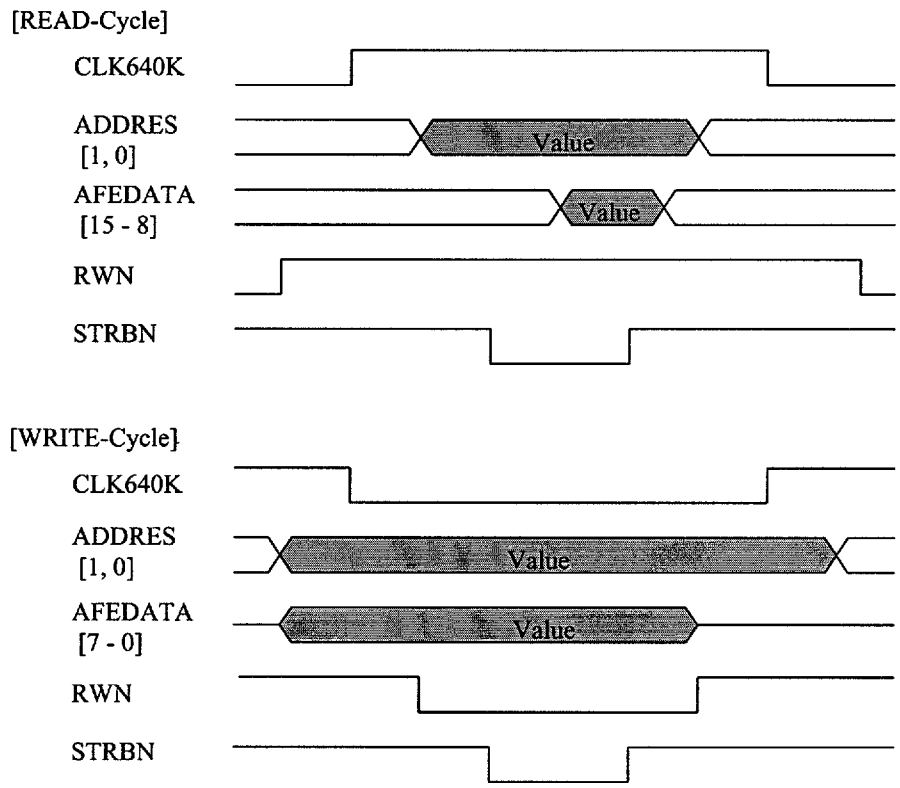


Figure 5.1: U Reference Point Interface (Receive Signal)

5.1.2 Transmit Signal

The transmit signal to the U reference point is passed through the external driver circuit. Driver circuit example is shown below.

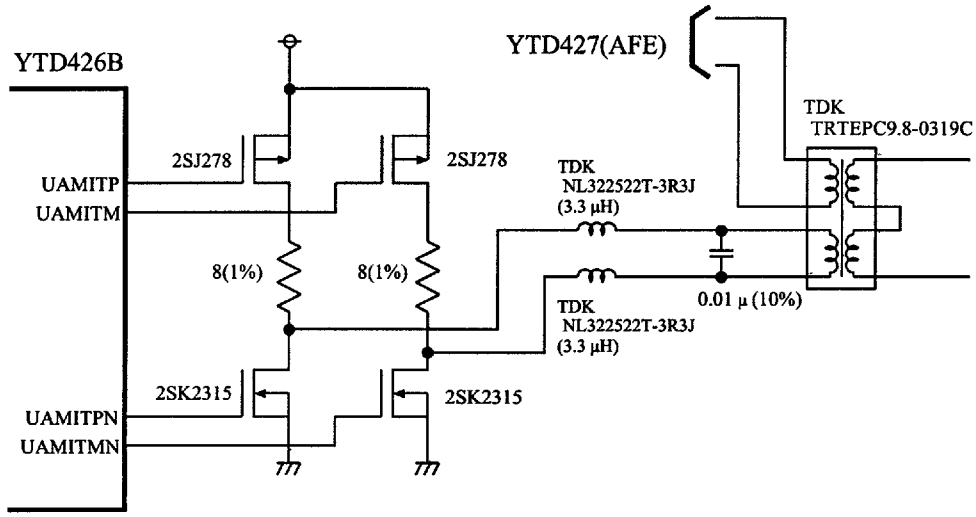


Figure 5.2: Driver Circuit Example

5.2 T Reference Point Interface

The interface to the T reference point side of YTD426B conforms to TTC Standard JT-I430(TTL interface).
When the AMI signal is "0", the pin is "H".
Do not apply "H" to TAMIRP and TAMIRM pins simultaneously, or results in abnormal operation.
The time chart is shown in Figure 5.3.

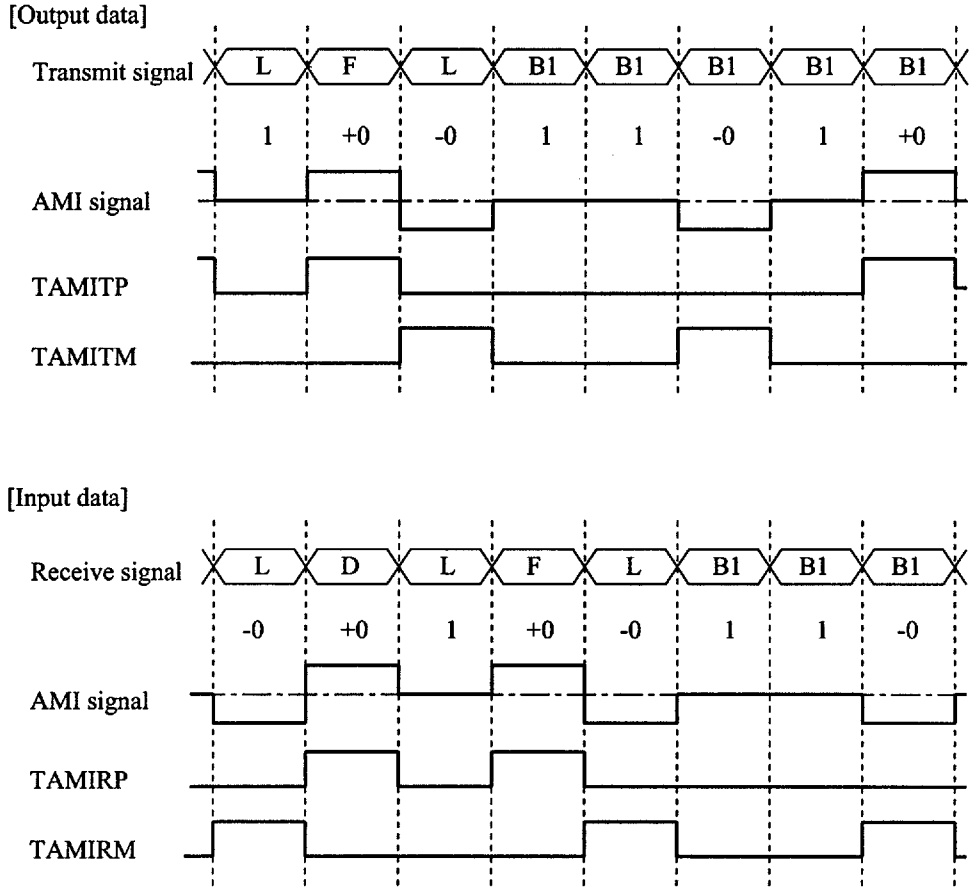


Figure 5.3: T Reference Point Interface

5.3 B Channel Interface

5.3.1 Signal

YTD426B can input or output the B channel data by synchronizing with a 128k to 2,048 kHz external clock.

The data input/output is initiated with the 8 kHz TSYNC/RSYNC signal. The data is acquired from the TBHW pins on the falling edge of the EXTCLK. Similarly, the data is output from the RBHW pins on the rising edge of the EXTCLK. During these operations, EXTCLK, TSYNC and RSYNC must be synchronized to the network by such circuit as the PLL circuit.

Because each Input pin and Output pin is allocated individually, the B1 and B2 channel data can be continuously input or output. However, depending on the relative position with the TSYNC/RSYNC signals, TB1/RB1 and TB2/RB2 time slot are specified.

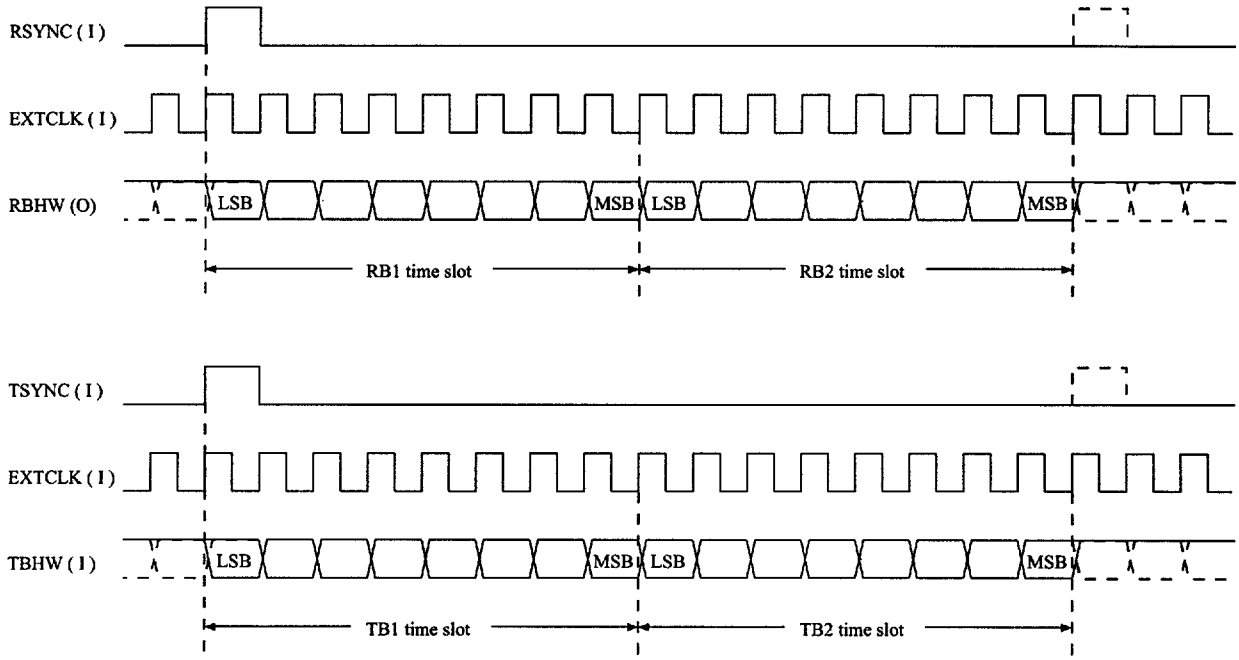


Figure 5.4: B Channel I/O Timing During External Clock Mode

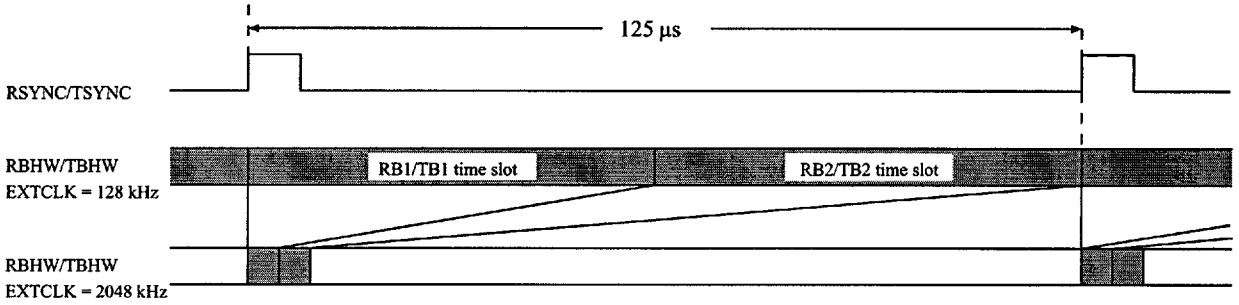


Figure 5.5: Time Slot with Respect to the External Clock Frequency

5.3.2 B Channel Control

The B channel data connection is controlled by specifying both BCHSET0-BCHSET2 pins and bits of D4 to D2 of control data as shown in the following table. If this selection/switch is not specified at initiation, both B1 and B2 channels will be disconnected (default).

Pin setting(BCHSET0,1,2) Control data setting(D2,D3,D4)		Time slot for transmitting and receiving from the B1 channel	Time slot for transmitting and receiving from the B2 channel
BCHSET0,1,2 D2,D3,D4	[L,L,L] [L,L,L]	–	–
BCHSET0,1,2 D2,D3,D4	[L,H,L] [L,L,H]	TB1/RB1	–
BCHSET0,1,2 D2,D3,D4	[L,L,H] [L,H,L]	–	TB2/RB2
BCHSET0,1,2 D2,D3,D4	[L,H,H] [L,H,H]	TB1/RB1	TB2/RB2
BCHSET0,1,2 D2,D3,D4	[H,L,L] [H,L,L]	–	–
BCHSET0,1,2 D2,D3,D4	[H,L,H] [H,H,L]	TB2/RB2	–
BCHSET0,1,2 D2,D3,D4	[H,H,L] [H,L,H]	–	TB1/RB1
BCHSET0,1,2 D2,D3,D4	[H,H,H] [H,H,H]	TB2/RB2	TB1/RB1

5.3.3 Loopback Control

YTD426B supports two loopback control functions which are usually performed on the TE side for testing and maintenance.

The loopback modes are specified either with the control data during Serial control or with setting the pins during Port control.

Loopback 4 mode

The selected B channel from the signal from the network is looped back toward the network.

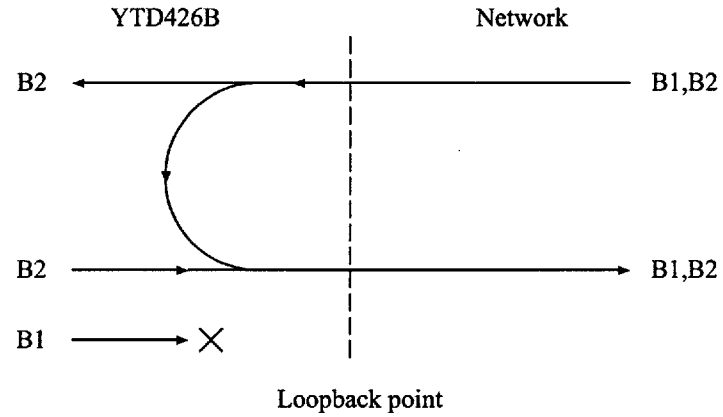


Figure 5.6: Loopback 4 (when only B1 channel is looped back

Loopback A mode

The signal from YTD426B is internally looped back toward YTD426B.

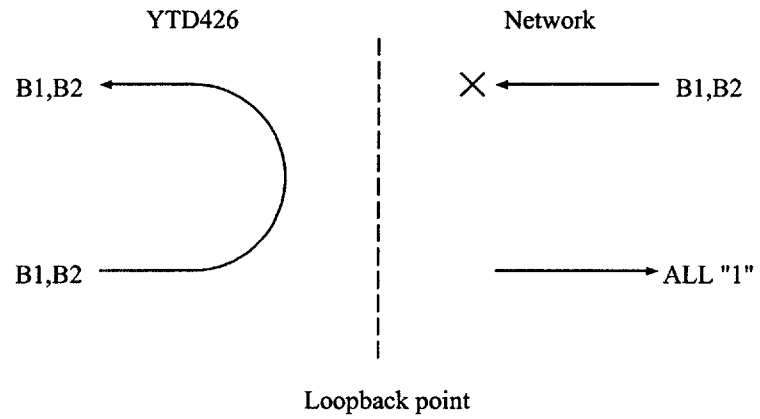


Figure 5.7: Loopback A (An example of B1, B2 loopback)

5.4 Serial Control Interface

The control data can be input or output synchronously with the 128k to 2,048kHz external clock when using the B channel interface function and controlling the line with Serial control (BCHIF pin="L", IOSEL pin="L").

The data I/O is initiated by the input of the TRGO/TRGI signal. The control data is acquired from the SDI pin on the falling edge of the SCLK, while the control data is output from the SDO pin on the rising edge of the SCLK.

The following setting/information can be input or output with the control data.

- B channel control
- Loopback control
- T reference point state information during slave

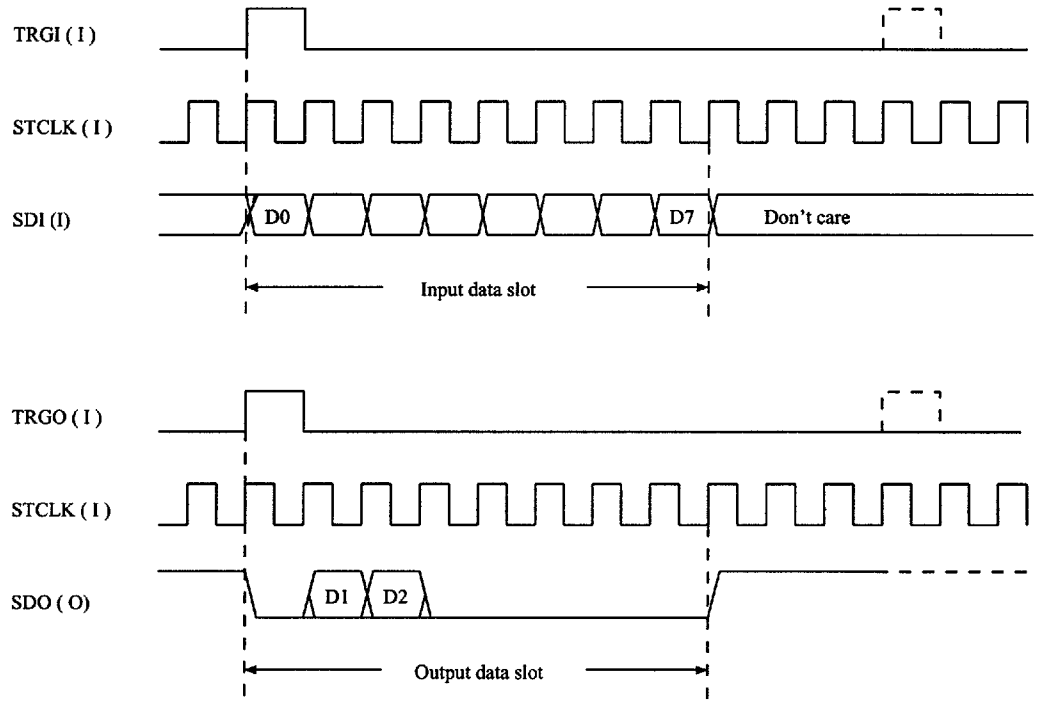


Figure 5.8: Serial Control Interface

Chapter 6

SOFTWARE INTERFACE

6.1 Serial Control Interface

When using YTD426B in Slave mode and controlling the line with Serial control, the T reference point condition is indicated as serial data. The B channel connection/switch and the loopback using the B channel interface function can also be set with the serial data.

6.1.1 MPH-DATA-INDICATION

Indicates the T reference point condition.

—	—	—	—	—	D2	D1	—	READ

Bit	Function
D1	Indicates the synchronized/lost synchronization state of the T reference point. 1 : Lost synchronization 0 : Synchronized
D2	Indicates the deactivated/activated state of the T reference point. 1 : Deactivated 0 : Activated

6.1.2 B Channel Control, Loopback Control

Sets the B channel connection/switch and loopback.

—	D6	D5	D4	D3	D2	D1	D0	WRITE

Bit	Function
D0,D1	Sets the loopback type. D1 D0 1 0 : B channel data loopback at the network side (loopback 4) 1 1 : B channel data loopback at the user side (loopback A)
D2	B channel connection data switch(See 5.3.2)
D3	TB2/RB2 time slot connection (See 5.3.2)
D4	TB1/RB1 time slot connection (See 5.3.2)
D5	Loopback 4, set B1 loopback
D6	Loopback 4, set B2 loopback

Chapter 7

ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	−0.3	+7.0	V
Input Voltage	V_{IN}	−0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	−20	+70	℃
Storage Temperature	T_{ST}	−50	+125	℃

(Based on V_{SS}=0.0V)

7.2 Recommended Operating Conditions

Supply Voltage	5.0 V±10% (Based on V_{SS} = 0.0 V)
Operating Temperature Range	−20 — 70 ℃

7.3 DC Characteristics

1. TTL interface input

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	V_{IH}		2.4			V
Low-Level Input Voltage	V_{IL}				0.8	V
Leakage Current	I_L	V_I=V_{SS} or V_{DD}	−10		+10	μA

Note: With respect to the input pins other than TESTIN15, POWMON and RESET pins.

2. TTL interface Schmitt input

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	V_{IH}		3.0			V
Low-Level Input Voltage	V_{IL}				0.8	V
Leakage Current	I_L	V_I=V_{SS} or V_{DD}	−10		+10	μA
Schmidt width	V_{SM}			1.6		V

Note: With respect to TESTIN15, POWMON and RESET pins.

3. CMOS interface output

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	V_{OH}	I_{OH} = -80.0 μA	V_{DD}−1.0			V
Low-Level Input Voltage	V_{OL}	I_{OL} = 1.6mA			V_{SS}+0.4	V
Leakage Current	I_{LZ}	V_I = V_{SS} or V_{DD}	−10		+10	μA

Note: With respect to pins other than the RBHW pins.

4. Open drain output

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Low-Level Output Voltage	V_{OL}	I_{OL}=1.6mA			V_{SS}+0.4	V
Leakage Current	I_{LZ}	V_I=V_{SS} or V_{DD}	−10		+10	μA

Note: With respect to the RBHW pins.

5. Power Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Power Consumption	P_{DT}	Drive		75		mW
Power Consumption	P_{DR}	Receive		85		mW

7.4 AC Characteristics

7.4.1 AFE interface

Output load condition

I_{OH} = -80 μA C_L = 50 pF

I_{OL} = 1.6 mA C_L = 50 pF

- Read timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Valid Address Time 1	t_{RCT1}		100			ns
Valid Address Time 2	t_{RCT2}		100			ns
RWN Setup Time	t_{RCT3}		100			ns
RWN Hold Time	t_{RCT6}		100			ns
Data Delay Time	t_{RCT4}				40	ns
Data Hold Time	t_{RCT5}		0		40	ns
STRBN Width	t_{RCT8}		90			ns
Address Setup Time	t_{RCT7}		30			ns
Address Hold Time	t_{RCT9}		60			ns

- Write timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Address Setup Time	t_{WCT1}		100			ns
Address Hold Time	t_{WCT2}		100			ns
Data Setup Time 1	t_{WCT3}		100			ns
Data Hold Time	t_{WCT4}		40			ns
Data Setup Time 2	t_{WCT5}		100			ns
RWN Delay Time	t_{WCT6}		100			ns
RWN Setup Time 1	t_{WCT7}		100			ns
RWN Setup Time 2	t_{WCT8}		30			ns
RWN Hold Time	t_{WCT10}		60			ns
STRBN Width	t_{WCT9}		90			ns

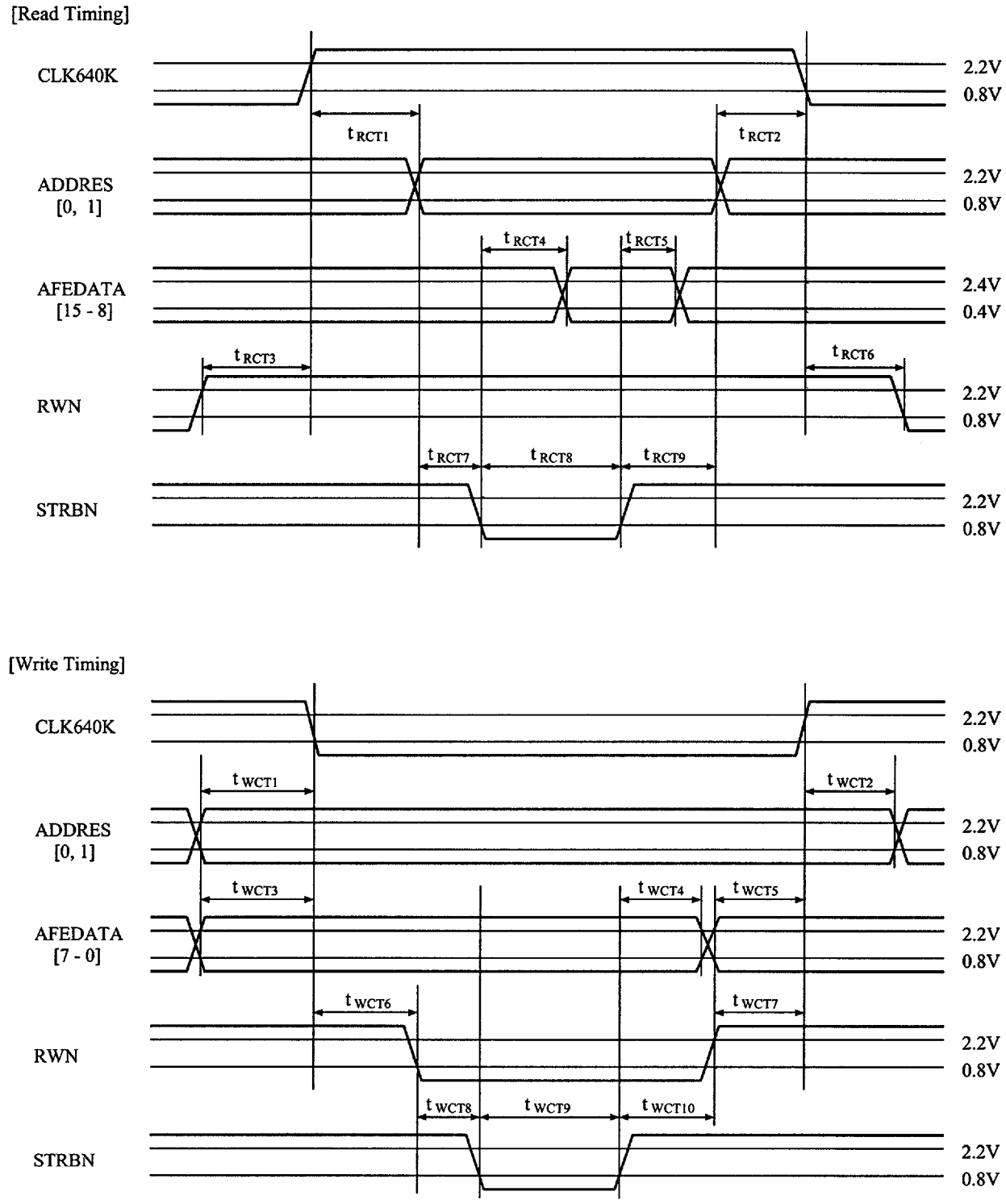


Figure 7.1: AFE Interface

7.4.2 B Channel Interface

Output Load Condition

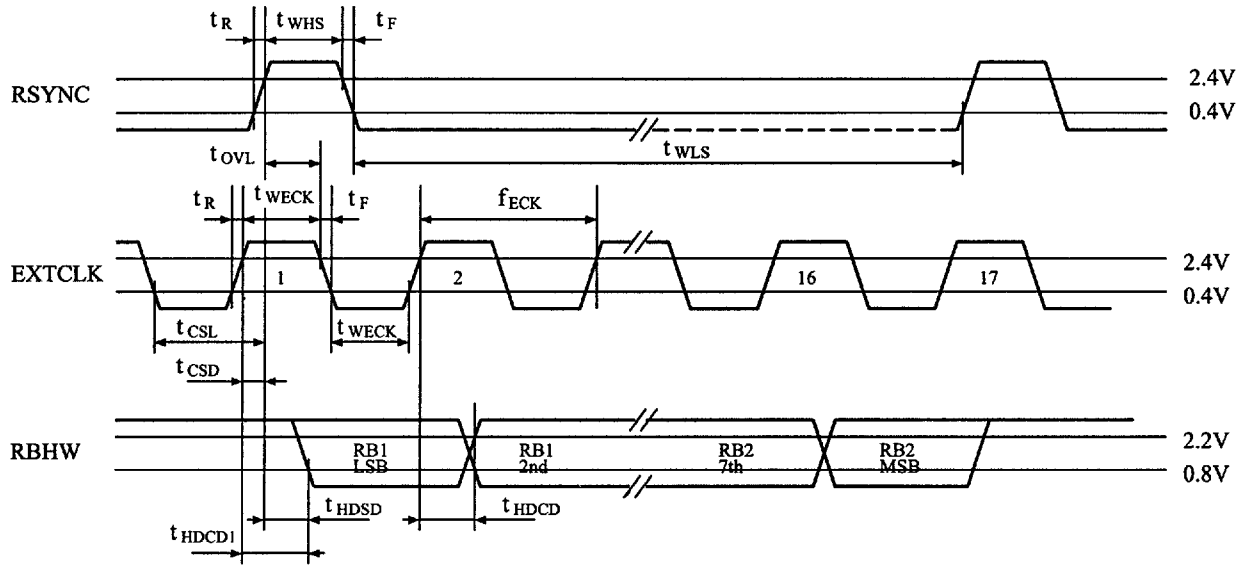
I_{OH} = -80 μA C_L = 50 pF

I_{OL} = 1.6 mA C_L = 50 pF

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Clock Frequency	f_{ECK}		128		2,048	kHz
Clock Cycle Period	t_{WECK}		200			ns
SYNC Frequency	f_{TSYNC}			8		kHz
SYNC High-Level Period	t_{WHS}		200			ns
SYNC Low-Level Period	t_{WLS}		8			μs
SYNC-Clock Overlap	t_{OVL}		150			ns
Digital Input Rise Time	t_R				50	ns
Digital Input Fall Time	t_F				50	ns
SYNC Timing to Clock	t_{CSL}		100			ns
	t_{CSD}				100	ns
Data Output Delay Time to Clock(**Note**)	t_{HDCD1}				170	ns
Data Output Delay Time to SYNC(**Note**)	t_{HDSD}				170	ns
Data Output Delay Time	t_{HDCD}				180	ns
Data Input Setup Time	t_{HDS}		65			ns
Data Input Hold Time	t_{HDH}		120			ns

(**Note**) Based on the slower signal between clock and SYNC.

[Receve Data Timing]



[Transmit Data Timing]

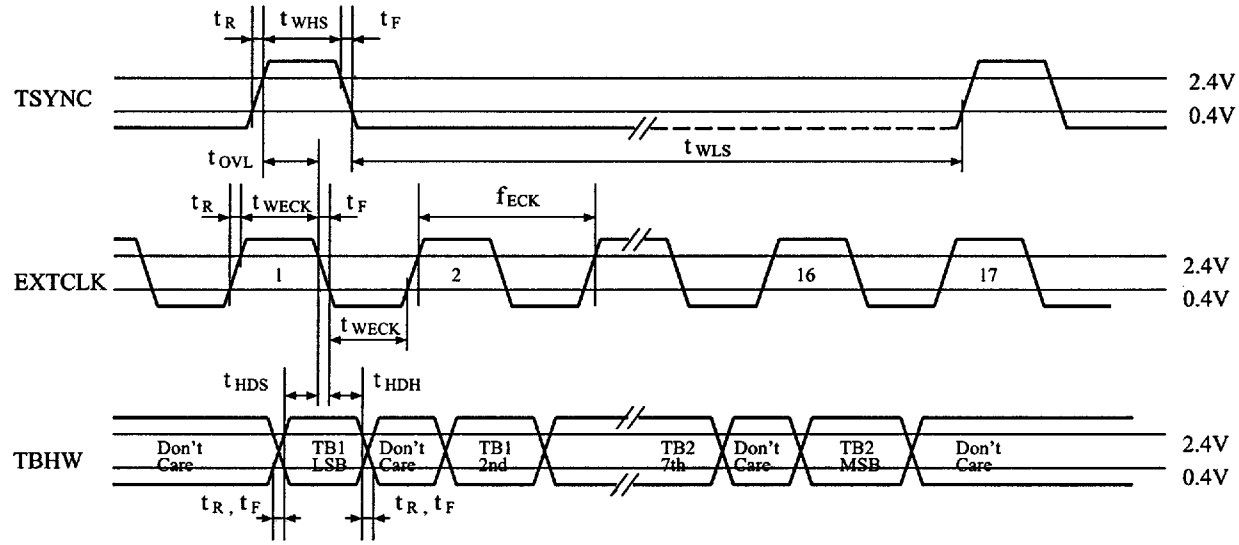
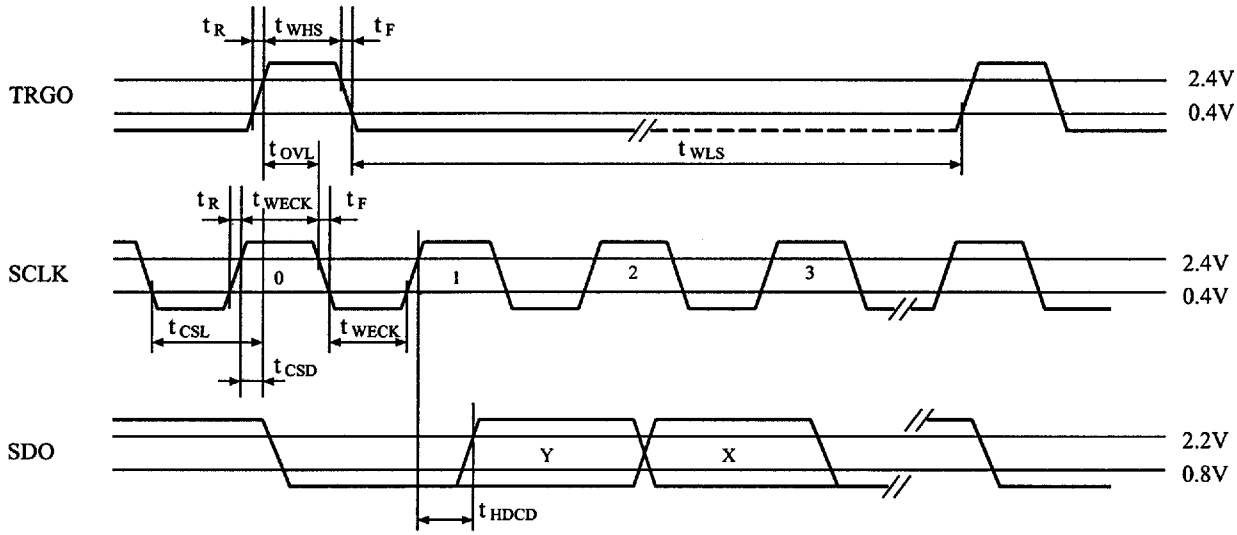


Figure 7.2: B Channel Interface

7.4.3 Serial Data Interface

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Clock Frequency	t_{ECK}		128		2,048	kHz
Clock Cycle Period	t_{WECK}		200			ns
SYNC Frequency	t_{SYNC}			8		kHz
SYNC High-Level Period	t_{WHS}		200			ns
SYNC Low-Level Period	t_{WLS}		8			μs
SYNC-Clock Overlap	t_{OVL}		150			ns
Digital Input Rise Time	t_R				50	ns
Digital Input Fall Time	t_F				50	ns
SYNC Timing to Clock	t_{CSL}		100			ns
	t_{CSD}				100	ns
Data Output Delay Time	t_{HDCD}				180	ns
Data Input Setup Time	t_{HDS}		65			ns
Data Input Hold Time	t_{HDH}		120			ns

[Serial Data Output Timing]



[Serial Data Input Timing]

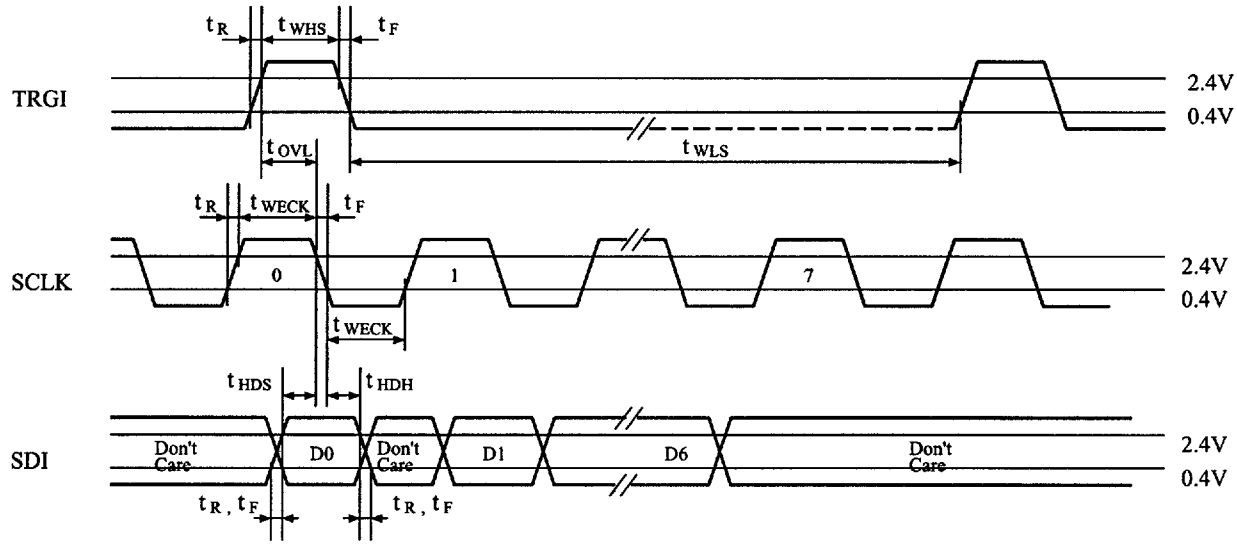


Figure 7.3: Serial Data Interface

7.4.4 T Reference Point Interface

Output Load Condition

I_{OH} = -80 μA C_L = 50 pF

I_{OL} = 1.6 mA C_L = 50 pF

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Transmit Pulse Width	t_{TPW}		5.00	5.208	5.40	μs
Receive Pulse Width	t_{RPW}			5.208		μs
Rise Time	t_{PR}				250	ns
Fall Time	t_{PF}				50	ns
Phase Difference between Tx and Rx signals	t_{TRD1}	Fixed sampling mode	10.0		14.0	μs
	t_{TRD2}	Adaptive sampling mode	10.0		42.0	μs
Phase Difference between Rx signals	t_{PH1}	Fixed sampling mode			4.0	μs
	t_{PH2}	Adaptive sampling mode			2.0	μs
Delay across Tx and Rx slots	t_{FD}	Fixed sampling mode			4.4	μs

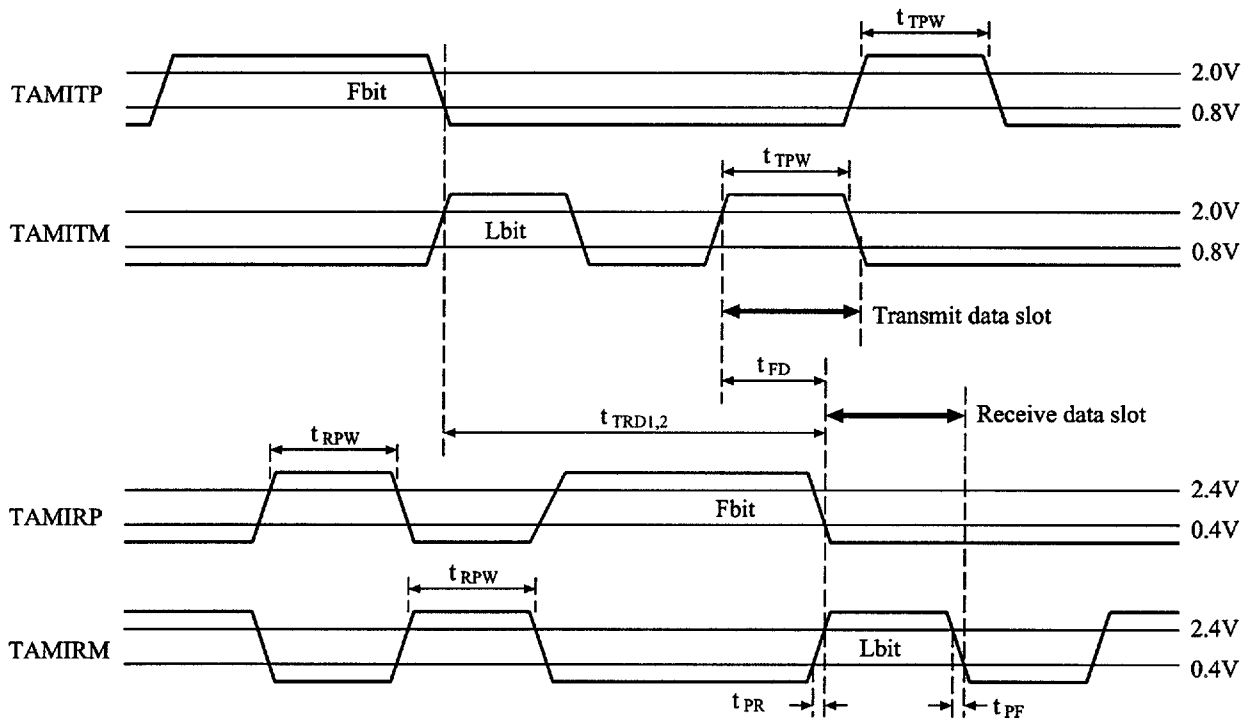


Figure 7.4: T Reference Point Interface

7.4.5 Clock

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
CLK192K Output Frequency	f_{CK192}	f_X=15.36MHz		192		kHz
CLK192K High-Level Period	t_{WCK192}	f_X=15.36MHz		2.604		μs
CLK400 Output Frequency	f_{CK400}	f_X=15.36MHz		400		Hz
CLK400 High-Level Period	t_{WCK400}	f_X=15.36MHz		3.125		μs

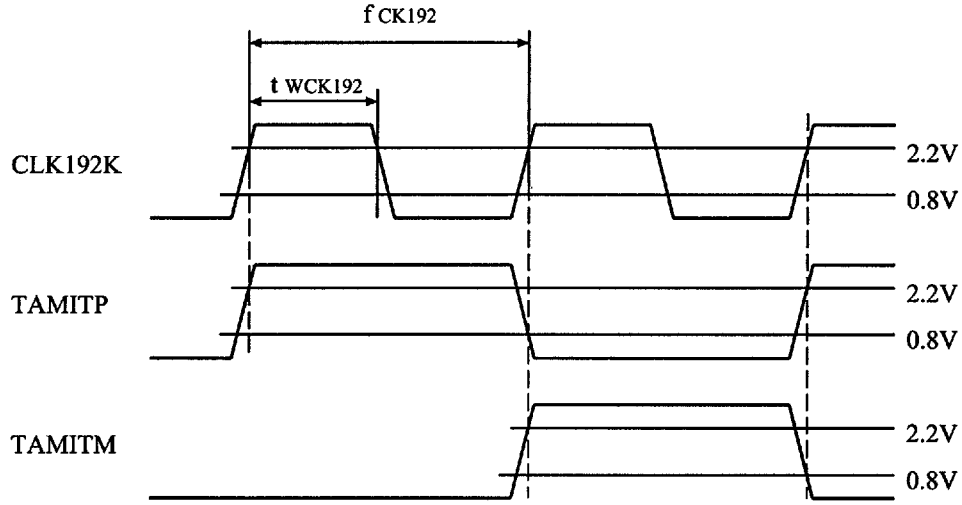


Figure 7.5: CLK192K Output

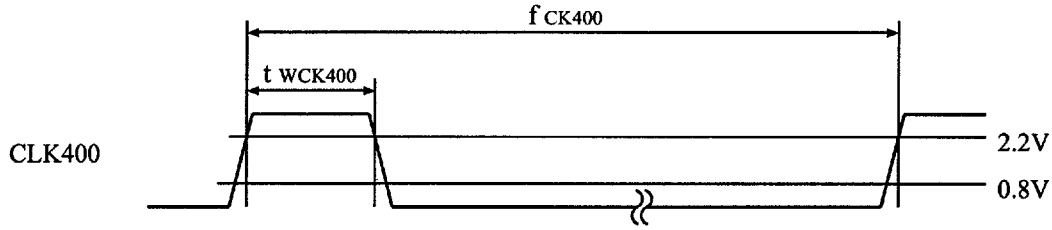
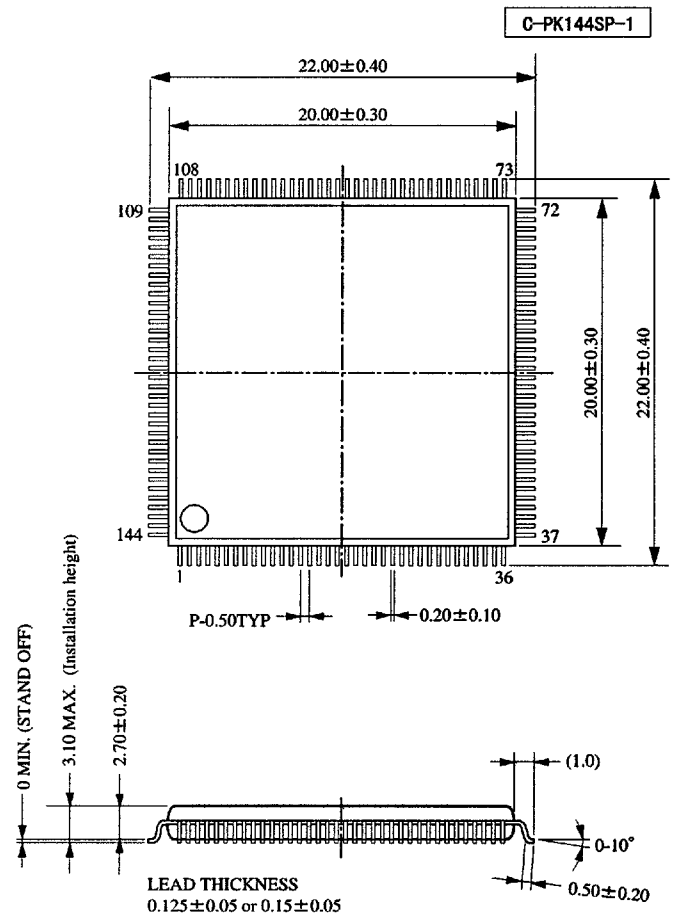


Figure 7.6: CLK400 Output

Chapter 8

PACKAGE OUTLINE



The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note : The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest Yamaha agent.

Appendix A

EXAMPLE OF APPLICATIONS

A.1 Example of Application Circuits

This circuit is an example of a configuration in which multiple YTD426B are mounted on the U reference point interface board. The master YTD426B is connected to YTD423B.

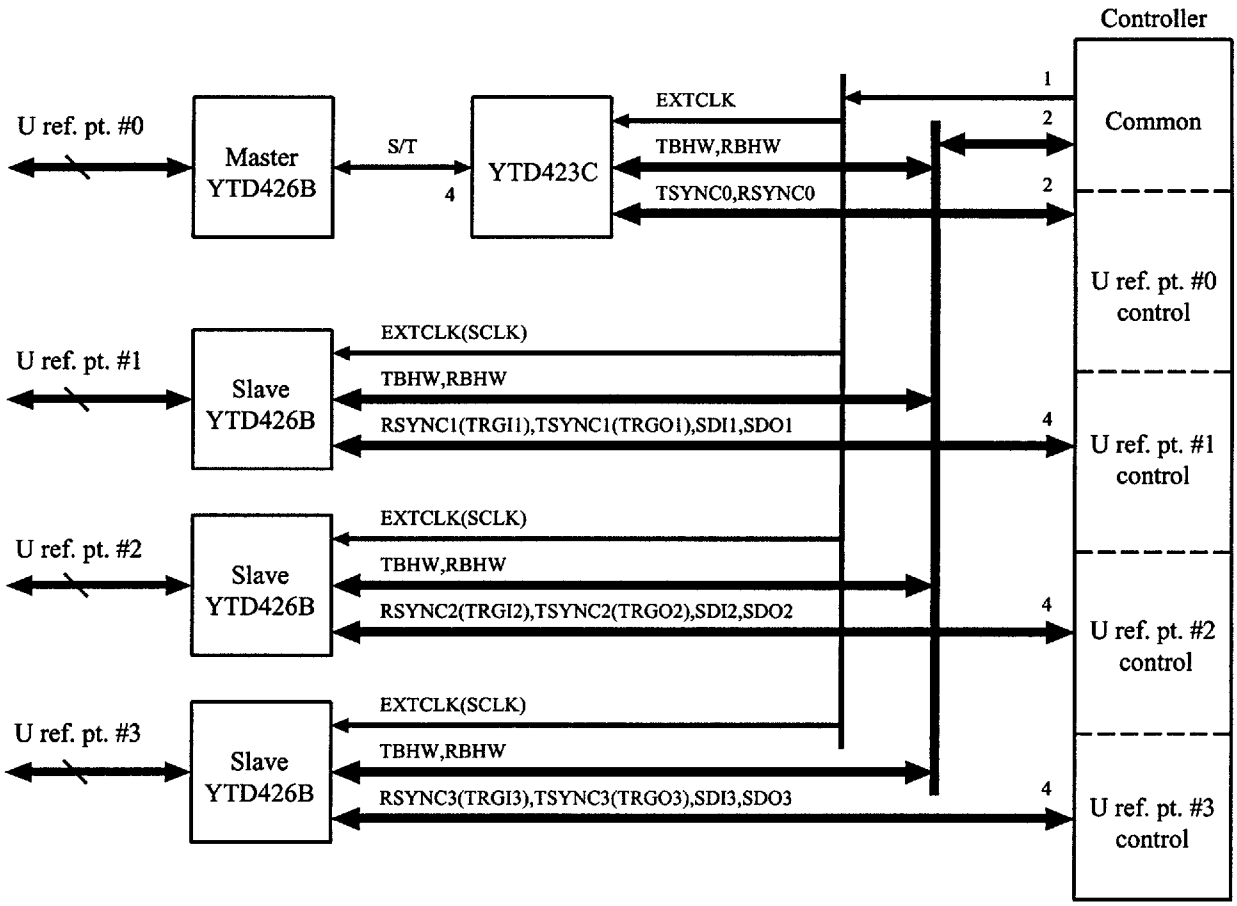


Figure A.1: U Reference Point Interface Board Block Diagram

- Connect YTD423B on the master side and control the D and B channels.
- The line on the slave side is controlled with Serial control.
- The B channel data is controlled by the time slot of the B channel interface (PCM highway).
- The B channel interface clock (EXTCLK) and the Serial control data clock (SCLK) are common clock.
- The signal for the serial control data (TRGO, TRGI) and the B channel data (TSYNC, RSYNC) are commonly triggered.

Signal lines for a 4B system

Function	No. of signal lines	Pins
T ref. pt. I/F	4	TAMIRP, TAMIRM, TAMITP, TAMITM
Timing signal	4	TSYNC0, RSYNC0, TSYNC1&TRGO1, RSYNC1&TRGI1
Serial control data	2	SDO1, SDI1
Bch data	2	TBHW, RBHW
Clock	1	EXTCLK&SCLK

Signal lines for a 8B system

Function	No. of signal lines	Pins
T ref. pt. I/F	4	TAMIRP, TAMIRM, TAMITP, TAMITM
Timing signal	8	TSYNC0, RSYNC0, TSYNC1&TRGO1, RSYNC1&TRGI1, TSYNC2&TRGO2, RSYNC2&TRGI2, TSYNC3&TRGO3, RSYNC3&TRGI3
Serial control data	6	SDO1, SDI1, SDO2, SDI2, SDO3, SDI3
Bch data	2	TBHW, RBHW
Clock	1	EXTCLK&SCLK

A.1.1 Example of A Slave Mode, Serial Control Circuit

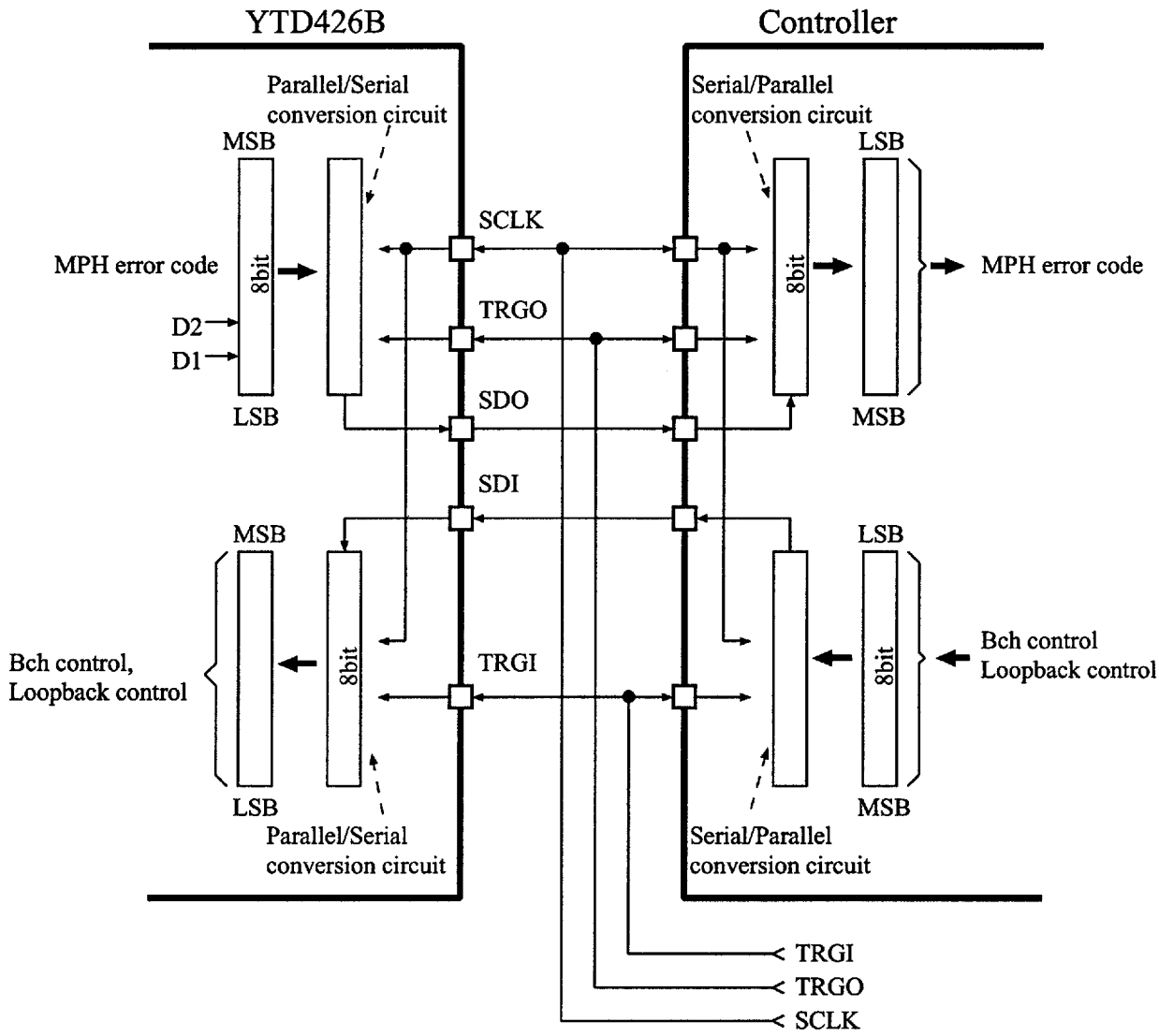


Figure A.2: Example of A Slave Mode, Serial Control Circuit

- Access to the slave side YTD426B
  - Inputs and outputs the Serial control data from and to the external controller through the SDI and SDO pins. These data are exchanged with 8 kHz cycle which is synchronized to the SCLK signal.
- Controller
  - Reads the MPH-DATA-INDICATION periodically or reads it using the interrupt signal that is generated when the state changes.
  - Updates YTD426B register settings as necessary.

Serial data timing

- 8-bit serial data synchronized to SCLK is transmitted following TRGO.
- 8-bit serial data synchronized to SCLK is acquired following TRGI.

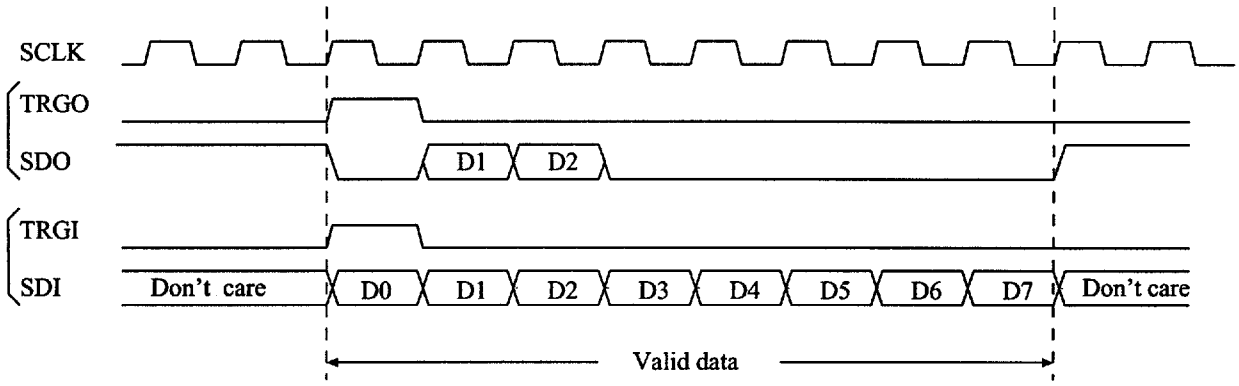


Figure A.3: Serial Data Timing

Slave mode activation procedure

1. NTACT pin

   - When YTD426B recognizes that the NTACT pin is "H", it activates the DSU and initiates the call originating process.

2. Activation procedure when call originating

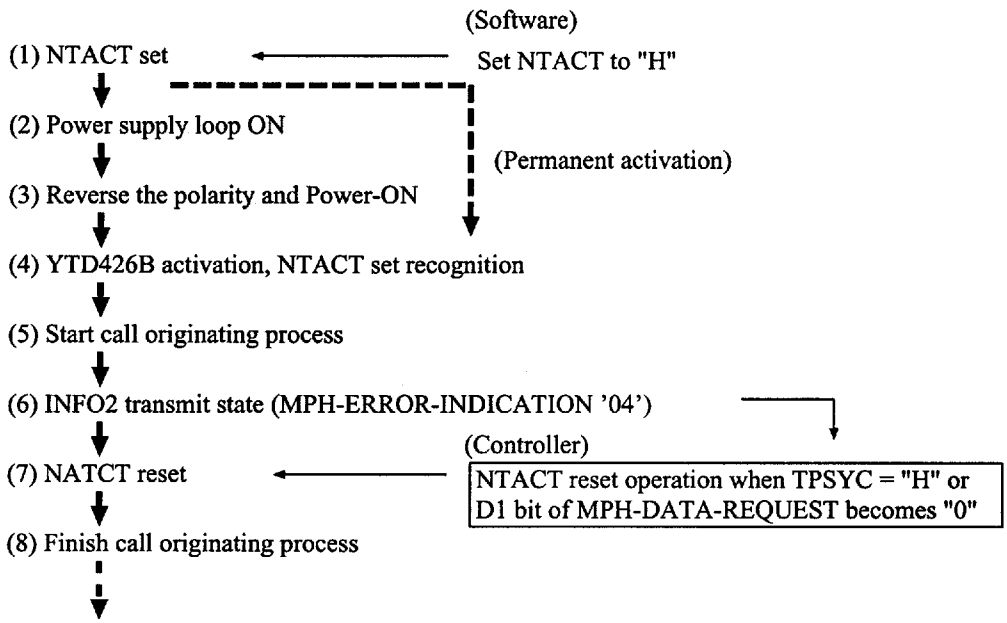


Figure A.4: DSU Activation Procedure

- Once the DSU is activated on a permanent activation setting, the state transits from step (1) to (4) directly for all subsequent procedures.
- Configure the controller so that it resets NTACT when synchronization is detected at the T reference point.

  Make reset signal either (1) when TPSYNC pin is "H" or (2) when D1 bit of MPH-DATA-INDICATION becomes "0".

Appendix B

REVISION HISTORY

- Modified contents from CATALOG No.LSI-5TD426B2 to LSI-5TD426B3
  - Modified description of TSMPSEL pin at 3.2.5 T Reference Point Option Setting.

Before Modification

Pin No.	Pin name	I/O	Function	Remarks
116	TSMPSEL	IN	Selects the receive data sampling timing at the T reference point. "L": Adaptive timing (point-to-point connection,long passive bus) "H": Fixed timing (short passive bus)	with pull-up resistor

After Modification

Pin No.	Pin name	I/O	Function	Remarks
116	TSMPSEL	IN	Selects the receive data sampling timing at the T reference point. "L": Adaptive timing "H": Fixed timing Usually fixed to "L".	with pull-up resistor

– Modified description of MULTI pin at 3.2.5 T Reference Point Option Setting.

Before Modification

Pin No.	Pin name	I/O	Function	Remarks
117	MULTI	IN	Sets the multiframe support on the T reference point side. "L": Do not support multiframe "H": Support multiframe	with pull-up resistor

After Modification

Pin No.	Pin name	I/O	Function	Remarks
117	MULTI	IN	Sets the multiframe support on the T reference point side. "L": Do not support multiframe (Use of the Qbit is impossible.) "H": Support multiframe (Use of the Qbit is possible.) Usually fixed to "H".	with pull-up resistor

– Modified description of TSMPAUT pin at 3.2.5 T Reference Point Option Setting.

Before Modification

Pin No.	Pin name	I/O	Function	Remarks
131	TSMPAUT	IN	Sets the sampling mode on the T reference point ‡. "L": Auto (TSMPSEL pin state is invalid) "H": Manual (TSMPSEL pin state is valid)	with pull-up resistor

After Modification

Pin No.	Pin name	I/O	Function	Remarks
131	TSMPAUT	IN	Usually fixed to "H".	with pull-up resistor

– Modified description of Note at 3.2.5 T Reference Point Option Setting.

Before Modification

† "positive polarity" means the condition that voltage level = "High" when logic = binary "0".

After Modification

† "positive polarity" means the condition that voltage level = "High" when logic = binary "0". (See 5.2 T Reference Point Interface)

– Deleted description of Note at 3.2.5 T Reference Point Option Setting

– Modified name from YTD423B to YTD423D.