



# STARTECH

An **EX4R** Company

# ST49C155

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## PREPROGRAMMED CPU MOTHERBOARD FREQUENCY GENERATOR

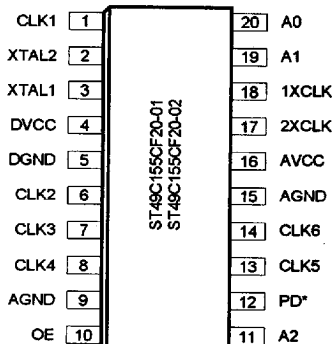
### GENERAL DESCRIPTION

The ST49C155 is a monolithic analog CMOS device designed to generate eight simultaneous clock outputs for mother board applications. It is designed in a 1.2 $\mu$  process to achieve 100 MHz operation with low clock jitter.

The ST49C155 may be used to replace existing BUS and I/O clocks generated from individual oscillators so that board space and number of oscillators are reduced. The high speed analog CMOS phase locked loops use the 14.318 MHz system clock or external crystal connected between XTAL1 and XTAL2 as the reference clock (reference clock can be changed to generate non-standard frequencies from the standard programmed device).

The ST49C155 is metal mask programmable to provide any custom set of CPUCLK frequencies. The programmed clock outputs are selectable via four address lines for 1XCLK / 2XCLK outputs.

### SOIC Package



### FEATURES

- Can replace multiple oscillators/crystals
- Pin-to-pin compatible to AV9155
- Compatible with 286, 386, and 486 CPUs
- Supports Turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Skew controlled 2X and 1X clocks
- Programmable analog phase locked loop
- High speed (up to 100 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip or SOIC package

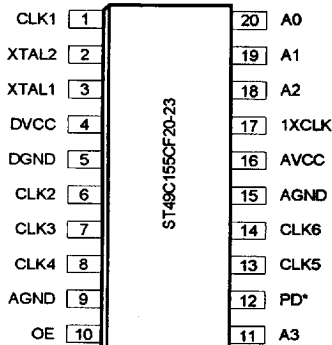
### ORDERING INFORMATION

| Part number     | Package     | Operating temperature |
|-----------------|-------------|-----------------------|
| ST49C155CP20-xx | Plastic-DIP | 0° C to +70° C        |
| ST49C155CF20-xx | SOIC        | 0° C to +70° C        |
| ST49C155CJ20-xx | PLCC        | 0° C to +70° C        |

Rev. 1.0

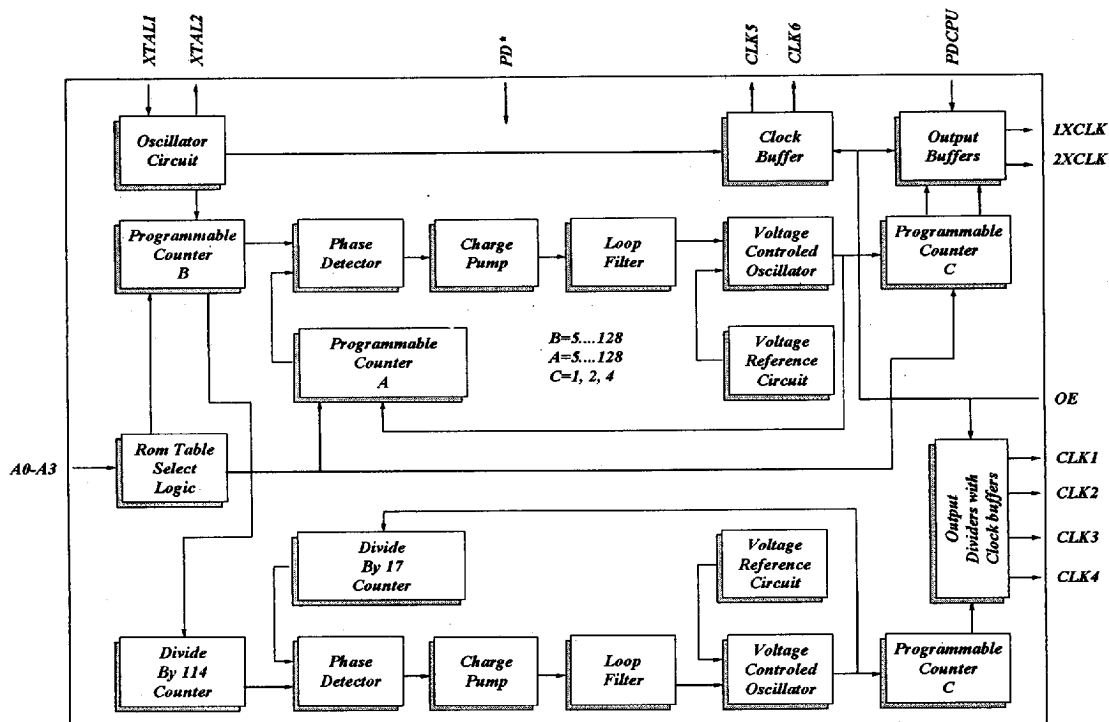
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# ST49C155

## BLOCK DIAGRAM



## SYMBOL DESCRIPTION ( ST49C155-01/ -02)

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| Symbol | Pin | Signal Type | Pin Description                                                                        |
|--------|-----|-------------|----------------------------------------------------------------------------------------|
| CLK1   | 1   | O           | 1.8432 MHz clock output.                                                               |
| XTAL2  | 2   | O           | Crystal output.                                                                        |
| XTAL1  | 3   | I           | Crystal or External clock input.                                                       |
| DVCC   | 4   | I           | Digital supply voltage. Single +5 volts.                                               |
| DGND   | 5   | O           | Digital signal ground.                                                                 |
| CLK2   | 6   | O           | 16 MHz ( ST49C155-01 ) or 32 MHz ( ST49C155-02 ) clock output.                         |
| CLK3   | 7   | O           | 24 MHz floppy disk clock output.                                                       |
| CLK4   | 8   | O           | 12 MHz keyboard clock output.                                                          |
| AGND   | 9   | O           | Analog ground.                                                                         |
| OE     | 10* | O           | Output Enable (active high). Low on this pin sets all the outputs to three state mode. |
| A2     | 11  | I           | CPU clock frequency select address 2.                                                  |
| PD*    | 12* | I           | Power down ( active low ). Shuts off entire chip when low.                             |
| CLK5   | 13  | O           | 14.318 MHz reference clock output.                                                     |
| CLK6   | 14  | O           | 14.318 MHz reference clock output.                                                     |
| AGND   | 15  | O           | Analog ground.                                                                         |
| AVCC   | 16  | I           | Analog supply voltage. Single +5 volts.                                                |
| 2XCLK  | 17  | I           | 2X CPU clock output.                                                                   |
| 1XCLK  | 18  | I           | 1X CPU clock output.                                                                   |
| A1     | 19  | I           | CPU clock frequency select address 1.                                                  |
| A0     | 20  | I           | CPU clock frequency select address 0.                                                  |

\*Have internal pull-up resistor on inputs

# ST49C155

## SYMBOL DESCRIPTION ( ST49C155-03)

| Symbol | Pin | Signal Type | Pin Description                                                                        |
|--------|-----|-------------|----------------------------------------------------------------------------------------|
| CLK1   | 1   | O           | 6 MHz clock output.                                                                    |
| XTAL2  | 2   | O           | Crystal output.                                                                        |
| XTAL1  | 3   | I           | Crystal or External clock input.                                                       |
| DVCC   | 4   | I           | Digital supply voltage. Single +5 volts.                                               |
| DGND   | 5   | O           | Digital signal ground.                                                                 |
| CLK2   | 6   | O           | 24 MHz floppy disk clock output.                                                       |
| CLK3   | 7   | O           | 16 MHz bus clock output.                                                               |
| CLK4   | 8   | O           | 8 MHz keyboard clock output.                                                           |
| AGND   | 9   | O           | Analog ground.                                                                         |
| OE     | 10* | O           | Output Enable (active high). Low on this pin sets all the outputs to three state mode. |
| A3     | 11  | I           | CPU clock frequency select address 3.                                                  |
| PD*    | 12* | I           | Power down ( active low ). Shuts off entire chip when low.                             |
| CLK5   | 13  | O           | 14.318 MHz reference clock output.                                                     |
| CLK6   | 14  | O           | 14.318 MHz reference clock output.                                                     |
| AGND   | 15  | O           | Analog signal ground.                                                                  |
| AVCC   | 16  | I           | Analog supply voltage. Single +5 volts.                                                |
| 1XCLK  | 17  | I           | CPU clock output.                                                                      |
| A2     | 18  | I           | CPU clock frequency select address 2.                                                  |
| A1     | 19  | I           | CPU clock frequency select address 1.                                                  |
| A0     | 20  | I           | CPU clock frequency select address 0.                                                  |

\*Have internal pull-up resistor on inputs

**CPU CLOCK TABLE FOR ST49C155-01, -02 (using 14.318 MHz input. All frequencies in MHz).**

| A2 A1 A0 | 2XCLK | 1XCLK |
|----------|-------|-------|
| 0 0 0    | 8     | 4     |
| 0 0 1    | 16    | 8     |
| 0 1 0    | 32    | 16    |
| 0 1 1    | 40    | 20    |
| 1 0 0    | 50    | 25    |
| 1 0 1    | 66.66 | 33.33 |
| 1 1 0    | 80    | 40    |
| 1 1 1    | 100   | 50    |

**ST49C155-23 (using 14.318 MHz input. All frequencies in MHz).**

| A2 A1 A0 | 2XCLK | 1XCLK |
|----------|-------|-------|
| 0 0 0    | 75    | 37.5  |
| 0 0 1    | 32    | 16    |
| 0 1 0    | 60    | 30    |
| 0 1 1    | 40    | 20    |
| 1 0 0    | 50    | 25    |
| 1 0 1    | 66.66 | 33.33 |
| 1 1 0    | 80    | 40    |
| 1 1 1    | 52    | 26    |

**ST49C155-03 (using 14.318 MHz input. All frequencies in MHz).**

**PERIPHERAL CLOCK TABLE FOR ST49C155-01**

| CLK1   | CLK2 | CLK3 | CLK4 |
|--------|------|------|------|
| 1.8432 | 16   | 24   | 12   |

**PERIPHERAL CLOCK TABLE FOR ST49C155-02**

| CLK1   | CLK2 | CLK3 | CLK4 |
|--------|------|------|------|
| 1.8432 | 32   | 24   | 12   |

**PERIPHERAL CLOCK TABLE FOR ST49C155-03**

| CLK1 | CLK2 | CLK3 | CLK4 |
|------|------|------|------|
| 6    | 24   | 16   | 8    |

**PERIPHERAL CLOCK TABLE FOR ST49C155-23**

| CLK1  | CLK2 | CLK3 | CLK4 |
|-------|------|------|------|
| 1.843 | 16   | 24   | 12   |

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## ACTUAL OUTPUT FREQUENCIES

### CPU CLOCK TABLE FOR ST49C155-01, -02

| A2 A1 A0 | 2XCLK  | 1XCLK |
|----------|--------|-------|
| 0 0 0    | 7.5    | 3.75  |
| 0 0 1    | 15.51  | 7.76  |
| 0 1 0    | 32.22  | 16.11 |
| 0 1 1    | 40.09  | 20.05 |
| 1 0 0    | 50.11  | 25.06 |
| 1 0 1    | 66.82  | 33.41 |
| 1 1 0    | 80.18  | 40.09 |
| 1 1 1    | 100.23 | 50.11 |

### CPU CLOCK TABLE FOR ST49C155-03

| A3 A2 A1 A0 | 1XCLK  |
|-------------|--------|
| 0 0 0 0     | 15.51  |
| 0 0 0 1     | 40.09  |
| 0 0 1 0     | 50.11  |
| 0 0 1 1     | 80.18  |
| 0 1 0 0     | 66.82  |
| 0 1 0 1     | 100.23 |
| 0 1 1 0     | 7.58   |
| 0 1 1 1     | 4.30   |
| 1 0 0 0     | 7.76   |
| 1 0 0 1     | 20.05  |
| 1 0 1 0     | 25.06  |
| 1 0 1 1     | 40.09  |
| 1 1 0 0     | 33.41  |
| 1 1 0 1     | 50.11  |
| 1 1 1 0     | 3.79   |
| 1 1 1 1     | 2.15   |

### CPU CLOCK TABLE FOR ST49C155-23

| A2 A1 A0 | 2XCLK  | 1XCLK  |
|----------|--------|--------|
| 0 0 0    | 75.170 | 37.585 |
| 0 0 1    | 31.940 | 15.970 |
| 0 1 0    | 60.136 | 30.068 |
| 0 1 1    | 40.090 | 20.045 |
| 1 0 0    | 50.113 | 25.057 |
| 1 0 1    | 66.476 | 33.238 |
| 1 1 0    | 80.181 | 40.091 |
| 1 1 1    | 51.903 | 25.952 |

### PERIPHERAL CLOCK TABLE FOR ST49C155-01

| CLK1   | CLK2 | CLK3  | CLK4  |
|--------|------|-------|-------|
| 1.8432 | 16   | 23.71 | 11.86 |

### PERIPHERAL CLOCK TABLE FOR ST49C155-02

| CLK1   | CLK2  | CLK3 | CLK4 |
|--------|-------|------|------|
| 1.8432 | 32.01 | 24   | 12   |

### PERIPHERAL CLOCK TABLE FOR ST49C155-03

| CLK1 | CLK2 | CLK3 | CLK4 |
|------|------|------|------|
| 6    | 24   | 16   | 8    |

### PERIPHERAL CLOCK TABLE FOR ST49C155-23

| CLK1  | CLK2 | CLK3 | CLK4 |
|-------|------|------|------|
| 1.843 | 16   | 24   | 12   |

## ABSOLUTE MAXIMUM RATINGS

|                       |                        |
|-----------------------|------------------------|
| Supply voltage        | 7 Volts                |
| Voltage at any pin    | GND-0.3 V to VCC+0.3 V |
| Operating temperature | 0° C to +70° C         |
| Storage temperature   | -40° C to +150° C      |
| Package dissipation   | 500 mW                 |

## DC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ - 70^\circ \text{ C}$ ,  $V_{CC} = 5.0 \text{ V} \pm 10\%$  unless otherwise specified.

| Symbol   | Parameter                   | Limits |     |     | Units      | Conditions                                                                      |
|----------|-----------------------------|--------|-----|-----|------------|---------------------------------------------------------------------------------|
|          |                             | Min    | Typ | Max |            |                                                                                 |
| $V_{IL}$ | Input low level             |        |     | 0.8 | V          |                                                                                 |
| $V_{IH}$ | Input high level            | 2.0    |     |     | V          |                                                                                 |
| $V_{OL}$ | Output low level            |        |     | 0.4 | V          |                                                                                 |
| $V_{OH}$ | Output high level           | 2.4    |     |     | V          |                                                                                 |
| $I_{IL}$ | Input low current           |        |     | -1  | mA         | $I_{OL} = 8.0 \text{ mA}$<br>$I_{OH} = 8.0 \text{ mA}$<br>Except pins 2, 10, 12 |
| $I_{IH}$ | Input high current          |        |     | 1   | mA         | $V_{IN} = V_{CC}$                                                               |
| $I_{CC}$ | Operating current           |        | 45  | 65  | mA         | No load.                                                                        |
| $R_{IN}$ | Internal pull-up resistance |        | 680 |     | k $\Omega$ | Pins 10, 12                                                                     |

## FREQUENCY TRANSITIONS

The ST49C155 is designed to provide smooth, glitch-free frequency transitions on the 1XCLK and 2XCLK clocks when the frequency select pins are changed. These frequency transitions are less than 0.1% frequency change per clock period.

# ST49C155

## AC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ - 70^\circ \text{ C}$ ,  $V_{CC} = 5.0 \text{ V} \pm 10\%$  unless otherwise specified.

| Symbol   | Parameter             | Limits |           |         | Units | Conditions              |
|----------|-----------------------|--------|-----------|---------|-------|-------------------------|
|          |                       | Min    | Typ       | Max     |       |                         |
| $T_4$    | Rise time             |        | 1         | 2       | ns    | 0.8V - 2.0V, 15pF       |
| $T_5$    | Fall time             |        | 1         | 2       | ns    | 2.0V - 0.8V, 15pF       |
| $T_6$    | Duty cycle            | 40     | 48/52     | 60      | %     | 1.4V switch point       |
| $T_6$    | Duty cycle            | 40     | 48/52     | 55      | %     | $V_{CC}/2$ switch point |
| $T_7$    | Jitter 1 sigma        |        | $\pm 0.5$ | $\pm 2$ | %     |                         |
| $T_7$    | Jitter absolute       |        | $\pm 2$   | $\pm 5$ | %     |                         |
| $T_8$    | Input frequency       |        | 14.318    |         | MHz   |                         |
| $T_9$    | Input clock rise time |        |           | 20      | ns    |                         |
| $T_{10}$ | Input clock fall time |        |           | 20      | ns    |                         |

## TIMING DIAGRAM

