YAMAHA LSI

YTM411B

MD9624LV

FAX/DATA/VOICE MODEM LSI

■ OUTLINE

The YTM411B is a one-chip MODEM LSI applicable to both the FAX MODEM and Data MODEM and requires low power as it can be operated with a power supply in the range: 3.3 ~ 5V.

The YTM411B is an upper-level chip of YAMAHA's FAX/DATA MODEM LSI YTM403C and has upper interchangeability in terms of software (interface register).

In applications as a FAX MODEM, the YTM411B incorporates a 9600/7200/4800/2400/300bps synchronous half-duplex (ITU-T (former CCITT) V.29, V.27ter, V.21ch2) data pumping function in and is an optimal G3 facsimile MODEM.

In applications as a data MODEM, the YTM411B is equipped with a 2400/1200/600/300bps asynchronous full-duplex (ITU-T V.22bis, V.22, V.21, BELL212A, 103) data pumping function and is an optimal data communication MODEM for personal computer communication and database retrieval.

In addition to the data pumping functions mentioned above, the YTM411B is also equipped with a USART function, which is generally considered indispensable for ECM (error correction mode) compatible G3 facsimile and data communication and is independently capable of HDLC framing and start-stop synchronous processing. It also makes a speech recording and reproducing function (voice function) available in the telephone circuit when the built-in ADC and DAC are accessed from the outside. It also incorporates A-law, μ-law in addition to ADPCM as a voice data compressing/expanding function and can deal with four kinds of sampling frequency.

The functions of the YTM411B are controlled by external microprocessors, which are not restricted but are selectable in accordance with external terminals.

■ FEATURES

- ☐ Single power source operation over 3.3V to 5V range
- ☐ Low power consumption
- ☐ Software (interface register) compatible with the YTM403C (YAMAHA FAX/DATA MODEM
- ☐ LSI)

  Communication compatibility
  - •ITU-T V.29/V.27ter/V.26bis/V.23/V.22bis/V22(A/B)/V.21
- ☐ •BELL 212A/202/103

  Communication speed
  - •Synchronous half-duplex communication: 9600/7200/4800/2400/1200/300bps
  - •Asynchronous full-duplex communication: 2400/1200/600/300bps
  - •Modified full-duplex communication: 4800(150/75) / 2400(150/75) /1200(150/75)/600 (150/75)

YAMAHA CORPORATION

YTM411B CATALOG
CATALOG No.: LSI-4TM411B2
1995. 2

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- ☐ Built-in VOICE function (voice recording and reproduction)
  - •Sampling frequency: 11025/9600/8000/7200Hz
  - •16-bit (max.) PCM
  - •Data compression and expansion function: ADPCM (3 or 4 bit), A-law, μ -law
  - •Silence detection, compression and insertion function
- ☐ Built-in scrambler/descrambler: V.29/V.27ter/V.22bis/V.22/BELL212A
- ☐ Built-in training sequencer: V.29/V.27ter
- ☐ Built-in handshake sequencer: V.22bis/V.22/BELL212A
- ☐ Built-in asynchronous/synchronous and synchronous/asynchronous conversion function
  - •ITU-T V.22bis/V.22 compatibility
  - •BELL212A compatibility
  - •Character length: 8, 9, 10, and 11 bits
- ☐ Built-in equalizer function
  - •Sending subscriber cable equalizer (3 types)
  - •Receiving subscriber cable equalizer (3 types)
  - •Adaptive automatic equalizer
- ☐ DTE interface
  - •Serial interface (ITU-T V.24)
  - •Parallel interface (microprocessor bus)
  - •Built-in USART function (processing HDLC framing, start-stop framing)
- ☐ Built-in programmable tone generating function
  - •Simultaneous 4-tone generation capability
  - •Programmable frequency and level
  - •Useful for sending guard tone, call progress tone and DTMF tone
- ☐ Built-in programmable tone detection function
  - •Programmable center frequency, bandwidth and level (3 channels)
  - •Allows call progress tone and DTMF tone detection
- ☐ Built-in guard tone notch filter: V.22bis/V.22
- ☐ Built-in training signal detection function: V.29/V.27ter
- ☐ Built-in S1 signal sending/detection function: V.22bis
- ☐ Built-in V.21ch2 flag sequence detection function
- ☐ Transmission clock selection capability: Internal clock/external clock/slave clock
- ☐ Reception dynamic range : operated in 3.3V -4 ~ -50 dBm / 5V 0 ~ -50 dBm
- ☐ Carrier detection level control
- ☐ Built-in AGC (Mode control)
- ☐ Sending level control: operated in 3.3V -10 ~ -∞dBm / 5V -6 ~ -∞dBm
- ☐ Built-in transmit/receive bandpass filter
- ☐ Built-in ADC/DAC: External control
- ☐ Eye pattern output
- ☐ Built-in loopback connection function
  - •Remote digital loopback
  - •Local digital loopback
  - •Local analog loopback
- ☐ General purpose I/O port: for NCU control
- ☐ Power down mode
- ☐ Package: 64-pin QFP/64-pin TQFP

■ ITEMS DIFFERENCES FROM YTM403C

(When using the YTM411B instead of the YTM403C, be sure to read this chapter)

☐ New Hardware Items

The YTM411B can be operated in the power supply range of 3.3~5V in contrast to 5V for the YTM403C.

Instead of two pins PI4 and PO4 of the YTM403C, the YTM411B has the following new pins:

CS2 pin: 2 chip select inputs
Another chip select input was newly added. If a decoding circuit is composed by also using the existing /CS1 pin, the external circuits can be reduced.
CS2 pin is positive logic and must be HIGH to enable the YTM411B to input/output data. Thus, be well aware that the chip select method differs between YTM411B and YTM403C.

/CSOUT pin: chip select output
When the YTM411B is chip-selected, the /CSOUT pin terminal is set to LOW. The position of this terminal enables the microprocessor to recognize whether or not the YTM411B has made the data bus input/output valid.

☐ New Items in Software

The voice function was enhanced and a mode was added. In addition to the method with voice data access in the built-in RAM interchangeable in terms of operability and data with the YTM403C, a method using voice data access in the interface register was added. A compression/expansion system, in 3, 4-bit ADPCM, 8-bit A-law, μ-law, in addition to 16-bit PCM, is available, which makes sampling rate conversion and silence functions effective. Again, a 64-word transmission/reception buffer can be used, permitting the load on the microprocessor to be reduced.

On the YTM411B, COL1-4bits and ROW1-4bits used for DTMF detection etc. on the YTM403C were assigned for DTMF detection only, with these detecting frequencies and band widths fixed. The operable mode is the voice mode (except partly), which permits simultaneous DTMF detection and transmission either during voice recording or during voice reproduction.

On the YTM411B, during V.26bis transmission/reception, scrambler/descrambler functions used for V.27ter are effective in the default state. The timing of the transmission and reception signals here can be changed by setting the parameters of the built-in RAM, and the scrambler/descrambler functions themselves can be nullified, like other modes, by setting the SDIS and DDIS bits.

The YTM411B has the following two operating modes added:

Sleep mode
In this mode there is no transmission or reception operation. It can be set by writing FFh in the configuration register.

1200bps of BELL202
On the YTM403C, BELL202 mode can be set by first setting the B202 bit to "1" and then writing 21h in the configuration register. On the YTM411B, added is another method which writes 25h in the configuration register.

The YTM411B has, added to the interface register of the YTM403C, the following 6 bits:

PLAY (voice reproduction control bit)
In the voice mode with data access in the interface register, the voice data are reproduced by setting the PLAY bit to "1" and the standby state is brought about by setting the bit to "0".

REC (voice recording control bit)
In the voice mode with data access in the interface register, the voice data are recorded by setting the REC bit to "1" and the standby state is brought about by setting the REC to "0".

TXBE (voice reproduction data byte order shift control bit)
In the voice mode with data access in the interface register, TXBE is used to shift the byte order of the voice data to be reproduced. To write the upper byte first, set this bit to "1" and to write the lower byte first, set the bit to "0".

RXBE (voice recording data byte order shift control bit)
In the voice mode with data access in the interface register, the RXBE is used to shift the byte order of the voice data to be recorded. To read the upper byte first, set this bit to "1" and to read the lower byte first, set the bit to "0".

AUDIO2 is for selecting monitor output or transmit
signal output (same as for TXO terminal). Setting this bit to "1" sets the AUDIO terminal to transmission/reception signal output.

AGC4 ("GAIN CONTROL" control bit)
If AGC4 is set to "1", GC3 bit control is possible. If AGC4 is set to "0", the YTM411B itself controls GC3 bit during V.29, V.27ter reception.

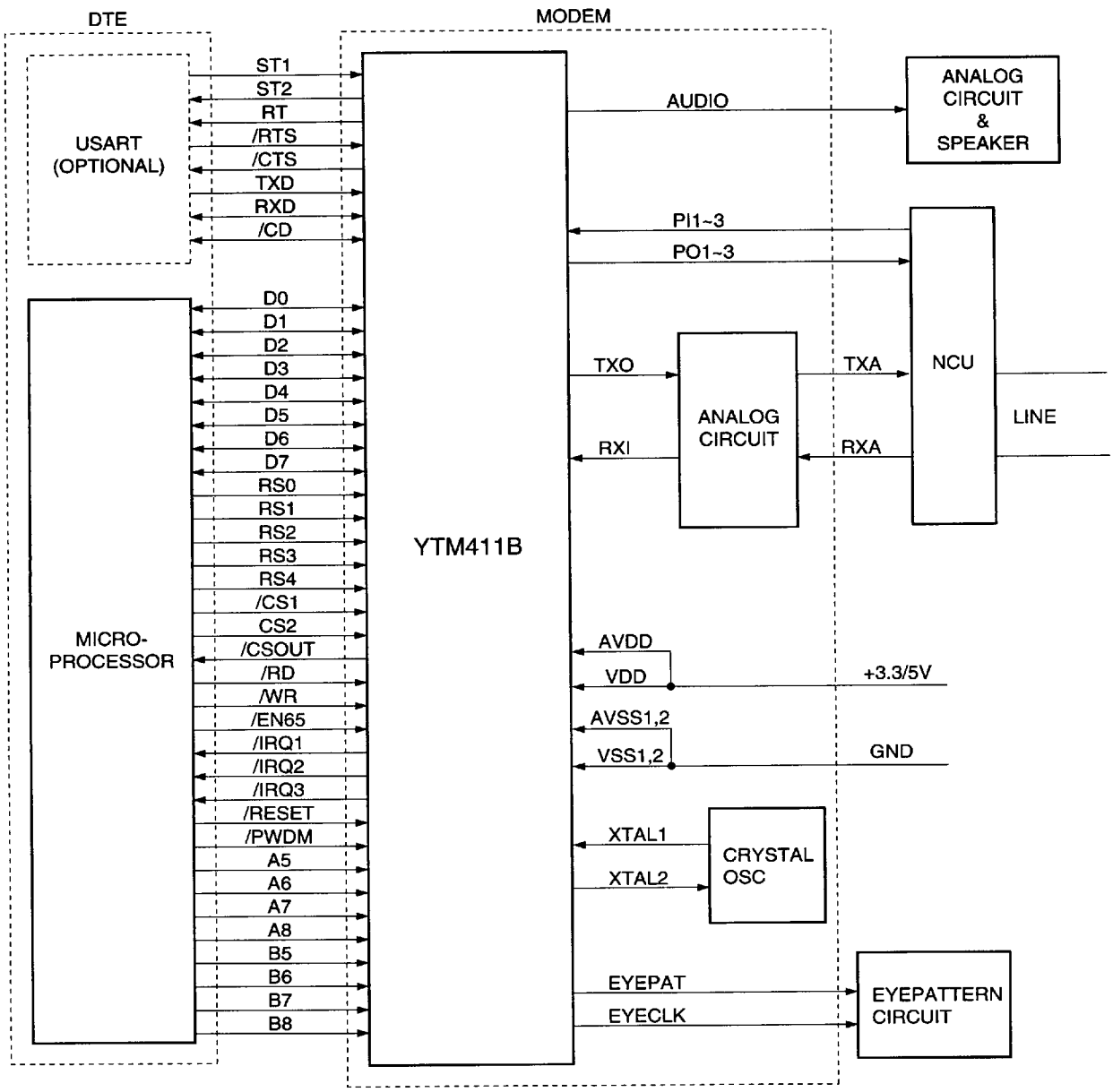
New functions are added to the following interface registers of the YTM403C.

CDET (silence detection status bit)
In the voice mode with data access in the interface register, if any silent part is detected in the voice data during recording, CDET turns to "0".

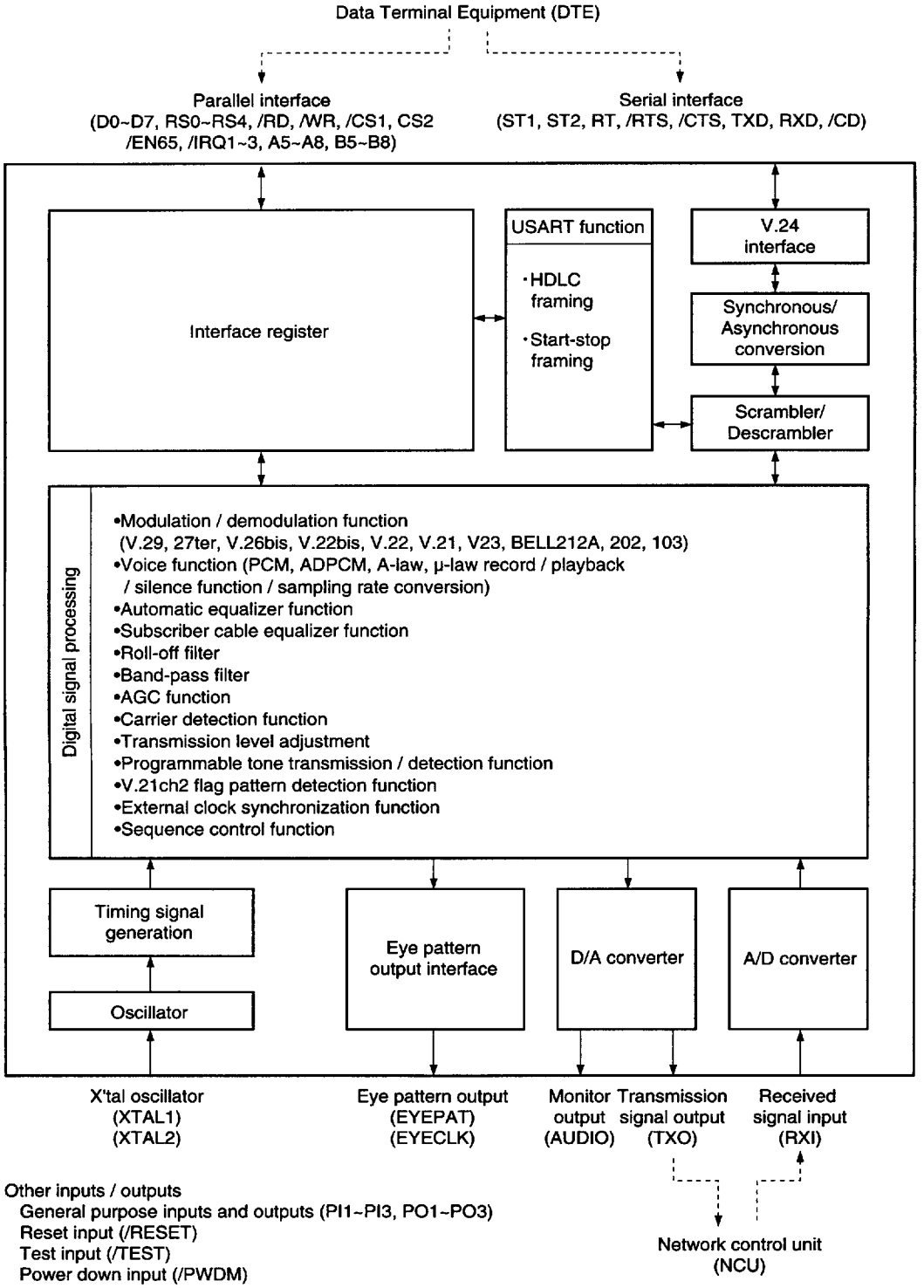
TXD8 (voice reproduction data access status bit)
In the voice mode with data access in the interface register, if TXD8 is "1" during reproduction, the upper byte of the reproduction data is written in the TXDATA register and if TXD8 is "0", the lower byte is written likewise.

RXD8 (voice recording data access status bit)
In voice mode with data access in the interface register, if RXD8 is "1" during recording, the value of RXDATA denotes the upper byte of the recording data and if RXD8 is "0", the same value denotes the lower byte.

■ SYSTEM BLOCK DIAGRAM



■ INTERNAL BLOCK DIAGRAM



OPERATION MODE AND COMMUNICATION PROTOCOL

The YTM411B has the following operating mode:

- ☐ 9600 bps half-duplex communication: V.29
- ☐ 7200 bps half-duplex communication: V.29
- ☐ 4800 bps half-duplex communication: V.29 / V.27ter
- ☐ 2400 bps half-duplex communication: V.27ter / V.26bis
- ☐ 1200 bps half-duplex communication: V.26bis / V.23 / BELL202
- ☐ 600 bps half-duplex communication: V.23
- ☐ 300 bps half-duplex communication: V.21ch2
- ☐ 75 bps half-duplex communication: V.23 / V.26bis / V.27ter
- ☐ 150 bps half-duplex communication: V.23 / V.26bis / V.27ter

(150 bps is outside the scope of ITU-T recommendation)

- ☐ 2400 bps full-duplex communication: V.22bis
- ☐ 1400 bps full-duplex communication: V.22(A,B) / BELL212A
- ☐ 600 bps full-duplex communication: V.22(A,B)
- ☐ 300 bps full-duplex communication: V.21 / BELL103

- ☐ PCM (VOICE) record and playback: 16-bits resolution
- ☐ ADPCM record and playback: YAMAHA 16-bits to 4-bits compression

Table 1 shows the communication protocol specifications applicable to the YTM411B.

Table 1 Communication protocols

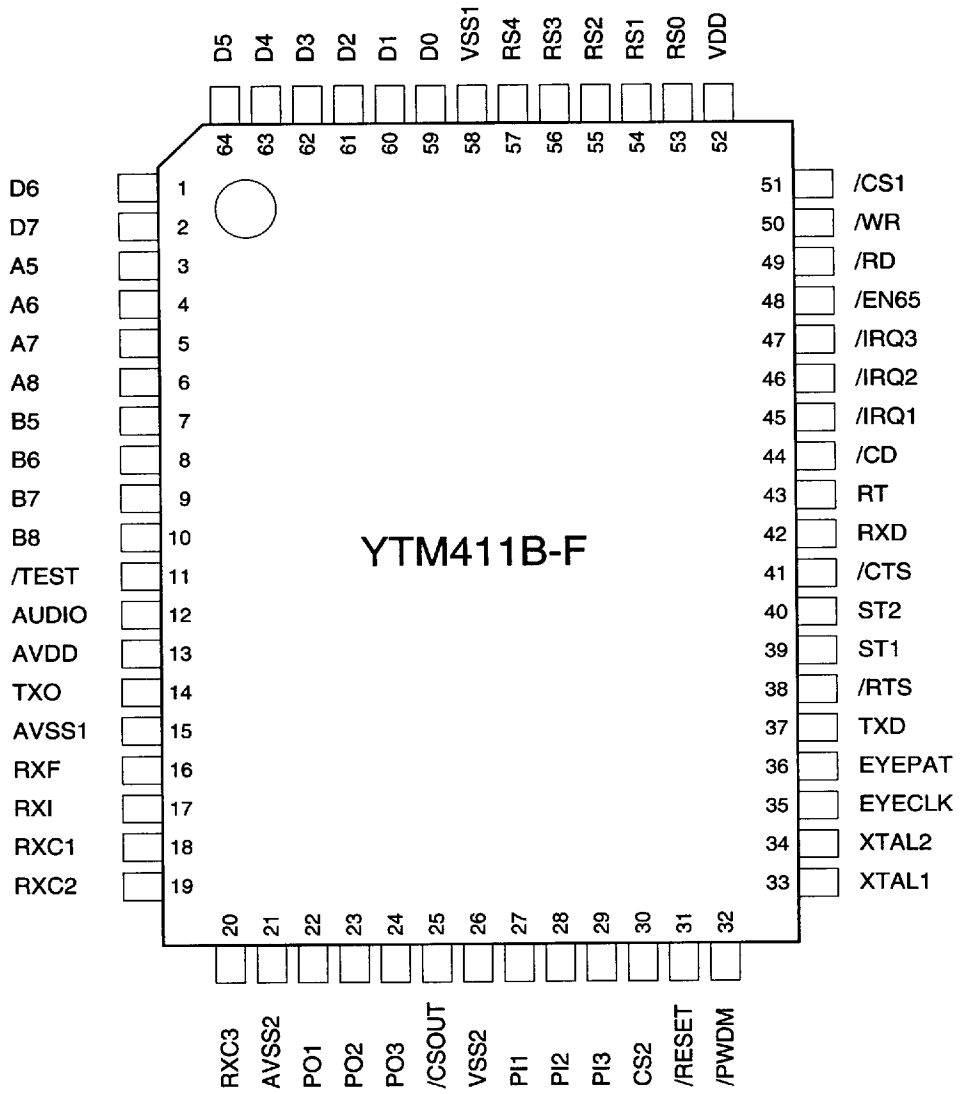
Communication protocol		Transmission speed (bps)	Modulation speed (Baud)	Carrier frequency (Hz)	Modulation method	Communication method
CCITT V.29		9600	2400	1700	16-QAM	Half-duplex (two-wire) Synchronous
		7200	2400	1700	8-QAM	
		4800	2400	1700	4-QAM	
CCITT V.27ter		4800	1600	1800	8-PSK	
		2400	1200	1800	4-PSK	
CCITT V.26bis		2400	1200	1800	4-PSK	
		1200	1200	1800	2-PSK	
CCITT V.23		1200	1200	Space 2100 Mark 1300	FSK	Half-duplex (two-wire)
		600	600	Space 1700 Mark 1300	FSK	
		150	150	Space 450 Mark 390	FSK	Half-duplex (two-wire) Backward
		75	75	Space 450 Mark 390	FSK	
BELL 202		1200	1200	Space 2200 Mark 1200	FSK	Half-duplex (two-wire)
CCITT V.22bis		2400	600	Low ch 1200 High ch 2400	16-QAM	Full-duplex (two-wire)
CCITT V.22		1200	600	Low ch 1200 High ch 2400	4-QAM	
		600	600	Low ch 1200 High ch 2400	2-QAM	
CCITT V.21	ch1	300	300	Space 1180 Mark 980	FSK	
	ch2	300	300	Space 1850 Mark 1650	FSK	
BELL 212A		1200	600	Low ch 1200 High ch 2400	4-QAM	
BELL 103	ch1	300	300	Space 1070 Mark 1270	FSK	
	ch2	300	300	Space 2025 Mark 2225	FSK	

*:150 bps is outside the scope of ITU-T recommendation

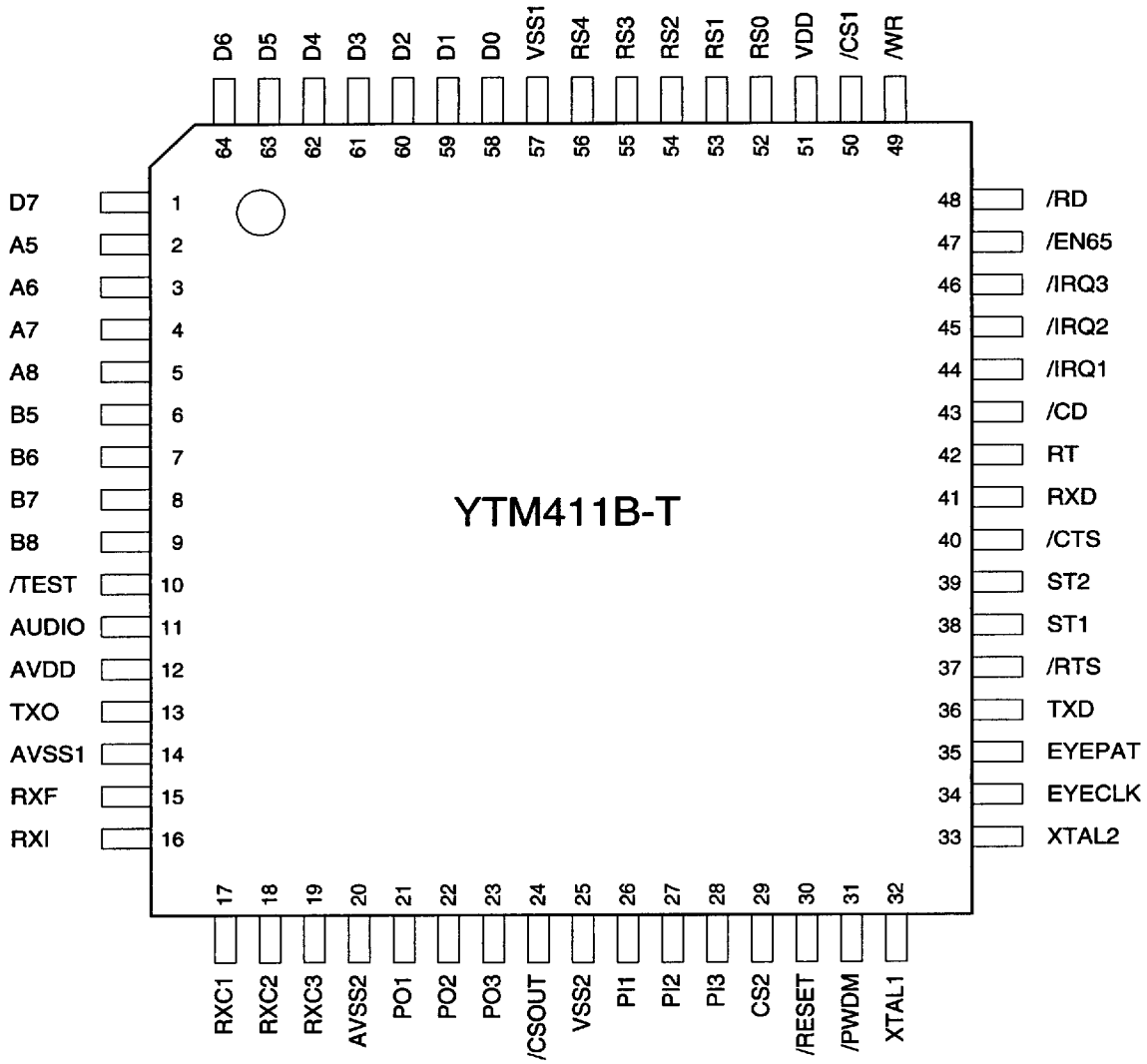
■ DESCRIPTION OF PINS

Pin Configuration

(1) 64-pin QFP



(2) 64-pin TQFP



■ Function Assignment to Pins

Pin name	Pin No.		TYPE	Function
	QFP	TQFP		
RS0 ~ RS4	53 ~ 57	52 ~ 56	DI	Interface register select input (5 bits)
A5 ~ A8,	3 ~ 6,	2 ~ 5,	DIO	Address decoder input/test input/output
B5 ~ B8	7 ~ 10	6 ~ 9		(When the A and B inputs are the same and pin CS1 is LOW and CS2 is HIGH, the register can be accessed.)
D0 ~ D7	59 ~ 64, 1,2	58 ~ 64, 1	DIO	Data bus (8 bits)
/EN65	48	47	DI	Microprocessor select input (LOW: 6502 type ,HIGH: 80 type)
/RD	49	48	DI	(/EN65: HIGH) Register read strobe input (/EN65: LOW) Strobe pulse input
/WR	50	49	DI	(/EN65: HIGH) Register write strobe input, (/EN65: LOW) R/W input
/CS1	51	50	DI	Chip select 1 input
CS2	30	29	DI	Chip select 2 input
/CSOUT	25	24	DO	Chip select output (if LOW, access to register is possible)
/IRQ1	45	44	DOD	Transmission interrupt request output (open-drain output)
/IRQ2	46	45	DOD	Reception interrupt request output (open-drain output)
/IRQ3	47	46	DOD	General interrupt request output (open-drain output)
/TEST	11	10	DIP	Test input (pull-up resistor incorporated)
TXD	37	36	DIP	Transmit data input (pull-up resistor incorporated)
RXD	42	41	DO	Receive data output
/RTS	38	37	DIP	Request to send input (pull-up resistor incorporated)
/CTS	41	40	DO	Clear to send output
/CD	44	43	DO	Data channel receive carrier detection output
ST1	39	38	DIP	Transmit data chock input (pull-up resistor incorporated)
ST2	40	39	DO	Transmit data clock output
RT	43	42	DO	Receive data clock output
RXI	17	16	AI	Receive signal input
RXC1	18	17	AO	AD conversion capacitor pin
RXC2	19	18	AO	AD conversion capacitor pin
RXC3	20	19	AO	AD conversion capacitor pin
RXF	16	15	AO	AD conversion output
TXO	14	13	AO	Transmit signal output (1 bit DAC output)
AUDIO	12	11	AO	Receive signal monitor output (1 bit DAC output)
PO1	22	21	DO	General-purpose output port 1
PO2	23	22	DO	General-purpose output port 2
PO3	24	23	DO	General-purpose output port 3
PI1	27	26	DI	General-purpose input port 1
PI2	28	27	DI	General-purpose input port 2
PI3	29	28	DI	General-purpose input port 3

Pin name	Pin No.		TYPE	Function
	QFP	TQFP		
EYEPAT	36	35	DO	Crystal oscillator pin or external oscillator clock input
EYECLK	35	34	DO	Crystal oscillator pin
VDD	52	51	PWR	Digital +3.3V / 5V source
VSS1	58	57	GND	Digital ground 1
VSS2	26	25	GND	Digital ground 2
AVDD	13	12	PWR	Analog +3.3V / 5V source
AVSS1	15	14	GND	Analog ground 1
AVSS2	21	20	GND	Analog ground 2
/RESET	31	30	DI	Reset input
/PWDM	32	31	DI	Power down mode setting input
XTAL1	33	32	XI	Crystal oscillator pin or external oscillator clock input
XTAL2	34	33	XO	Crystal oscillator pin

NOTE:

TYPE symbols

DI.....Digital input
DO.....Digital output
DIP.....Pull-up resistor incorporated digital input
DOD.....Open-drain output
DIO.....Digital input/output
AI.....Analog input
AO.....Analog output
PWR.....Power supply
GND.....Ground
XI,XO.....Crystal oscillator connection

■ INTERFACE REGISTER MAP

RS4~ RS0	Reg. No.		bit 7 (MSB)	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0 (LSB)
11111	1F	D	TXCONF							
11110	1E	D	TXINIT	-	TXTDIS	TXEPT	TXCBL2	TXCBL1	TXCLK2	TXCLK1
11101	1D	D	RTS	B202	-	PLAY	-	TXMHD	SDIS	TXS1
11100	1C	D	CTS	TXE	-	-	-	-	-	-
11011	1B	U	THDLC2	THDLC1	TXRUN2	TXRUN1	TXHDIE	TXABRT	TXFCS	TXFLAG
11010	1A	U	TXASYN	TXOSP	TXCHR2	TXCHR1	-	TXBE	TXPON	TXPODD
11001	19	U	TXREQ	TXRQIE	TXPDM	LB3	LB2	LB1	TXBRK	TXD8
11000	18	U	TXDATA							
10111	17	D	RXCONF							
10110	16	D	RXINIT	-	RXTDIS	-	RXCBL2	RXCBL1	-	-
10101	15	D	-	-	-	REC	EQHD	EQRS	DDIS	S1/P2IE
10100	14	D	CDET	FCD	SQD	TDET	300DET	SMDET	UMDET	S1/P2DET
10011	13	U	RHDLC2	RHDLC1	-	-	RXHDIE	RXABRT	RXCRC	RXFLAG
10010	12	U	RXASYN	RXOSP	RXCHR2	RXCHR1	-	RXBE	RXPON	RXPODD
10001	11	U	RXREQ	RXRQIE	RXDSEL	RXOVRN	RXPERR	RXFERR	BDET	RXD8
10000	10	U	RXDATA							
01111	0F	D	XRAMRQ	XRAMIE	XRAMW	XBYTE	XTIME	XBAUD	XRAMA9	XRAMA8
01110	0E	D	XRAMA							
01101	0D	D	XRAMDM							
01100	0C	D	XRAMDL							
01011	0B	D	YRAMRQ	YRAMIE	YRAMW	YBYTE	YTIME	YBAUD	YRAMA9	YRAMA8
01010	0A	D	YRAMA							
01001	09	D	YRAMDM							
01000	08	D	YRAMDL							
00111	07	D	TONE4	TONE3	TONE2	TONE1	AGC4	-	-	AGC1
00110	06	D	AHS	AUDIO1	AUDIO2	FRSP	GC4	GC3	GC2	GC1
00101	05	D	TIME4	TIME3	TIME2	TIME1	-	FR3	FR2	FR1
00100	04	D	COL4	COL3	COL2	COL1	ROW4	ROW3	ROW2	ROW1
00011	03	D	TIME4E	TIME3E	TIME2E	TIME1E	TIME1R	TIMEIE	-	-
00010	02	D	-	-	-	-	-	-	-	-
00001	01	¥	SRESET	PWRSV	PI2IE	PI1IE	-	PO3	PO2	PO1
00000	00	¥	WRBUSY	IA1	IA2	IA3	-	PI3	PI2	PI1

Note: For the bits indicated by - , "0" must always be written.

No mesh :Control bit

:Status bit

:Bit with both control bit and status bit function

:Bit that causes an interrrupt

D :DSP-related register

U :USART circuit-related register

¥ :Registers composed of asynchronous circuits, and remain operational even during the power save mode.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (VSS1=VSS2=AVSS1=AVSS2=0[V])

Item	Symbol	Rating		Unit
		min.	max.	
Source Voltage	V_{DD}	- 0.5	7.0	V
Input Voltage	V_I	- 0.5	VDD + 0.5	V
Output Voltage	V_O	- 0.5	VDD + 0.5	V
Storage temperature	T_{stg}	- 50	125	℃

(The electrical characteristics are all target specifications.)

2. Recommended Operating Conditions (VSS1=VSS2=AVSS2=0 [V])

Item	Symbol	Rating			Unit
		min.	typ.	max.	
Source Voltage	V_{DD}	3.0	3.3	5.5	V
Operational ambient temperature	T_{op}	-40	25	85	℃
Clock frequency	f_{CLK}	19.6588	19.6608	19.6628	MHz

(The electrical characteristics are all target specifications.)

3.DC Characteristics

(Where not otherwise specified,the recommended operating conditions apply)

(1) @VDD =3.3 ± 0.3V

Item		Symbol	Applicable pin type and measuring condition	Rating			Unit
				min.	typ.	max.	
High-level input voltage		V_{DIH}	DI,DIP,DIO	2.0	-	-	V
Low-level input voltage		V_{DIL}	DI,DIP,DIO	-	-	$0.2V_{DD}$	V
Input leak current		I_{LDIH}	DI	-10	-	10	µA
Pull-up current		I_{PU}	DIP	-20	-	-200	µA
Input capacitance (*1)		C_I	DI,DIP	-	10	-	pF
High-level output voltage		V_{DOH}	DO,DIO @I_{OH}=-1.0mA @I_{OL}=2mA	2.4	-	-	V
Low-level output voltage		V_{DOL}		-	-	0.4	V
Open-drain low-level output current		I_{DOD}	DOD @0.4V	-	-	4.0	mA
Output leak current		I_{LOUT}	DIO,DOD (At HI-Z)	-10	-	10	µA
Output capacitance (*1)		C_O	DO,DIO,DOD	-	15	-	pF
High-level clock input voltage		V_{CLKH}	XI (*2)	$0.8V_{DD}$	-	-	V
Low-level clock input voltage		V_{CLKL}	XI (*2)	-	-	$0.2V_{DD}$	V
Clock input leak current		I_{LCLK}	XI (*2)	-100	-	100	µA
Clock input capacitance (*1)		C_{LI}	XI (*2)	-	15	-	pF
Analog input voltage range		V_{AI}	AI	0.0	-	V_{DD}	V
Analog input leak current		I_{LAI}	AI	-1	-	1	mA
Analog output voltage range		V_{AO}	AO	0.0	-	V_{DD}	V
Source current (*3)	Normal operation	I_{DD}	PWR,GND	-	30	50	mA
	Power save	I_{PSV}		-	80	160	µA
	Power down	I_{PWN}		-	5	20	µA

(*1) Under operational ambient temperature T_{OP} = 25℃,and source voltage V_{DD} = 3.3V

(*2) When external clock is input

(*3) The source current (type) is under source voltage V_{DD} = 3.3V , and operational ambient temperature T_{OP}= 25℃,and (max.) is under V_{DD} = 3.6V, T_{OP} = recommended condition.

(2) @VDD = 5.0 ± 0.5V

Item		Symbol	Applicable pin type and measuring condition	Rating			Unit
				min.	typ.	max.	
High-level input voltage		V_{DIH}	DI,DIP,DIO	2.0	-	-	V
Low-level input voltage		V_{DIL}	DI,DIP,DIO	-	-	0.8	V
Input leak current		I_{LDIH}	DI	-10	-	10	µA
Pull-up current		I_{PU}	DIP	-20	-	-200	µA
Input capacitance (*1)		C_I	DI,DIP	-	10	-	pF
High-level output voltage		V_{DOH}	DO,DIO @I_{OH}=-2.0mA	V_{DD}-1.0	-	-	V
Low-level output voltage		V_{DOL}	@I_{OL}=2mA	-	-	0.4	V
Open-drain low-level output current		I_{DOD}	DOD @0.4V	-	-	4.0	mA
Output leak current		I_{LOUT}	DIO,DOD (At HI-Z)	-10	-	10	µA
Output capacitance (*1)		C_O	DO,DIO,DOD	-	15	-	pF
High-level clock input voltage		V_{CLKH}	XI (*2)	V_{DD}-1.0	-	-	V
Low-level clock input voltage		V_{CLKL}	XI (*2)	-	-	1.0	V
Clock input leak current		I_{LCLK}	XI (*2)	-100	-	100	µA
Clock input capacitance (*1)		C_{LI}	XI (*2)	-	15	-	pF
Analog input voltage range		V_{AI}	AI	0.0	-	V_{DD}	V
Analog input leak current		I_{LAI}	AI	-1	-	1	mA
Analog output voltage range		V_{AO}	AO	0.0	-	V_{DD}	V
Source current (*3)	Normal operation	I_{DD}	PWR,GND	-	60	100	mA
	Power save	I_{PSV}		-	200	500	µA
	Power down	I_{PWN}		-	5	50	µA

(*1) Under operational ambient temperature T_{OP} = 25℃,and source voltage V_{DD} = 5.0V

(*2) When external clock is input

(*3) The source current (type) is under source voltage V_{DD} = 5.0V , and operational ambient temperature T_{OP} = 25℃,and (max.) is under V_{DD}= 5.5V, T_{OP} = recommended condition.

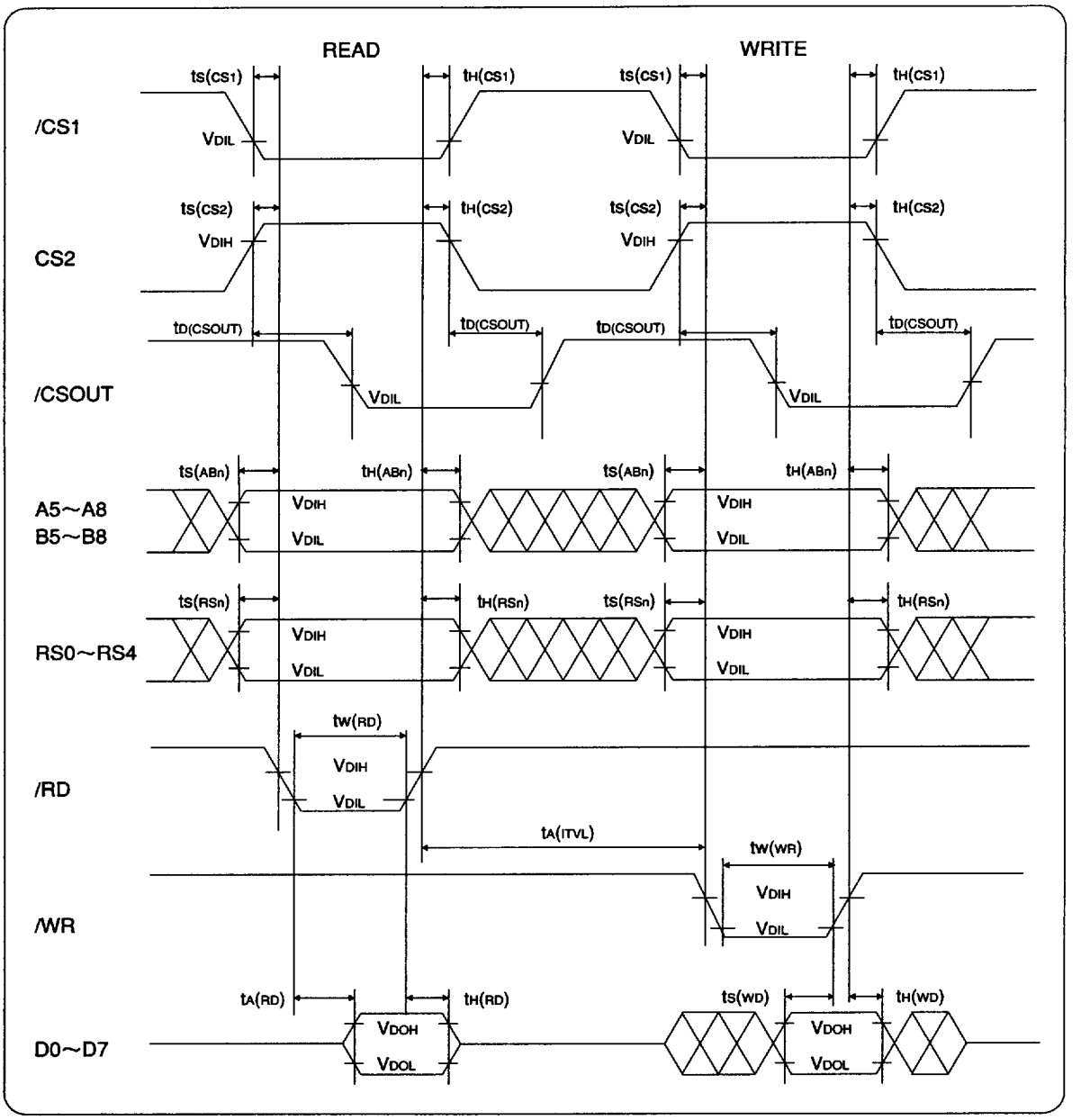
4. AC Characteristics

(Where not otherwise specified the recommended operating conditions apply)

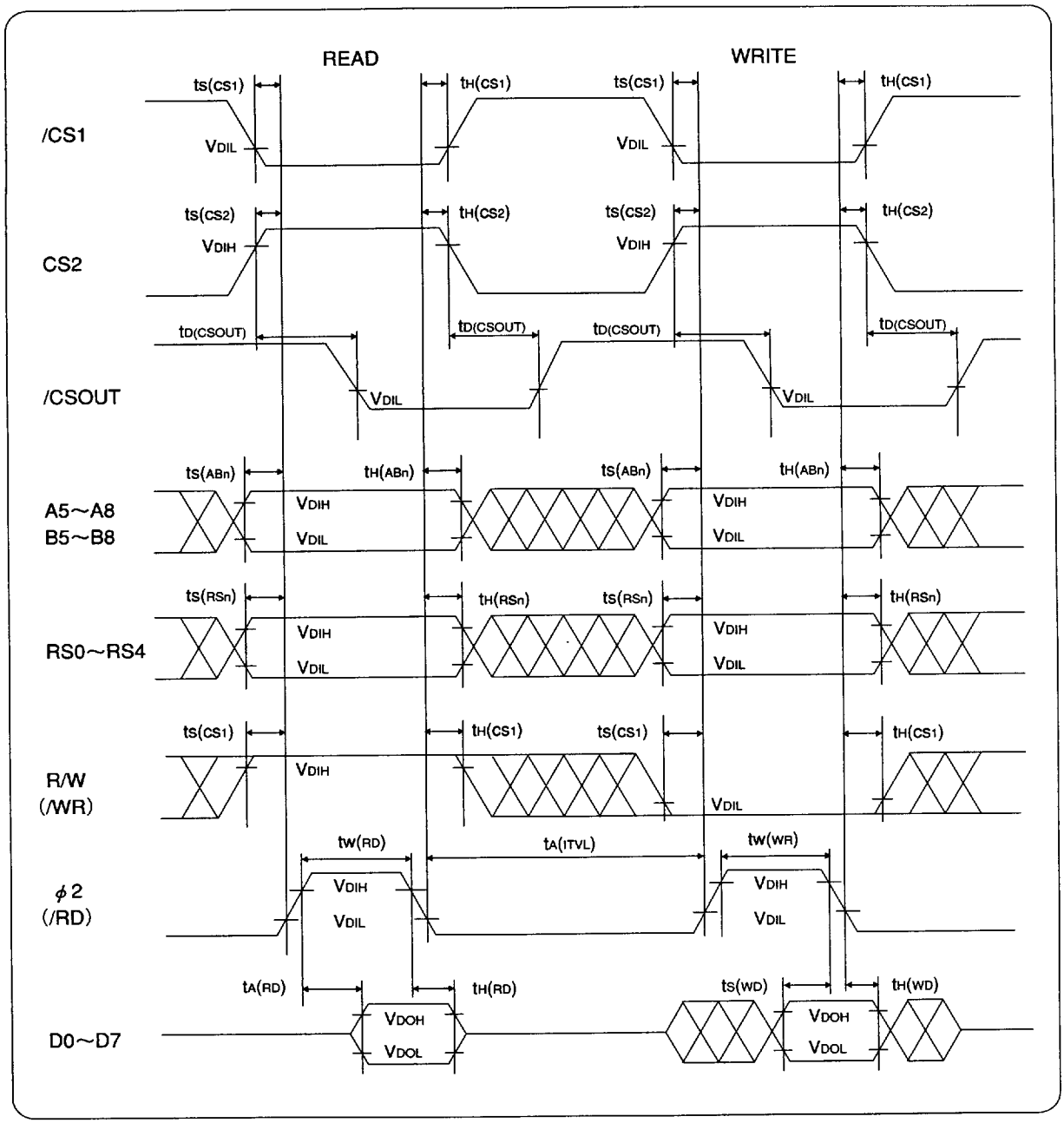
Item	Symbol	Condition	Rating			Unit
			min.	typ.	max.	
Reset input pulse width	$t_{w(RESET)}$		1.0	-	-	ms
/CS1 set-up time	$t_{S(CS1)}$	to /RD, /WR	0	-	-	ns
CS2 set-up time	$t_{S(CS2)}$					
/CS1 hold time	$t_{H(CS1)}$	from /RD, /WR	0	-	-	ns
CS2 hold time	$t_{H(CS2)}$					
/CSOUT delay time	$t_{D(CSOUT)}$	C_L=100pF	-	-	80	ns
ABn set-up time	$t_{S(ABn)}$	to /RD, WR	10	-	-	ns
ABn hold time	$t_{H(ABn)}$	from /RD, /WR	10	-	-	ns
RSn set-up time	$t_{S(RSn)}$	to /RD, /WR	10	-	-	ns
RSn hold time	$t_{H(RSn)}$	from /RD, /WR	10	-	-	ns
Write data set-up time	$t_{S(WD)}$		30	-	-	ns
Write data hold time	$t_{H(WD)}$		10	-	-	ns
Write strobe pulse width	$t_{W(WR)}$		60	-	-	ns
Read data access time	$t_{A(RD)}$	C_L=100pF	-	-	80	ns
Read data hold time	$t_{H(RD)}$		10	-	50	ns
Read strobe pulse width	$t_{W(RD)}$		60	-	-	ns
Read / write access interval	$t_{A(ITVL)}$	(*1)	1	-	-	µs

(*1) Interface register access interval

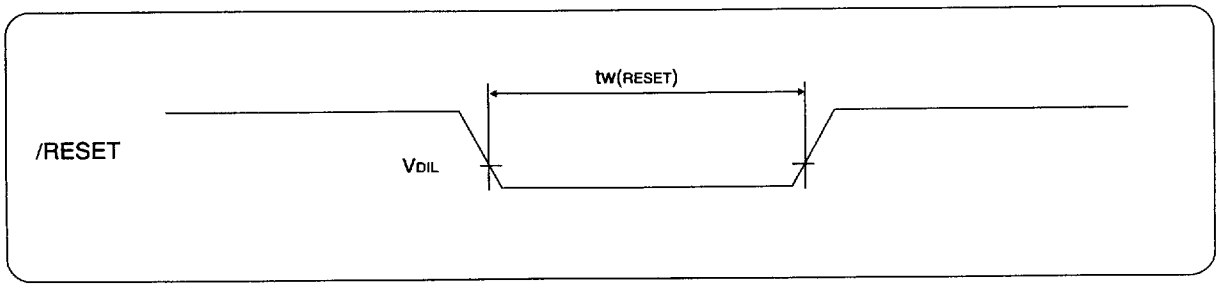
5. AC Characteristics Timing Chart
(a) 80 type mode (/EN65 = HIGH)



(b) 6502 type (68 type) mode (/EN65 = LOW)

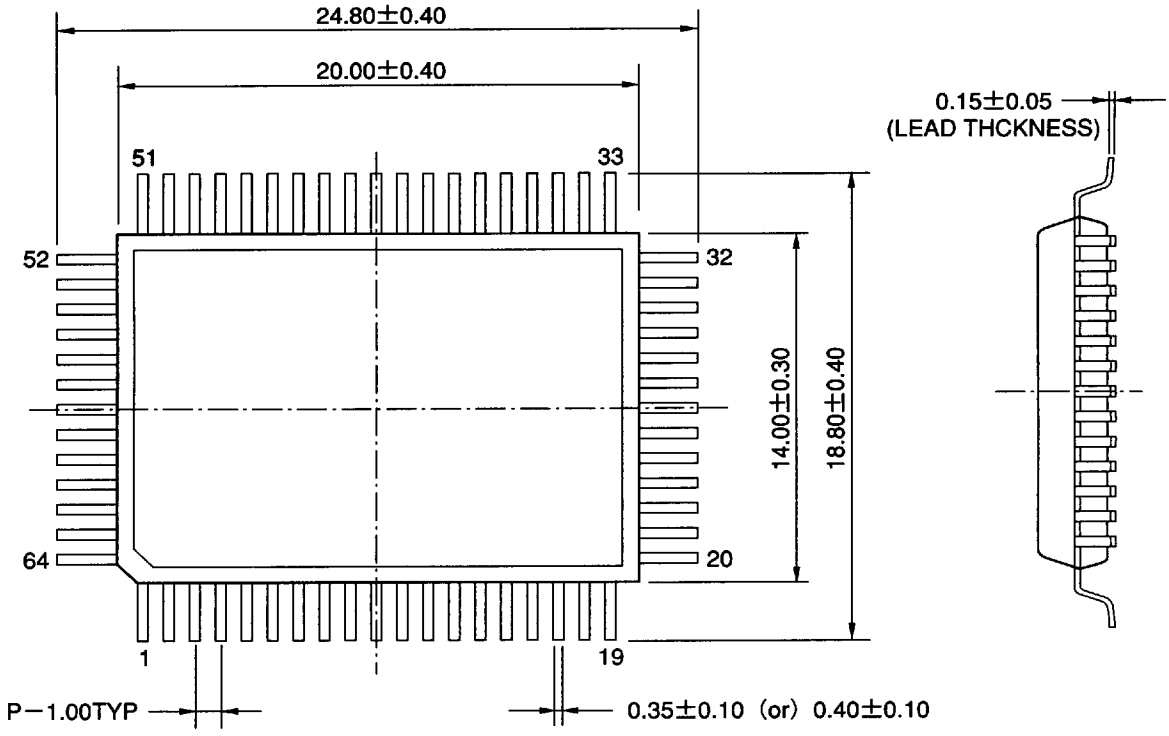


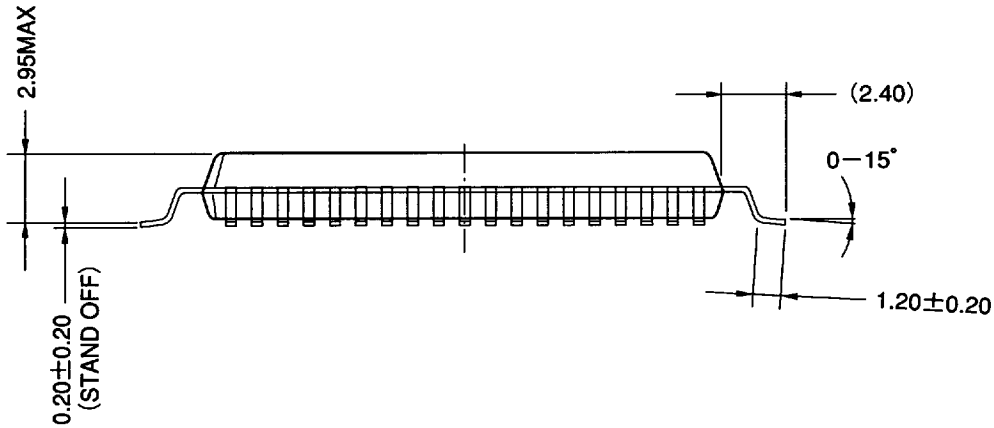
(c) Reseting



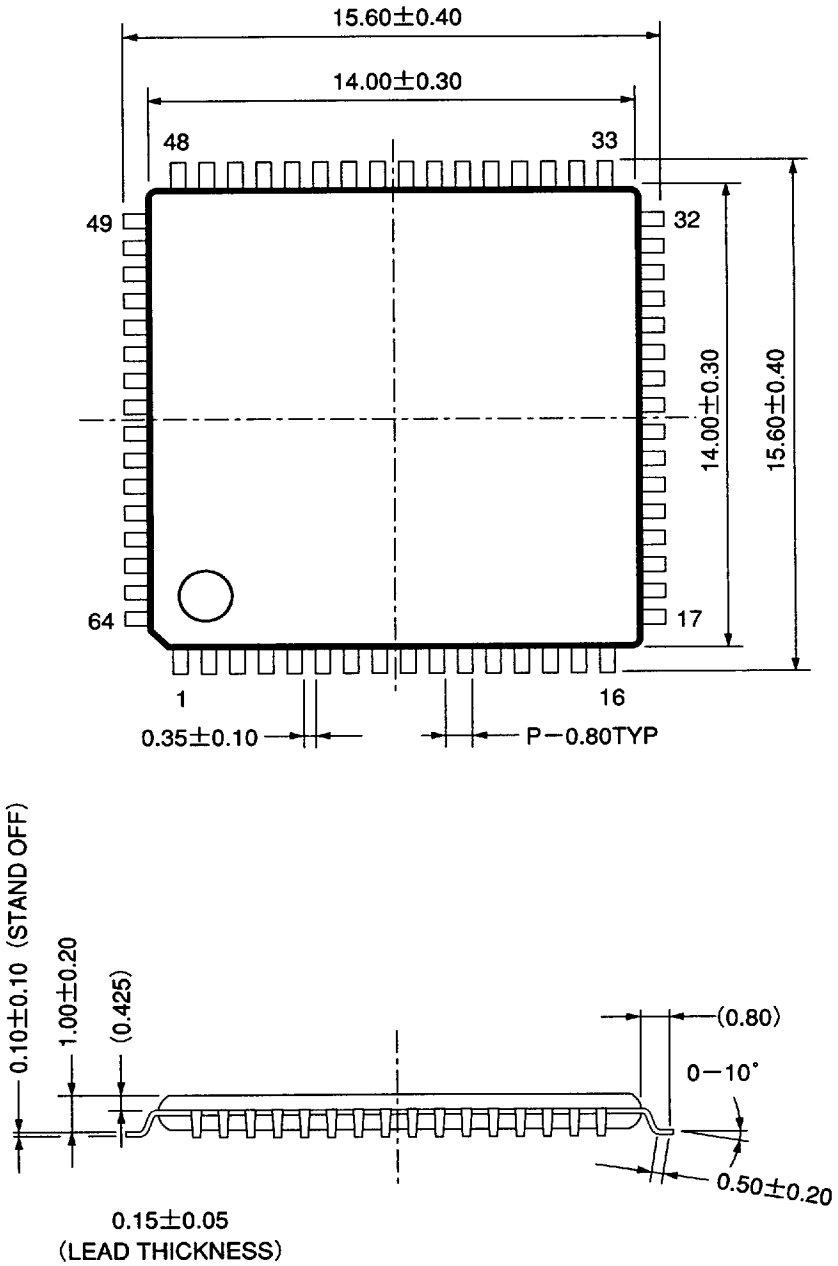
■ EXTERNAL DIMENSIONS

(1) 64-pin QFP





(2) 64-pin TQFP



The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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