Initializing The CIO

Zilog

Application Note

October 1982

INTRODUCTION

Zilog's Z8536 Counter/Timer and Parallel I/O Unit (CIO) and Z8036 (Z-CIO) can provide convenient solutions to many microprocessor-based design problems. Their handshake control, bit manipulation, pattern recognition, and interrupt control capabilities extend the range of applications far beyond that of traditional counter/timer and parallel I/O circuits. This application note gives a generalized procedure for initializing the CIO, as well as an initialization example for one particular application. All comments in this document referring to "the CIO" apply to both the Z8036 and Z8536. References to the Z-CIO refer only to the Z8036.

ACCESSING THE REGISTERS

From the programmer's point of view, the only difference between the Z8036 and the Z8536 is the way the registers are accessed. In the Z8036, they are mapped directly into the CPU's I/O address space, and the Right Justified Address (RJA) bit in the Master Interrupt Control register determines which address bits are used to select them. When RJA = 0, bits AD_6-AD_1 are decoded, and when RJA = 1, bits AD_5-AD_0 are decoded.

The Z8536 uses only A_0 and A_1 to select the registers and thus occupies only four bytes of I/O address space. The Data registers for each port are accessed directly using A_0 and A_1. The Control registers (as well as the Data registers) can be accessed using the following two-step sequence with $A_0 = A_1 = 1$: first, write the address of the target register to an internal 6-bit pointer register; then read from or write to the target register. An internal state machine determines whether a given access refers to the pointer or the target register.

SOFTWARE RESET

A software reset is performed by writing a 1 to the Reset bit in the Master Interrupt Control register. This causes all control bits to be reset to 0, all port I/O lines to be at high impedance, the Interrupt pin to be inactive, and the Interrupt Enable Output (IEO) pin to follow the Interrupt Enable Input (IEI) pin. A reset disables all functions except a read or write to the Reset bit; therefore the Reset bit must be cleared before any other control bits can be programmed.

INITIALIZATION

Once the CIO has been reset and, in the Z-CIO, the RJA bit has been programmed, it can easily be initialized for a given application by using the procedures outlined in the flowcharts of Figures 1 through 7. These flowcharts are intended to serve more as a logical guide than as a sequential algorithm. The actual sequence of initialization is unimportant, except that a few basic rules must be observed:

- The ports and counter/timers should be enabled only after their functions have been completely specified.
- When Ports A and B are linked, Port B should be enabled before, or simultaneously with, the enabling of Port A. Also, the Port Link Control (PLC) bit in the Master Configuration Control register should be set before either port is enabled.

- The counter/timers should be triggered only after they have been enabled.
- When Counter/Timers 1 and 2 are linked, the functions of both must be specified and the Counter/Timer Link Control (LC) bits (in the Master Configuration Control register) must be programmed before either counter/timer is enabled.
- The Master Interrupt Enable (MIE) bit in the Master Interrupt Control register should be set only after the functions of the CIO's interrupt sources have been completely specified.

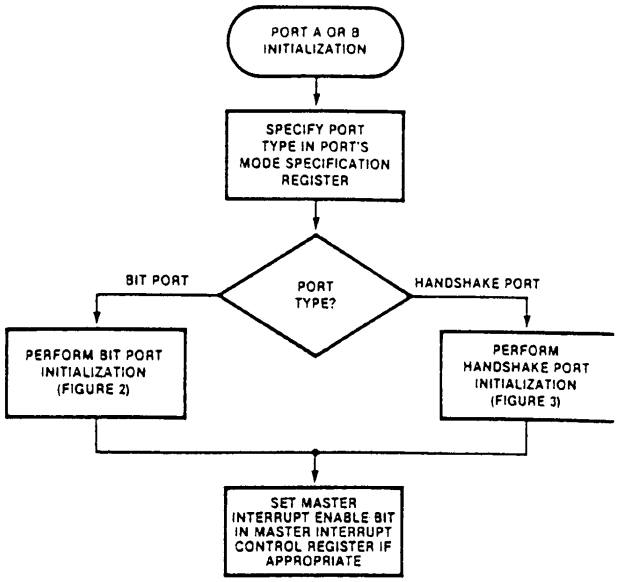


Figure 1. Port A or B Initialization

Table 1. Z8036/Z8536 CIO Register Summary

Internal Address (Binary)	Read/Write	Register Name
$A_5...A_0$		**Main Control Registers**
000000	R/W	Master Interrupt Control
000001	R/W	Master Configuration Control
000010	R/W	Port A Interrupt Vector
000011	R/W	Port B Interrupt Vector
000100	R/W	Counter/Timer Interrupt Vector
000101	R/W	Port C Data Path Polarity
000110	R/W	Port C Data Direction
000111	R/W	Port C Special I/O Control
		Most Often Accessed Registers
001000	*	Port A Command and Status
001001	*	Port B Command and Status
001010	*	Counter/Timer 1 Command and Status
001011	*	Counter/Timer 2 Command and Status
001100	*	Counter/Timer 3 Command and Status
001101	R/W	Port A Data**
001110	R/W	Port B Data**
001111	R/W	Port C Data**
		Counter/Timer Related Registers
010000	R	Counter/Timer 1 Current Count (MS Byte)
010001	R	Counter/Timer 1 Current Count (LS Byte)
010010	R	Counter/Timer 2 Current Count (MS Byte)

* All bits can be read and some bits can be written.

** Also directly addressable in Z8536 using pins A_0 and A_1.

Table 1. Z8036/Z8536 CIO Register Summary--Continued

Internal Address (Binary)	Read/Write	Register Name
		Counter/Timer Related Registers (continued)
010011	R	Counter/Timer 2 Current Count (LS Byte)
010100	R	Counter/Timer 3 Current Count (MS Byte)
010101	R	Counter/Timer 3 Current Count (LS Byte)
010110	R/W	Counter/Timer 1 Time Constant (MS Byte)
010111	R/W	Counter/Timer 1 Time Constant (LS Byte)
011000	R/W	Counter/Timer 2 Time Constant (MS Byte)
011001	R/W	Counter/Timer 2 Time Constant (LS Byte)
011010	R/W	Counter/Timer 3 Time Constant (MS Byte)
011011	R/W	Counter/Timer 3 Time Constant (LS Byte)
011100	R/W	Counter/Timer 1 Mode Specification
011101	R/W	Counter/Timer 2 Mode Specification
011110	R/W	Counter/Timer 3 Mode Specification
011111	R	Current Vector
		Port A Specification Registers
100000	R/W	Port A Mode Specification
100001	R/W	Port A Handshake Specification
100010	R/W	Port A Data Path Polarity
100011	R/W	Port A Data Direction
100100	R/W	Port A Special I/O Control
100101	R/W	Port A Pattern Polarity
100110	R/W	Port A Pattern Transition
100111	R/W	Port A Pattern Mask
		Port B Specification Registers
101000	R/W	Port B Mode Specification
101001	R/W	Port B Handshake Specification
101010	R/W	Port B Data Path Polarity
101011	R/W	Port B Data Direction
101100	R/W	Port B Special I/O Control
101101	R/W	Port B Pattern Polarity
101110	R/W	Port B Pattern Transition
101111	R/W	Port B Pattern Mask

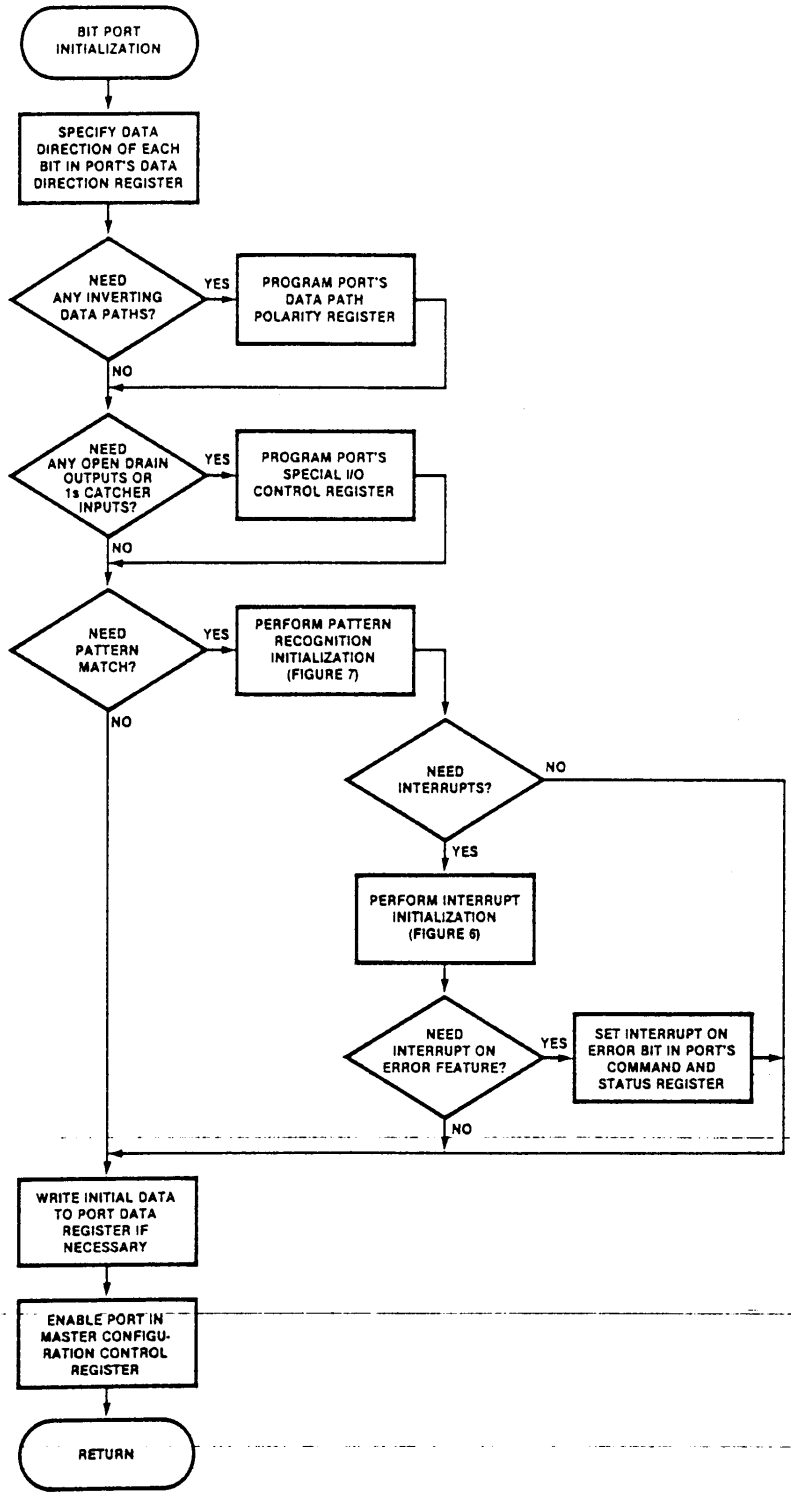
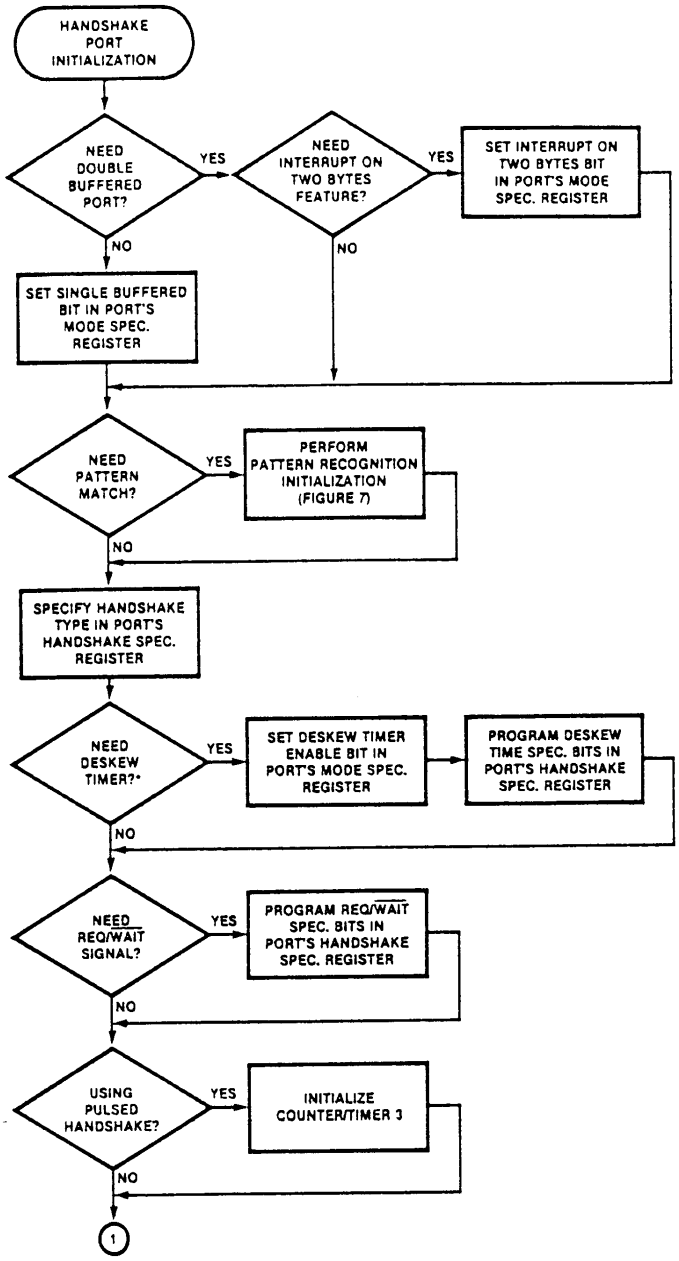


Figure 2. Bit Port Initialization



*Deskew Timers Are Used Only For Output Ports.

Figure 3. Handshake Port Initialization

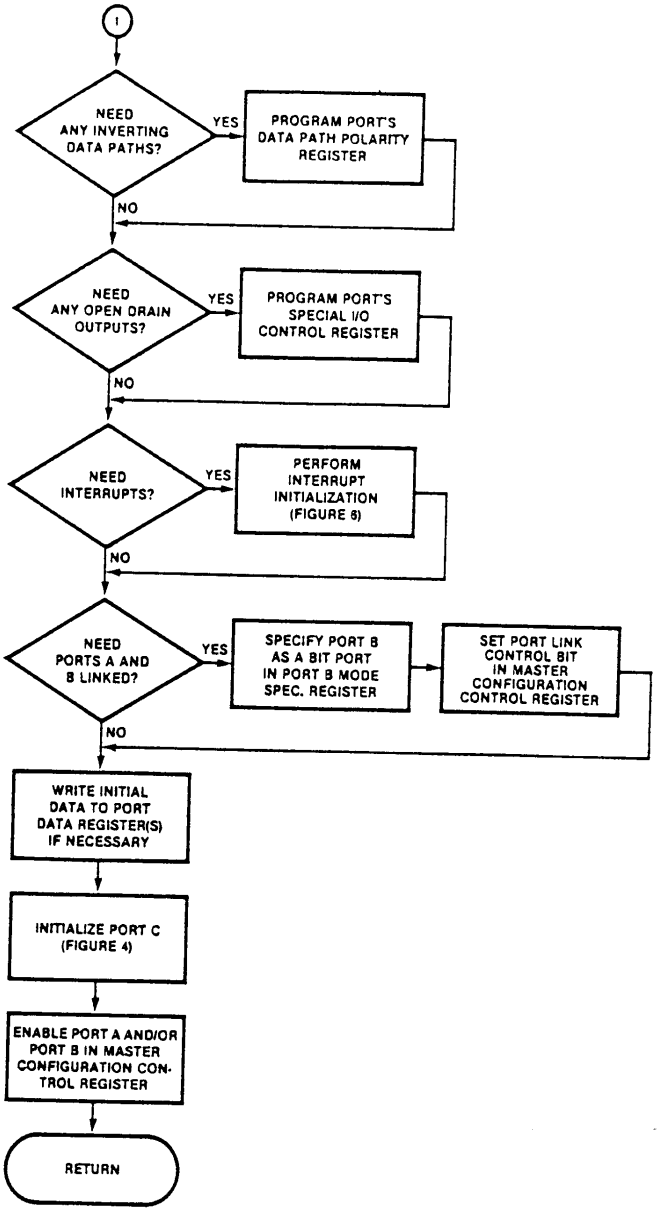


Figure 3. Handshake Port Initialization (continued)

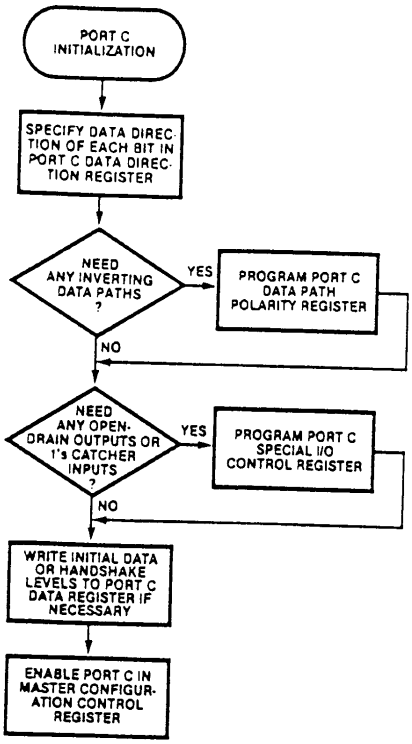


Figure 4. Port C Initialization

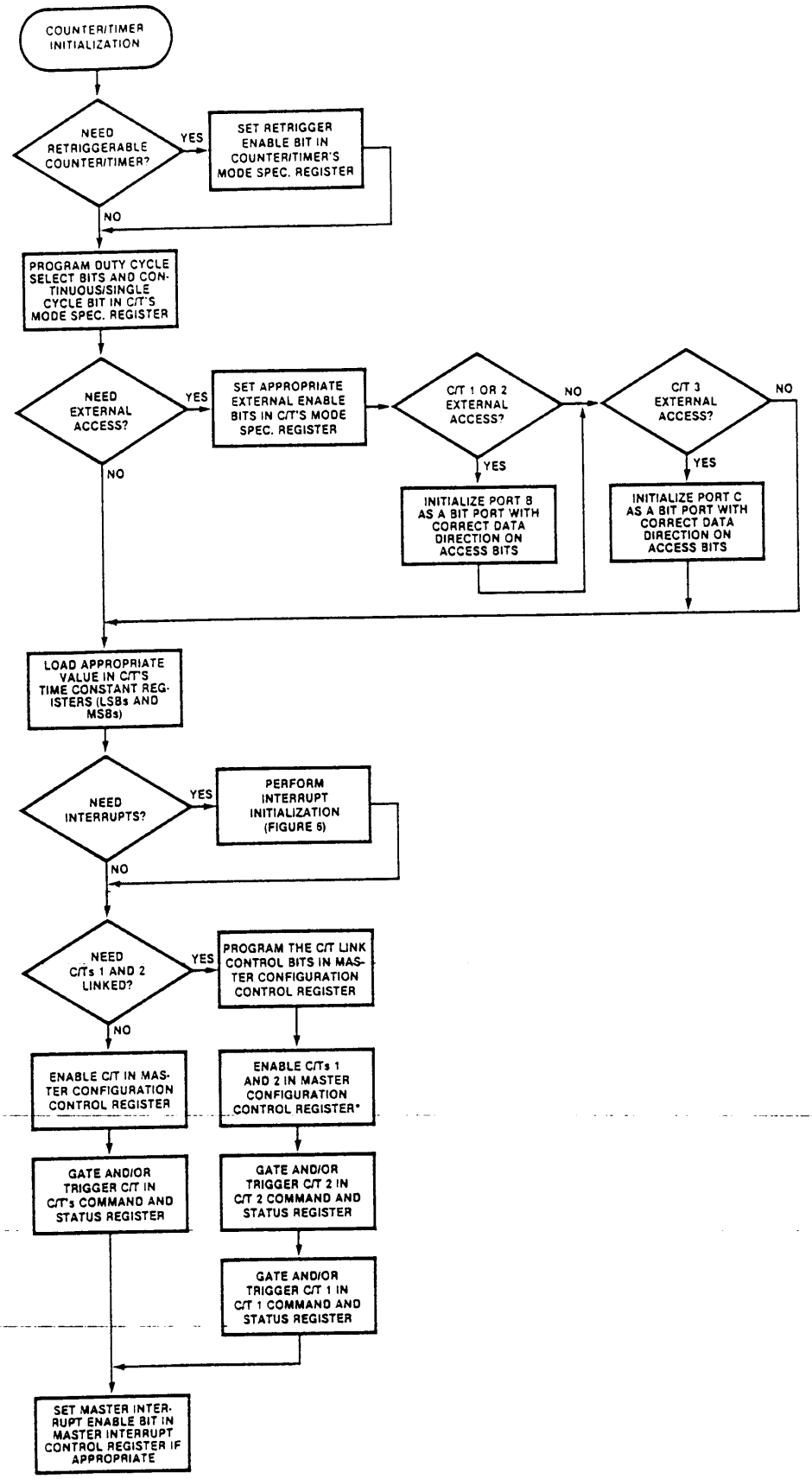


Figure 5. Counter/Timer Initialization

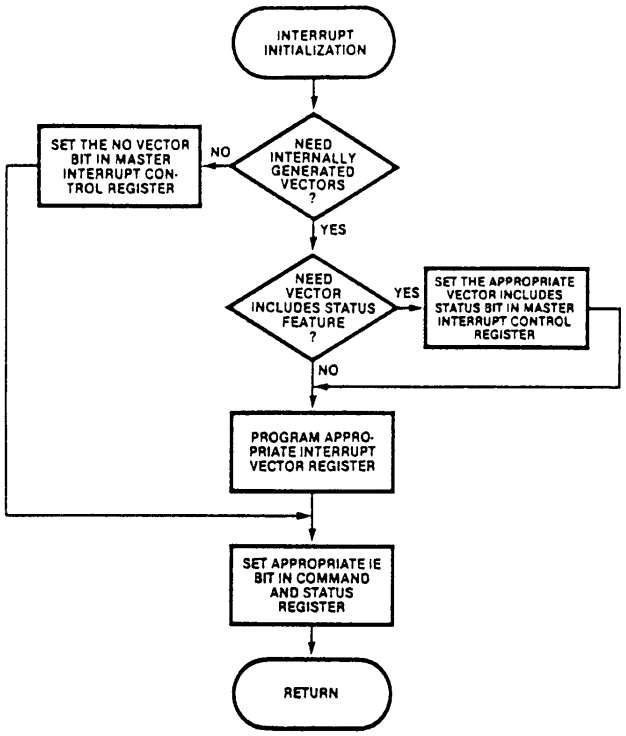


Figure 6. Interrupt Initialization

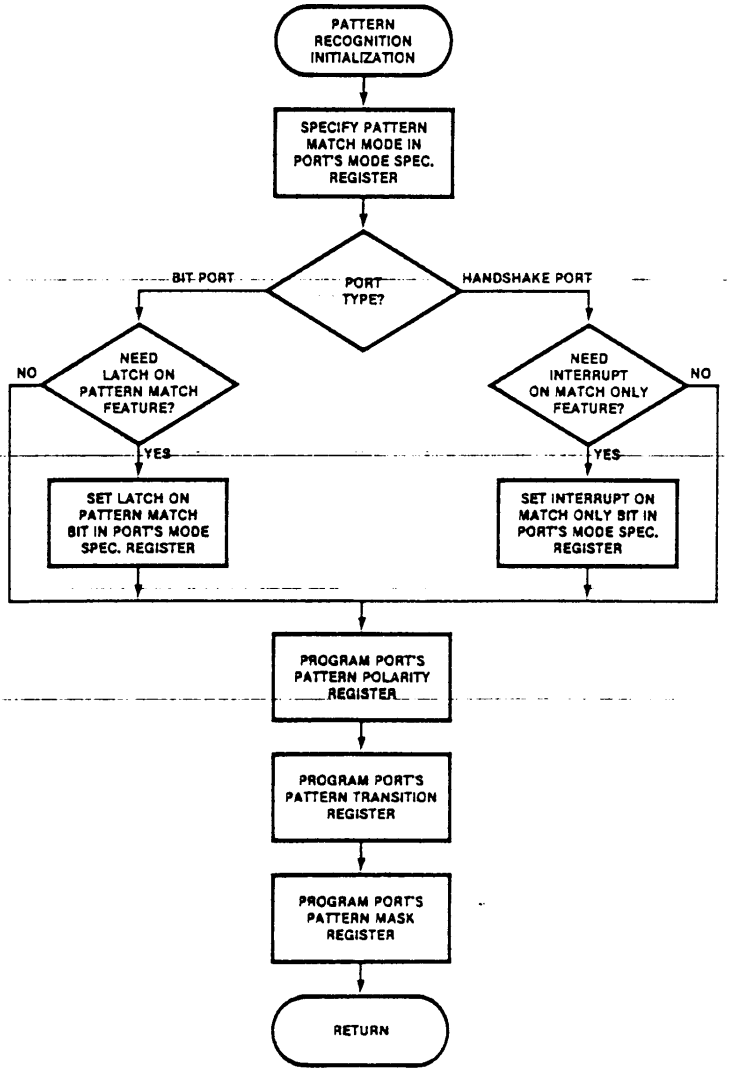


Figure 7. Pattern Recognition Initialization

APPLICATION EXAMPLE

Figure 8 shows the Z8036 configured to function as:

- An input handshake port
- A priority interrupt controller
- A squarewave generator
- A watchdog timer
- A general-purpose timer

In addition, there are two bits left over to function as bit-addressable output lines. The following sections discuss the specific initialization procedures used to program each of the functions.

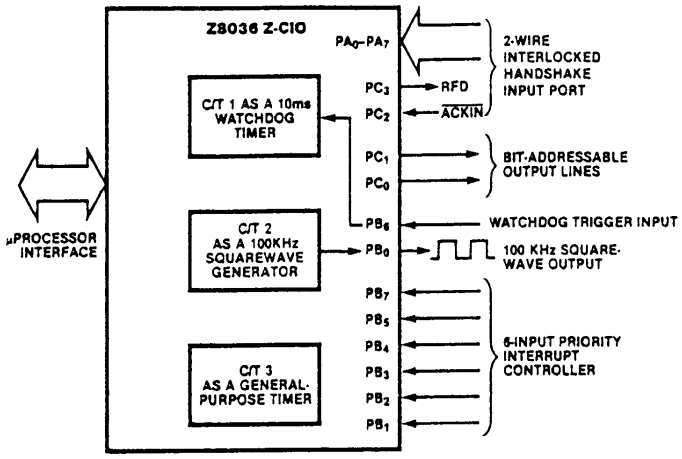


Figure 8. Z-CIO Application Example

Port A as an Input Handshake Port

In Figure 8, Port A is an input port with 2-Wire Interlocked Handshake. (The CIO also supports Strobed Handshake, Pulsed Handshake, and IEEE 3-Wire Handshake.) Port C provides the handshake control signals, with PC_2 as $\overline{ACKIN}$ (Acknowledge Input) and PC_3 as the RFD (Ready For Data) output.

Port A is specified as an input handshake port by writing a 0 to bit D_7 and a 1 to bit D_6 of the Port A Mode Specification register. Writing a 1 to bit D_5 and a 0 to bit D_4 of the same register specifies the double-buffered mode and allows the port to interrupt the CPU when both the Buffer register and Input Data register are full. Since the ports reset to Interlocked Handshake, the Port A Handshake Specification register need not be programmed in this example.

If Port A is to place an interrupt vector on the system bus during Interrupt Acknowledge transactions, then the Port A Interrupt Vector register should be programmed with the appropriate value. The Port A interrupt logic is enabled by writing 1s to bits D_7 and D_6, and a 0 to bit D_5 of the Port A Command and Status register. This encoded command sets the Port A Interrupt Enable (IE) bit.

The programmer should specify the correct data direction for the handshake bits, as well as the initial state of RFD. Writing F4 (hexidecimal) to the Port C Data Direction register programs PC_3 (RFD) as an output bit, PC_2 ($\overline{ACKIN}$) as an input bit, and allows PC_1 and PC_0 to function as bit-addressable output lines. PC_0, PC_1, and PC_3 can be programmed with their initial values by writing to the Port C Data register. In this example, PC_3 (RFD) is initially High, signaling that Port A is ready for data.

Port B as a Priority Interrupt Controller

The priority interrupt controller is implemented using the OR-Priority Encoded Vector (OR-PEV) mode of pattern recognition. When any of the six inputs (PB_1-PB_5 and $PB7_7$) are High, Port B's Pattern Match Flag and Interrupt Pending (IP) bits are set. If no higher priority interrupt sources (e.g., Port A) are under service, and if Port B's interrupts are enabled, the CIO interrupts the CPU. If no higher priority interrupts are pending at the time of the next Interrupt Acknowledge cycle, then Port B places its interrupt vector on the bus. Encoded within this vector is the value of the highest priority interrupt request at Port B (with PB_7 as the highest priority input). The CPU can then automatically branch to the appropriate service routine.

To function as a priority interrupt controller, Port B must be specified as a bit port with OR-PEV pattern match; hence a 06_H must be loaded into the Port B Mode Specification register. PB_1-PB_5 and PB_7 must be programmed as input bits by writing 1s to bits D_1-D_5 and D_7 of the Port B Data Direction register. The polarity of the interrupt request signals can be specified independently in the Port B Pattern Polarity register and the sources can be individually masked using the Port B Pattern Mask register. In this example, all of the interrupts are active High and bits PB_0 and

PB_6 are masked off; FF_H is therefore loaded into the Port B Pattern Polarity register, and BE_H is loaded into the Port B Pattern Mask register. Transition pattern specifications should not be used in the OR-PEV pattern match mode, so the Port B Pattern Transition register should not be programmed.

The base interrupt vector should be loaded into the Port B Interrupt Vector register, and the Port B interrupt logic is enabled by writing 1s to bits D_7 and D_6, and a 0 to bit D_5 of the Port B Command and Status register. Also, the Port B Vector Includes Status (VIS) bit should be set so that unique vectors can be generated for each of the interrupt sources (this can be done at the same time the MIE bit is set).

Counter/Timer 1 as a Watchdog Timer

In this example, Counter/Timer 1 acts as a watchdog timer, interrupting the CPU whenever a 10 ms interval elapses without the occurrence of a rising edge on its trigger input (PB_6). Each time the timer is triggered (i.e., with each rising edge on PB_6), it reloads its time constant and begins counting down toward the terminal count. Since the Counter/Timer 1 Time Constant is programmed to provide a timeout interval of 10 ms, a terminal count condition always indicates that at least 10 ms has elapsed since the last rising edge on PB_6.

The programmer must set bits D_2 and D_4 of the Counter/Timer 1 Mode Specification register. Bit D_2 is the Retrigger Enable (REB) bit, and D_4 is the External Trigger Enable (ETE) bit. All other bits in this register can remain reset to 0. Since PB_6 is the designated external trigger input whenever Counter/Timer 1's ETE bit is set, Port B must be programmed as a bit port and PB_6 must be programmed as an input bit.

Since Counter/Timer 1 is in the Timer mode (i.e., it does not have an external count input), it counts the pulses of the internal clock signal (PCLK/2). Assuming a 4 MHz PCLK, the Time Constant should be $20{,}000_{10}$ for a 10 ms timeout interval. This can be achieved by loading $4E_H$ to the most-significant byte of Counter/Timer 1's Time Constant, and 20_H to the least-significant byte of Counter/Timer 1's Time Constant.

The base interrupt vector should be loaded into the Counter/Timer Interrupt Vector register, and the Counter/Timer 1 interrupt logic is enabled by writing 1s to bits D_7 and D_6, and a 0 to bit D_5 of the Counter/Timer 1 Command and Status register. Also, the Counter/Timer VIS bit should be set so that Counter/Timers 1 and 2 can generate unique vectors. (This can be done at the same time the MIE bit is set.)

Counter/Timer 2 as a Squarewave Generator

While Counter/Timer 1 uses PB_6 as its trigger input, Counter/Timer 2 can use PB_0 as its output. The squarewave duty cycle is selected by writing a 1 to bit D_1 and a 0 to bit D_0 of the Counter/Timer 2 Mode Specification register. Setting bits D_7 and D_6 of the same register specifies the Continuous mode with an external output. Since PB_0 is the designated Counter/Timer 2 output whenever Counter/Timer 2's External Output Enable (EOE) bit is set, Port B must be programmed as a bit port and PB_0 must be programmed as an output bit.

In the Squarewave mode, the timeout interval should be equal to half the period of the desired squarewave (see the CIO Technical Manual, section 4.2.5, document number 00-2091-01). A frequency of 100 KHz corresponds to a period of 10 µs and, therefore, a timeout interval of 5 µs. With a 4MHz PCLK, the period of the input clock signal (PCLK/2) is 0.5 µs, and therefore the necessary Time Constant is 10_{10} or $000A_H$. This value should be loaded into the Counter/Timer 2 Time Constant registers. Since the squarewave generator does not interrupt the CPU, there is no need to enable Counter/Timer 2's interrupt logic.

Counter Timer 3 as a General-Purpose Timer

For Counter/Timer 3 to interrupt the CPU periodically, the user must specify the Continuous mode by setting bit D_7 of the Counter/Timer 3 Mode Specification register. All other bits in this register can remain reset to 0. Loading $4E20_H$ to the Counter/Timer 3 Time Constant registers specifies a 10 ms timeout interval. Writing 1s to bits D_7 and D_6, and a 0 to bit D_5 of the Counter/Timer 3 Command and Status register enables the Counter/Timer 3 interrupt logic.

When all of their functions have been completely specified, the ports and counter/timers can be enabled simultaneously by writing $F4_H$ to the Master Configuration Control register. At this point, the counter/timers can be started by setting the Gate Command (GCB) and Trigger Command (TCB) bits in each of their Command and Status registers. Finally, setting the MIE bit, along with the appropriate VIS bits, completes the initialization. Table 2 summarizes the initialization sequence for this application example.

Table 2. Initialization Sequence for Application Example

Step	Register Programmed	Address AD_7-AD_0	Hex Value Loaded	Comments
1.	Master Interrupt Control	X0000000*	01	Reset Z-CIO.
2.	Master Interrupt Control	X000000X	00	Clear Reset.
3.	Port A Mode Specification	X100000X	60	Double-buffered input port, interrupt on two bytes.
4.	Port A Interrupt Vector	X000010X	VV	Interrupt vector depends on user's system.
5.	Port A Command and Status	X001000X	C0	Port A Interrupt Enable.
6.	Port C Data Direction	X000110X	F4	PC_2 is input PC_0, PC_1 and PC_3 are output.
7.	Port C Data	X001111X	48	RFD is initially High. PC_0 and PC_1 are initially Low.
8.	Port B Mode Specification	X101000X	06	Bit port, OR-PEV pattern match.
9.	Port B Data Direction	X101011X	FE	PB_0 is output. PB_1-PB_7 are input.
10.	Port B Pattern Polarity	X101101X	FF	Interrupt inputs are active High.
11.	Port B Pattern Mask	X101111X	BE	PB_0 and PB_6 are masked off.
12.	Port B Interrupt Vector	X000011X	VV	Interrupt vector depends on user's system.
13.	Port B Command and Status	X001001X	C0	Port B Interrupt Enable.
14.	Counter/Timer 1 Mode Specification	X011100X	14	Single cycle, External Trigger Enable, Retrigger Enable.
15.	Counter/Timer 1's Time Constant-MSBs	X010110X	4E	Time Constant = $(20,000)_{10}$ for a 10 ms timeout.
16.	Counter/Timer 1's Time Constant-LSBs	X010111X	20	

* If the initial state of the RJA bit is unknown, then the first access to the Master Interrupt Control register must be performed with AD_0 = 0.

Table 2. Initialization Sequence for Application Example--Continued

Step	Register Programmed	Address AD_7-AD_0	Hex Value Loaded	Comments
17.	Counter/Timer Interrupt Vector	X000100X	VV	Interrupt vector depends on user's system.
18.	Counter/Timer 1 Command and Status	X001010X	C0	Counter/Timer 1 Interrupt Enable.
19.	Counter/Timer 2's Mode Specification	X011101X	C2	Continuous, External Output Enable, Squarewave duty cycle.
20.	Counter/Timer 2's Time Constant MSBs	X011000X	00	
21.	Counter/Timer 2's Time Constant LSBs	X011001X	0A	Time Constant = $(10)_{10}$ for 5 μs timeout.
22.	Counter/Timer 3 Mode Specification	X011110X	80	Continuous, no external enable.
23.	Counter/Timer 3 Time Constant MSBs	X011010X	4E	Time Constant = $(20,000)_{10}$ for a 10 ms timeout.
24.	Counter/Timer 3's Time Constant LSBs	X011011X	20	
25.	Counter/Timer 3 Command and Status	X001100X	C0	Counter/Timer 3 Interrupt Enable.
26.	Master Configuration Control	X000001X	F4	Enable all ports and counter/timers.
27.	Counter/Timer 1 Command and Status	X001010X	06	Trigger and Gate commands.
28.	Counter/Timer 2 Command and Status	X001011X	06	Trigger and Gate commands.
29.	Counter/Timer 3 Command and Status	X001100X	06	Trigger and Gate commands.
30.	Master Interrupt Control	X000000X	8C	Master Interrupt Enable, Port B Vector Includes Status, Counter/Timer Vector Includes Status.