PRELIMINARY MILITARY PRODUCT SPECIFICATION

Z16C30

CMOS USC
UNIVERSAL SERIAL CONTROLLER

FEATURES

- Two independent, 0 to 10Mbit/sec, full duplex channels, each with two baud rate generators and Digital Phase-Locked Loop for clock recovery.
- 32 byte data FIFO's for each receiver and transmitter.
- 12.5 MByte/sec (16 bit) data bus bandwidth.
- Multi-protocol operation under program control with independent mode selection for receiver and transmitter.
- Async mode with one to eight bits/character, 1/16 to 2 stop bits/character in 1/16 bit increments; programmable clock factor; break detect and generation; odd, even, mark, space or no parity and framing error detection. Supports one Address/Data bit and MIL STD 1553B protocols.
- Byte oriented synchronous mode with one to eight bits/character; programmable idle line condition; optional receive sync stripping; optional preamble transmission; 16- or 32-bit CRC and transmit-to-receive slaving (for X.21).
- Bisync mode with 2- to 16-bit programmable sync characters; programmable idle line condition; optional receive sync stripping; optional preamble transmission; 16- or 32-bit CRC.
- Transparent Bisync mode with EBCDIC or ASCII character code; automatic CRC handling; programmable idle line condition; optional preamble transmission; automatic recognition of DLE, SYN, SOH, ITX, ETX, ETB, EOT, ENQ and ITB.
- External character sync mode for receive.
- HDLC/SDLC mode with eight bit address compare; extended address field option; 16- or 32-bit CRC; programmable idle line condition; optional preamble transmission and loop mode.
- DMA interface with separate request and acknowledge for each receiver and transmitter.
- Channel load command for DMA controlled initialization.
- Flexible bus interface for direct connection to most microprocessors; user programmable for 8- or 16-bits wide. Directly supports 680X0 family or 8X86 family bus interfaces.
- Low power CMOS.
- Improved Radiation Tolerance
- 68 pin PGA Package.

GENERAL DESCRIPTION

The USC Universal Serial Controller is a dual-channel multi-protocol data communications peripheral designed for use with any conventional multiplexed or non-multiplexed bus. The USC functions as a serial-to-parallel, parallel-to-serial converter/controller and may be software configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including two baud rate generators per channel, a digital phase-locked loop per channel, character counters for both receive and transmit in each channel and 32 byte data FIFO's for each receiver and transmitter.

The USC handles asynchronous formats, synchronous byte-oriented formats such as BISYNC and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The device can generate and check CRC in any synchronous mode and can be programmed to check data integrity in various modes. The USC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O. The same is true for most of the other pins in each channel.

GENERAL DESCRIPTION (Continued)

Interrupts are supported with a daisy-chain hierarchy, with the two channels having completely separate interrupt structures.

High-speed data transfers via DMA are supported by a Request/Acknowledge signal pair for each receiver and transmitter. The device supports automatic status transfer via DMA and also allows device initialization under DMA control.

To aid the designer in efficiently programming the USC, additional literature is available. The Technical Manual describes in detail all features presented in this Product Specification and gives programming sequence hints. The Programmer's Assistant is a MS-DOS disk based programming initialization tool to be used in conjunction with the Technical Manual. There are also available assorted application notes and development boards to assist the designer in the hardware/software development.

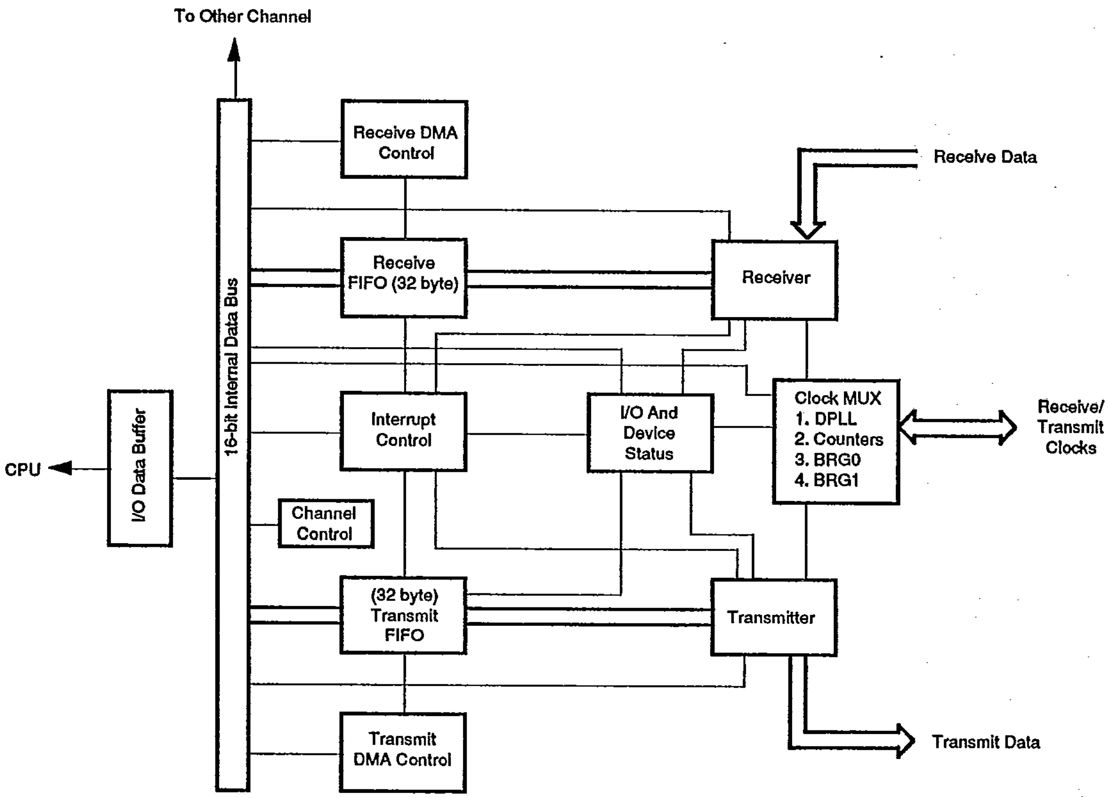


Figure 1. USC Block Diagram

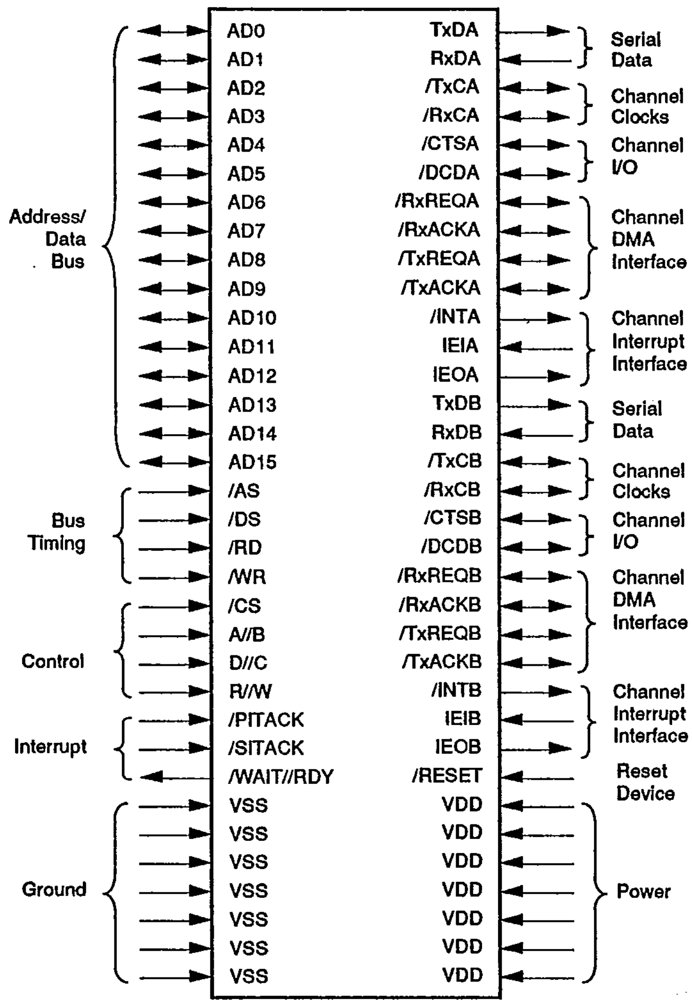


Figure 2. Pin Functions

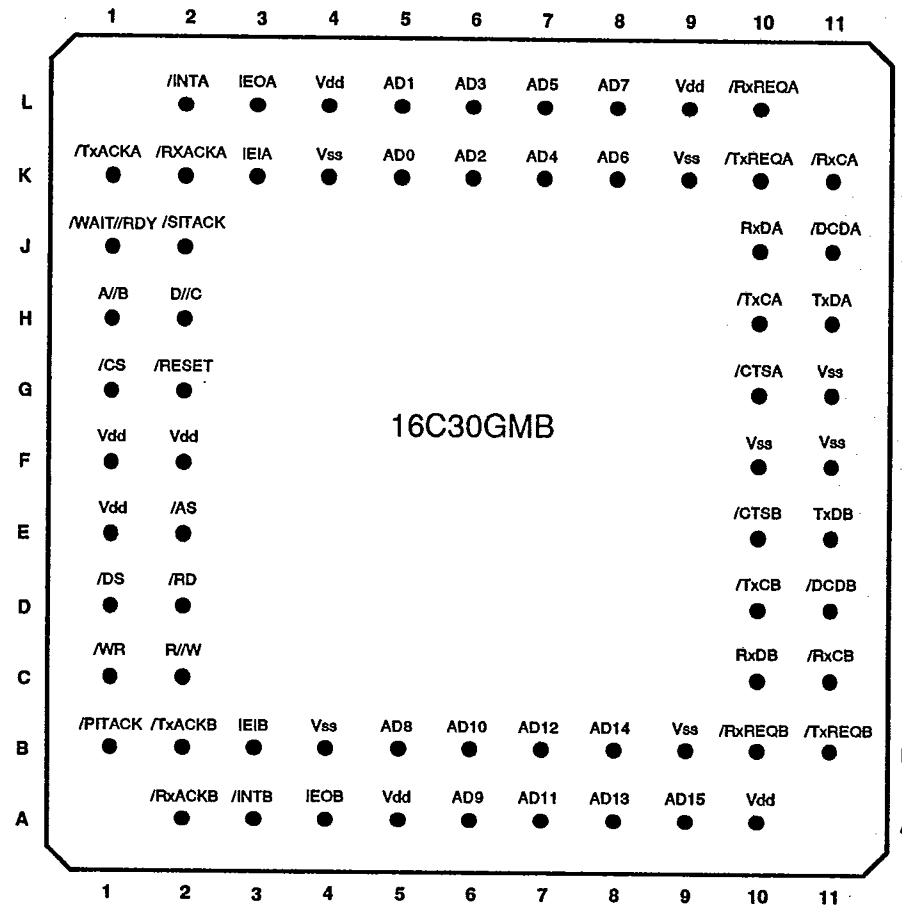


Figure 3. Pin Assignments

PIN DESCRIPTION

The device contains 13 pins per channel for channel I/O, 16 pins for address and data, 12 pins for CPU handshake and 14 pins for power and ground.

Three separate bus interface types are available for the device. The Bus Configuration Register (BCR) and external connections to the AD bus control selection of the bus type.

A 16-bit bus is selected by setting the BCR bit 2 to a 1.

The 8-bit bus is selected by setting BCR bit 2 to 0 and tying AD15 - AD8 to Vss.

The 8-bit bus with separate address, is selected by setting BCR bit 2 to 0. During the BCR write, AD15 is forced to a 1 and forcing AD14-AD8 to zero.

The multiplexed bus is selected for the USC if there is an Address Strobe prior to or during the transaction which writes the BCR.

If no Address Strobe is present prior to or during the transaction which writes the BCR, a non-multiplexed bus is selected (See Figure 6).

The section below describes in detail the USC pin assignment.

/RESET. *Reset* (input, active Low). This signal resets the device to a known state. The first write to the USC after a reset accesses the BCR to select additional bus options for the device.

/AS. *Address Strobe* (input, active Low). This signal is used in the multiplexed bus modes to latch the address on the AD lines. The AS signal is not used in the non-multiplexed bus modes and should be tied to V_{DD} in these cases.

/DS. *Data Strobe* (input, active Low). This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle. DS also strobes data into the device during the active state of R/W.

/RD. *Read Strobe* (input, active Low). This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle.

/WR. *Write Strobe* (input, active Low). This signal strobes data into the device during a write.

R/W. *Read/Write* (input). This signal determines the direction of data transfer for a read or write cycle in conjunction with DS.

/CS. *Chip Select* (input, active Low). This signal selects the device for access and must be asserted for read and write cycles, but is ignored during interrupt acknowledge and fly-by DMA transfers. In the case of a multiplexed bus interface, CS is latched by the rising edge of AS.

A//B. *Channel A/Channel B Select* (input). This signal selects between the two channels in the device. High selects channel A and Low selects channel B.

This signal is sampled and the result is latched during the BCR (Bus Configuration Register) write. It programs the sense of the /WAIT//RDY signal appropriate for different bus interfaces. See /WAIT//RDY below.

D//C. *Data/Control Select* (input). This signal, when High, provides for direct access to the RDR and TDR. In the case of a multiplexed bus interface, D//C High overrides the address provided to the device.

/SITACK. *Status Interrupt Acknowledge* (input, active Low). This signal is a status signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle. This signal is compatible with 680x0 family microprocessors.

/PITACK. *Pulsed Interrupt Acknowledge* (input, active Low). This is a strobe signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle.

PITACK may be programmed to accept a single pulse or double pulse acknowledge type. This programming is done in the BCR. With the double pulse type selected, the first PITACK is recognized but no action takes place. The interrupt vector is returned on the second pulse if the no vector option is not selected. The double pulse type is compatible with 8x86 family microprocessors.

/WAIT//RDY. */Wait Data Ready* (output, active Low). This signal indicates when the data is available during a read cycle, when the device is ready to receive data during a write cycle, and when a valid vector is available during an interrupt acknowledge cycle. It may be programmed to function either as a Wait signal or a Ready signal using the state of the A//B pin during the BCR write. When A//B is High during the BCR write, this signal functions as a wait output and thus supports the READY function of 8X86 family microprocessors. When A//B is Low during the BCR write, this signal functions as a ready output and thus supports the DTACK function of 680X0 family microprocessors.

AD15-AD0. *Address/Data Bus* (bidirectional, active High, 3-state). The AD signals carry addresses to, and data to and from, the device. When the 16-bit non-multiplexed bus is selected, AD15-0 carry data to and from the device. Addresses are provided using a pointer within the device that is loaded with the desired register address. When the 8-bit non-multiplexed bus is selected without separate address, only AD7-0 are used to transfer data. The pointer is used for addressing; AD15-8 are unused.

When the 8-bit non-multiplexed bus is selected with separate address, AD7-0 are used to transfer data, while AD15-8 are used as an address bus. When the 16-bit multiplexed bus is selected, addresses are latched from AD7-0 and data transfers are sixteen bits wide. When the 8-bit multiplexed bus is selected without separate address, only AD7-0 are used to transfer addresses and data; AD15-8 are unused. When the 8-bit multiplexed bus with separate address is selected, only AD7-0 are used to transfer data, while AD15-8 are used as an address bus.

/INTA, /INTB. *Interrupt Request* (outputs, active Low). These signals indicate that the channel has an interrupt condition pending and is requesting service. These outputs are NOT open-drain.

IEIA, IEIB. *Interrupt Enable In* (inputs, active High). The IEI signal for each channel is used with the accompanying IEO signal to form an interrupt daisy chain. An active IEI indicates that no device having higher priority is requesting or servicing an interrupt.

IEOA, IEOB. *Interrupt Enable Out* (outputs, active High). The IEO signal for each channel is used with the accompanying IEI signal to form an interrupt daisy chain. IEO is Low if IEI is Low, an interrupt is under service in the channel, or an interrupt is pending during an interrupt acknowledge cycle.

/TxACKA, /TxACKB. *Transmit Acknowledge* (inputs or outputs, active Low). The primary function of these signals is to perform fly-by DMA transfers to the transmit FIFOs. Also, they can be used as bit inputs or outputs.

/RxACKA, /RxACKB. *Receive Acknowledge* (inputs or outputs, active Low). The primary function of these signals is to perform fly-by DMA transfers from the receive FIFOs. Also, they can be used as bit inputs or outputs.

TxDA, TxDB. *Transmit Data* (outputs, active High, 3-state). These signals carry the serial transmit data for each channel.

RxDA, RxDB. *Receive Data* (inputs, active High). These signals carry the serial receive data for each channel.

/TxCA, /TxCB. *Transmit Clock* (inputs or outputs, active Low). These signals are used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various transmitter signals or internal clock signals.

/RxCA, /RxCB. *Receive Clock* (inputs or outputs, active Low). These signals are used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various receiver signals or internal clock signals.

/TxREQA, /TxREQB. *Transmit Request* (inputs or outputs, active Low). The primary function of these signals is to request DMA transfers to the transmit FIFOs. They may also be used as simple inputs or outputs.

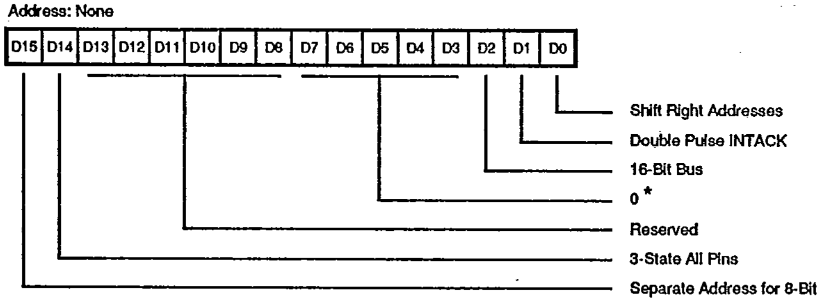
/RxREQA, /RxREQB. *Receive Request* (inputs or outputs, active low). The primary function of these signals is to request DMA transfers from the receive FIFOs. They may also be used as simple inputs or outputs.

/CTSA, /CTSB. *Clear To Send* (inputs or outputs, active Low). These signals are used as enables for the respective transmitters. They may also be programmed to generate interrupts on either transition or used as simple inputs or outputs.

/DCDA, /DCDB. *Data Carrier Detect* (inputs or outputs, active Low). These signals are used as enables for the respective receivers. Also, they may be programmed to generate interrupts on either transition or used as simple inputs or outputs.

ARCHITECTURE

The USC internal structure includes two completely independent full-duplex serial channels, each with two baud rate generators, a digital phase-locked loop for clock recovery, transmit and receive character counters and a full-duplex DMA interface. The two serial channels share a common bus interface. The bus interface is designed to provide easy interface to most microprocessors, whether they employ a multiplexed, non-multiplexed, 8-bit or 16-bit bus structure. Each channel is controlled by a set of thirty 16-bit registers, nearly all of which are readable and writable. There is one additional 16-bit register in the bus interface used to configure the nature of the bus interface. The BCR functions are shown in Figure 4.



* Must be programmed as 0.

Figure 4. Bus Configuration Register

DATA PATH

Both the transmitter and the receiver in the channel are actually microcoded serial processors. As the data shifts through the transmit or receive shift register, the microcode watches for specific bit patterns, counts bits, and at the appropriate time transfers data to or from the FIFOs. The microcode also checks status and generates status interrupts as appropriate.

FUNCTIONAL DESCRIPTION

The functional capabilities of the USC are described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, the USC offers such features as read/write registers, a flexible bus interface, DMA interface support and vectored interrupts.

Data Communications Capabilities

The USC provides two independent full-duplex channels programmable for use in any common data communication protocol. The receiver and transmitter modes are completely independent, as are the two channels. Each receiver and transmitter is supported by a 32-byte deep FIFO and a 16-bit message length counter. All modes allow optional even, odd, mark or space parity. Synchronous modes allow the choice of two 16-bit or one 32-bit CRC polynomial.

Selection of from one to eight bits-per-character is available in both receiver and transmitter, independently. Error and status conditions are carried with the data in the receive and transmit FIFOs to greatly reduce the CPU overhead required to send or receive a message. Specific, appropriately timed interrupts are available to signal such conditions as overrun, parity error, framing error, end-of-frame, idle line received, sync acquired, transmit under-run, CRC sent, closing sync/flag sent, abort sent, idle line sent and preamble sent. In addition, several useful internal signals such as receive FIFO load, received sync, transmit FIFO read and transmission complete may be sent to pins for use by external circuitry.

Asynchronous Mode. The receiver and transmitter can handle data at a rate of 1/16, 1/32, or 1/64 the clock rate. The receiver rejects start bits less than one-half a bit time and will not erroneously assemble characters following a framing error. The transmitter is capable of sending one, two, or anywhere in the range of 1/16th to two stop bits per character in 1/16 bit increments.

External Sync Mode. The receiver is synchronized to the receive data stream by an externally-supplied signal on a pin for custom protocol applications.

Isochronous Mode. Both transmitter and receiver may operate on start-stop (async) data using a 1x clock. The transmitter can send one or two stop bits.

Asynchronous With Code Violations. This is similar to Isochronous mode except that the start bit is replaced by a three bit-time code violation pattern as in MIL-STD 1553B. The transmitter can send zero, one or two stop bits.

FUNCTIONAL DESCRIPTION (Continued)

Asynchronous With Code Violations. This is similar to Isochronous mode except that the start bit is replaced by a three bit-time code violation pattern as in MIL-STD 1553B. The transmitter can send zero, one or two stop bits.

Monosync Mode. In this mode, a single character is used for synchronization. The character can either be eight bits long with an arbitrary data character length, or the sync character length may be programmed to match the data character length. The receiver is capable of automatically stripping sync characters from the received data stream. The transmitter may be programmed to automatically send CRC on either an underrun or at the end of a programmed message length.

Bisync Mode. This mode is identical to monosync mode except that character synchronization requires two successive characters for synchronization. The two characters need not be identical.

HDLC Mode. In this mode, the receiver recognizes flags, performs optional address matching, accommodates extended address fields, 8- or 16-bit control fields and logical control fields, performs zero deletion and CRC checking. The receiver is capable of receiving shared-zero flags, recognizes the abort sequence and can receive arbitrary length messages. The transmitter automatically sends opening and closing flags, performs zero insertion and can be programmed to send an abort, an extended abort, a flag or CRC and a flag on transmit underrun. Also, the transmitter automatically sends the closing flag with optional CRC at the end of a programmed message length. Shared-zero flags are selected in the transmitter and a separate character length may be programmed for the last character in the frame.

Bisync Transparent Mode. In this mode, the synchronization pattern is DLE-SYN, programmable selected from either ASCII or EBCDIC encoding. The receiver recognizes control character sequences and automatically handles CRC calculations without CPU intervention. The transmitter can be programmed to send either SYN, DLE-SYN, CRC-SYN, or CRC-DLE-SYN upon underrun and can automatically send the closing DLE-SYN with optional CRC at the end of a programmed message length.

NBIP Mode. This mode is identical to async except that the receiver checks for the status of an additional address/data bit between the parity bit and the stop bit. The value of this bit is FIFO'ed along with the data. This bit is automatically inserted in the transmitter with the value that is FIFO'ed with the transmit data.

802.3 Mode. This mode implements the data format of IEEE 802.3 with 16-bit address compare. In this mode, DCD and CTS are used to implement the carrier sense and collision detect interactions with the receiver and transmitter.

Slaved Monosync Mode. This mode is available only in the transmitter and allows the transmitter (operating as though it were in monosync mode) to send data that is byte-synchronous to the data being received by the receiver.

HDLC Loop Mode. This mode is also available only in the transmitter and allows the USC to be used in an HDLC loop configuration. In this mode, the receiver is programmed to operate in HDLC mode so that the transmitter echos received messages. Upon receipt of a particular bit pattern (actually a sequence of seven consecutive ones) the transmitter breaks the loop and inserts its own frame(s).

Data Encoding

The USC may be programmed to encode and decode the serial data in any of eight different ways as shown in Figure 5. The transmitter encoding method is selected independently of the receiver decoding method.

NRZ. In NRZ, 1 is represented by a high level for the duration of the bit cell and a 0 is represented by a Low level for the duration of the bit cell.

NRZB. Data is inverted from NRZ.

NRZI-Mark. In NRZI-Mark, 1 is represented by a transition at the beginning of the bit cell. That is, the level present in the preceding bit cell is reversed. A 0 is represented by the absence of a transition at the beginning of the bit cell.

NRZI-Space. In NRZI-Space, 1 is represented by the absence of a transition at the beginning of the bit cell. That is, the level present in the preceding bit cell is maintained. A 0 is represented by a transition at the beginning of the bit cell.

Biphase-Mark. In Biphase-Mark, 1 is represented by a transition at the beginning of the bit cell and another transition at the center of the bit cell. A 0 is represented by a transition at the beginning of the bit cell only.

Biphase-Space. In Biphase-Space, 1 is represented by a transition at the beginning of the bit cell only. A 0 is represented by a transition at the beginning of the bit cell and another transition at the center of the bit cell.

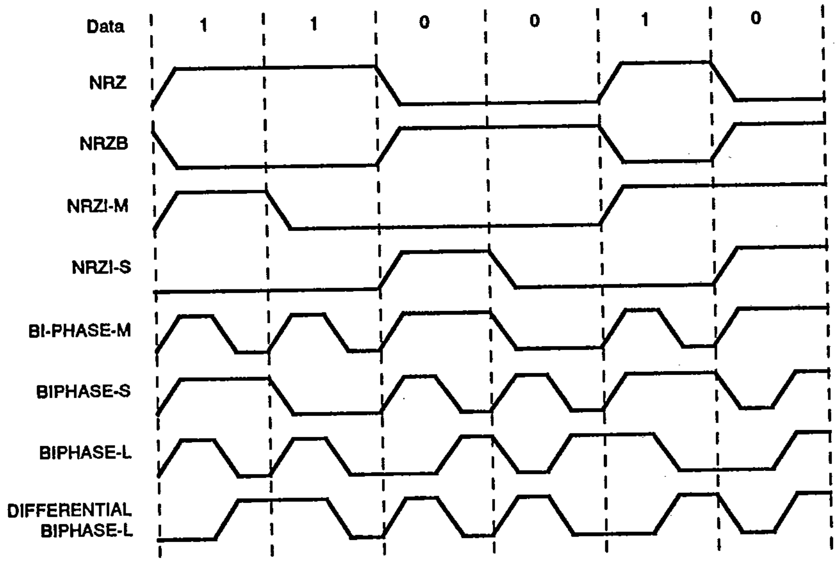


Figure 5. Data Encoding

Biphase-Level. In Biphase-Level, 1 is represented by a High during the first half of the bit cell and a Low during the second half of the bit cell. A 0 is represented by a Low during the first half of the bit cell and a High during the second half of the bit cell.

Differential Biphase-level. In Differential Biphase-Level, 1 is represented by a transition at the center of the bit cell, with the opposite polarity from the transition at the center of the preceding bit cell. A 0 is represented by a transition at the center of the bit cell with the same polarity as the transition at the center of the preceding bit cell. In both cases there may be transitions at the beginning of the bit cell to set up the level required to make the correct center transition.

Character Counters

Each channel in the USC contains a 16-bit character counter for both receiver and transmitter. The receive character counter may be preset either under software control or automatically at the beginning of a receive message. The counter decrements with each receive character and at the end of the receive message the current value in the counter is automatically loaded into a four-deep FIFO. This allows DMA transfer of data to proceed without CPU intervention at the end of a message, as the values in the FIFO allow the CPU to determine message boundaries in memory. Similarly, the transmit character counter is loaded either under software control or automatically at the beginning of a transmit message. The counter is decremented with each write to the transmit FIFO. When the counter has decremented to zero, and that byte is sent, the transmitter automatically terminates the message in the appropriate fashion (usually CRC and the closing flag or sync character) without requiring CPU intervention.

Baud Rate Generators

Each channel in the USC contains two baud generators. Each generator consists of a 16-bit time constant register and a 16-bit down counter. In operation, the counter decrements with each baud rate generator clock, with the time constant automatically reloaded when the count reaches zero. The output of the baud rate generator toggles when the counter reaches a count of one-half of the time constant and again when the counter reaches zero. A new time constant may be written at any time but the new value will not take effect until the next load of the counter. The outputs of both baud rate generators are sent to the clock multiplexer for use internally or externally. The baud rate generator output frequency is related to the baud rate generator input clock frequency by the following formula:

Output frequency =
Input frequency/(time constant + 1)

This allows an output frequency in the range of 1 to 1/65536 of the input frequency, inclusive.

FUNCTIONAL DESCRIPTION (Continued)

Digital Phase-Locked Loop
Each channel in the USC contains a Digital Phase-Locked Loop (DPLL) to recover clock information from a data stream with NRZI or Biphase encoding. The DPLL is driven by a clock that is nominally 8, 16 or 32 times the receive data rate. The DPLL uses this clock, along the data stream, to construct a clock for the data. This clock may then be routed to the receiver, transmitter, or both, or to a pin for use externally. In all modes the DPLL counts the input clock to create nominal bit times. As the clock is counted, the DPLL watches the incoming data stream for transitions. Whenever a transition is detected, the DPLL makes a count adjustment (during the next counting cycle), to produce an output clock which tracks the incoming bit cells. The DPLL provides properly phased transmit and receive clocks to the clock multiplexer.

Counters
Each channel contains two 5-bit counters, which are programmed to divide an input clock by 4, 8, 16 or 32. The inputs of these two counters are sent to the clock multiplexer. The counters are used as prescalers for the baud rate generators, or to provide a stable transmit clock from a common source when the DPLL is providing the receive clock.

Clock Multiplexer
The clock multiplexer in each channel selects the clock source for the various blocks in the channel and selects an internal clock signal to potentially be sent to either the RxC or TxC pin.

Test Modes
The USC is programmed for local loopback or auto echo operation. In local loopback, the output of the transmitter is internally routed to the input of the receiver. This allows testing of the USC data paths without any external logic. Auto echo connects the RxD pin directly to the TxD pin. This is useful for testing serial links external to the USC.

I/O Interface Capabilities
The USC offers the choice of polling, interrupt (vectored or non-vectored) and block transfer modes to transfer data, status and control information to and from the CPU.

Polling. All interrupts are disabled. The registers in the USC are automatically updated to reflect current status. The CPU polls the Daisy Chain Control Register (DCCR) to determine status changes and then reads the appropriate status register to find and respond to the change in status. USC status bits are grouped according to function to simplify this software action.

Interrupt. When a USC responds to an interrupt acknowledge from the CPU, an interrupt vector may be placed on the data bus. This vector is held in the Interrupt Vector Register (IVR). To speed interrupt response time, the USC modifies three bits in this vector to indicate which type of interrupt is being requested.

Each of the six sources of interrupts in each channel of the USC (Receive Status, Receive Data, Transmit Status, Transmit Data, I/O Status and Device Status) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt-Under-Service (IUS) and Interrupt Enable (IE). If the IE bit for a given source is set, that source can request interrupts. Note that individual sources within the six groups also have interrupt enable bits which are set for the particular source. In addition, there is a Master Interrupt Enable (MIE) bit in each channel which globally enables or disables interrupts within the channel.

The other two bits are related to the interrupt priority chain. A channel in the USC may request an interrupt only when no higher priority interrupt source is requesting one, e.g., when IEI is High for the channel. In this case, the channel activates the INT signal. The CPU then responds with an interrupt acknowledge cycle, and the interrupting channel places a vector on the data bus.

In the USC, the IP bit signals that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority within the channel and external to the channel are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the channel being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an interrupt acknowledge cycle if there are no higher priority devices requesting interrupts.

There are six sources of interrupt in each channel: Receive Status, Receive Data, Transmit Status, Transmit Data, I/O Status and Device Status, prioritized in that order within the channel. There are six sources of Receive Status interrupt, each individually enabled: exited hunt, idle line, break/abort, code violation/end-of-transmission/end-of-frame, parity error and overrun error. The Receive Data interrupt is generated whenever the receive FIFO fills with data beyond the level programmed in the Receive Interrupt Control Register (RICR).

There are six sources of Transmit Status interrupt, each individually enabled: preamble sent, idle line sent, abort sent, end-of-frame/end-of-transmission sent, CRC sent and underrun error. The Transmit Data interrupt is generated whenever the transmit FIFO empties below the level programmed in the Transmit Interrupt Control Register (TICR). The I/O Status interrupt serves to report transitions on any of six pins. Interrupts are generated on either or both edges with separate selection and enables for each pin. The pins programmed to generate I/O Status interrupts are /RxC, /TxC, /RxREQ, /TxREQ, /DCD and /CTS. These interrupts are independent of the programmed function of the pins. The Device Status interrupt has four separately enabled sources: receive character count FIFO overflow, DPLL sync acquired, BRG1 zero count and BRGO zero count.

Block Transfer Mode. The USC accommodates block transfers via DMA through the /RxREQ, /TxREQ, /RxACK and /TxACK pins. The /RxREQ signal is activated when the fill level of the receive FIFO exceeds the value programmed in the RICR. The DMA may respond with either a normal bus transaction or by activating the /RxACK pin to read the data directly (fly-by transfer). The /TxREQ signal is activated when the empty level of the transmit FIFO falls below the value programmed in the TICR. The DMA may respond either with a normal bus transaction or by activating the /TxACK pin to write the data directly (fly-by transfer). The /RxACK and /TxACK pin functions for this mode are controlled by the Hardware Configuration Register (HCR). Then using the /RxACK and /TxACK pins to transfer data, no chip select is necessary; these are dedicated strobes for the appropriate FIFO.

PROGRAMMING

The Programmers Assistant (MS DOS based) and Technical Manual are available to provide details about programmming the USC. Also included are explanations and features of all registers in the USC.

The registers in each USC channel are programmed by the system to configure the channels. Before this can occur, however, the system must program the bus interface by writing to the Bus Configuration Register (BCR). The BCR has no specific address and is only accessible immediately after a hardware reset of the device. The first write to the USC, after a hardware reset, programs the BCR. From that time on the normal channel registers may be accessed. No specific address need be presented to the USC for the BCR write; the USC knows that the first write after a hardware reset is destined for the BCR.

In the multiplexed bus case, all registers are directly addressable via the address latched by /AS at the beginning of a bus transaction. The address is decoded from either AD6-AD0 or AD7-AD1. This is controlled by the Shift Right/Shift Left bit in the BCR. The address maps for these two cases are shown in Table 1. The D//C pin is still used to directly access the receive and transmit data registers (RDR and TDR) in the multiplexed bus; if D//C is High the address latched by /AS is ignored and an access of RDR or TDR is performed.

In the non-multiplexed bus case, the registers in each channel are accessed indirectly using the address pointer in the Channel Command/Address Register (CCAR) in each channel. The address of the desired register is first written to the CCAR and then the selected register is accessed; the pointer in the CCAR is automatically cleared after this access. The RDR and TDR are accessed directly using the D//C pin, without disturbing the contents of the pointer in the CCAR.

Table 1. Multiplexed Bus Address Assignments

Address Signal	Shift Left	Shift Right
Byte/Word *Access	AD7	AD6
Address 4	AD6	AD5
Address 3	AD5	AD4
Address 2	AD4	AD3
Address 1	AD3	AD2
Address 0	AD2	AD1
Upper/Lower *Byte Select	AD1	AD0

There are two important things to note about the USC. First, the Channel Reset bit in the CCAR places the channel in the reset state. To exit this reset state either a word of all zeros must be written to the CCAR (16-bit bus) or a byte of all zeros must be written to the lower byte of the CCAR (8-bit bus). The second thing to note is that after reset, the transmit and receive clocks are not connected. The first thing that should be done in any initialization sequence is a write to the Clock Mode Control Register (CMCR) to select a clock source for the receiver and transmitter.

The register addressing is shown in Table 2. and the bit assignments for the registers are shown in Figure 6.

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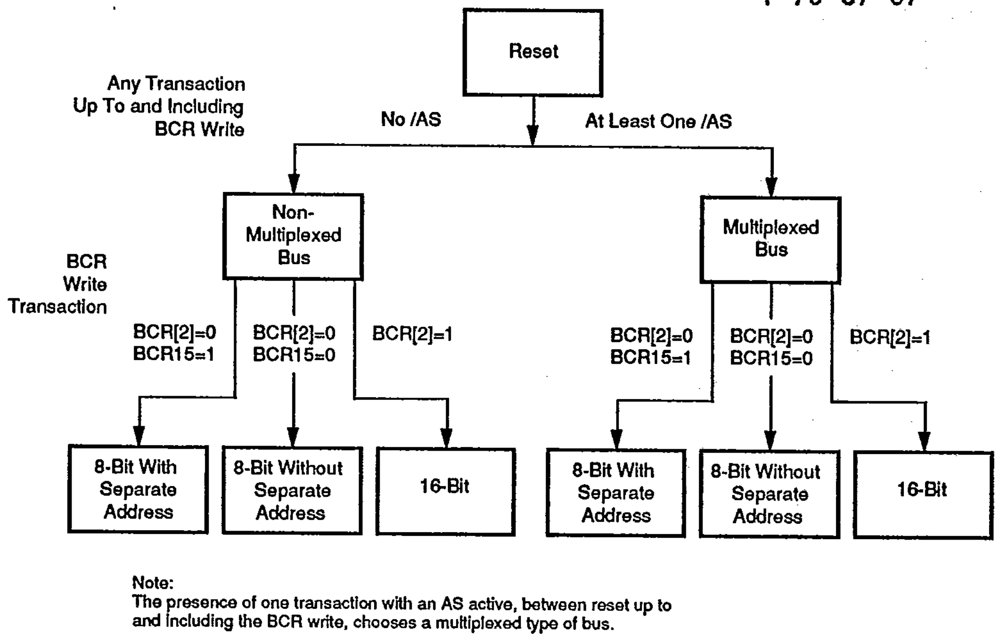

Figure 6. BCR Reset Sequence and Bit Assignments

Table 2. Register Address List

Address 43210			Address 43210		
00000	CCAR	Channel Command/Address Register	10010	RCSR	Receive Command/Status Register
00001	CMR	Channel Mode Register	10011	RICR	Receive Interrupt Control Register
00010	CCSR	Channel Command/Status Register	10100	RSR	Receive Sync Register
00011	CCR	Channel Control Register	10101	RCLR	Receive Count Limit Register
00110	TMDR	Test Mode Data Register	10110	RCCR	Recieve Character Count Register
00111	TMCR	Test Mode Control Register	10111	TC0R	Time Constant 0 Register
01000	CMCR	Clock Mode Control Register	1X000	TDR	Transmit Data Register (Write Only)
01001	HCR	Hardware Configuration Register	11001	TMR	Transmit Mode Register
01010	IVR	Interrupt Vector Register	11010	TCSR	Transmit Command/Status Register
01011	IOCR	I/O Control Register	11011	TICR	Transmit Interrupt Control Register
01100	ICR	Interrupt Control Register	11100	TSR	Transmit Sync Register
01101	DCCR	Daisy-chain Control Register	11101	TCLR	Transmit Count Limit Register
01110	MISR	Misc Interrupt Status Register	11110	TCCR	Transmit Character Count Register
01111	SICR	Status Interrupt Control Register	11111	TC1R	Time Constant 1 Register
1X000	RDR	Receive Data Register (Read Only)			
10001	RMR	Receive Mode Register	XXXXX	BCR	Bus Configuration Register

REGISTERS

Address: 00000

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

- D0: Upper//Lower Byte Select (W0)
- D1: Address 0 (W0)
- D2: Address 1 (W0)
- D3: Address 2 (W0)
- D4: Address 3 (W0)
- D5: Address 4 (W0)
- D6: Byte/Word Access (W0)
- D7: DMA Continue (W0)
- D10: Channel Reset

Mode Control (D9, D8):

D9	D8	Mode Control
0	0	Normal Operation
0	1	Auto Echo
1	0	External Local Loopback
1	1	Internal Local Loopback

Channel Command (W0) (D15–D11):

D15	D14	D13	D12	D11	Channel Command (W0)
0	0	0	0	0	Null Command
0	0	0	0	1	Reserved
0	0	0	1	0	Reset Highest IUS
0	0	0	1	1	Reserved
0	0	1	0	0	Trigger Channel Load DMA
0	0	1	0	1	Trigger Rx DMA
0	0	1	1	0	Trigger Tx DMA
0	0	1	1	1	Trigger Rx & Tx DMA
0	1	0	0	0	Reserved
0	1	0	0	1	Rx FIFO Purge
0	1	0	1	0	Tx FIFO Purge
0	1	0	1	1	Rx & Tx FIFO Purge
0	1	1	0	0	Reserved
0	1	1	0	1	Reload Rx Character Count
0	1	1	1	0	Reload Tx Character Count
0	1	1	1	1	Reload Rx & Tx Character Count
1	0	0	0	0	Reserved
1	0	0	0	1	Load TC0
1	0	0	1	0	Load TC1
1	0	0	1	1	Load TC0 & TC1
1	0	1	0	0	Select Serial Data LSB First *
1	0	1	0	1	Select Serial Data MSB First
1	0	1	1	0	Select Straight Memory Data *
1	0	1	1	1	Select Swapped Memory Data
1	1	0	0	0	Reserved
1	1	0	0	1	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

* Selected Upon Reset

Figure 7. Channel Command/Address Register

Address: 00001

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Receiver Mode (D3–D0)

D3	D2	D1	D0	Mode
0	0	0	0	Asynchronous
0	0	0	1	External Synchronous
0	0	1	0	Isochronous
0	0	1	1	Asynchronous with CV
0	1	0	0	Monosync
0	1	0	1	Bisync
0	1	1	0	HDLC
0	1	1	1	Transparent Bisync
1	0	0	0	NBIP
1	0	0	1	802.3
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

- D4: Rx Submode 0
- D5: Rx Submode 1
- D6: Rx Submode 2
- D7: Rx Submode 3

Transmitter Mode (D11–D8)

D11	D10	D9	D8	Mode
0	0	0	0	Asynchronous
0	0	0	1	Reserved
0	0	1	0	Isochronous
0	0	1	1	Asynchronous with CV
0	1	0	0	Monosync
0	1	0	1	Bisync
0	1	1	0	HDLC
0	1	1	1	Transparent Bisync
1	0	0	0	NBIP
1	0	0	1	802.3
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Slaved Monosync
1	1	0	1	Reserved
1	1	1	0	HDLC Loop
1	1	1	1	Reserved

- D12: Tx Submode 0
- D13: Tx Submode 1
- D14: Tx Submode 2
- D15: Tx Submode 3

Figure 8. Channel Mode Register

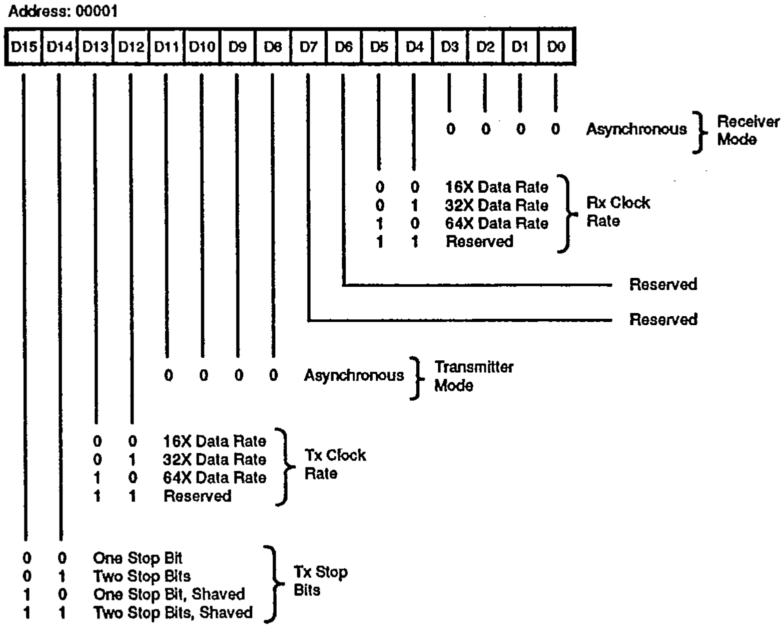

Figure 9. Channel Mode Register, Asynchronous Mode

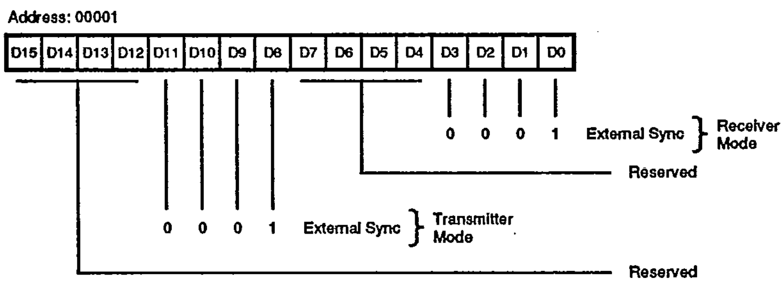

Figure 10. Channel Mode Register, External Sync Mode

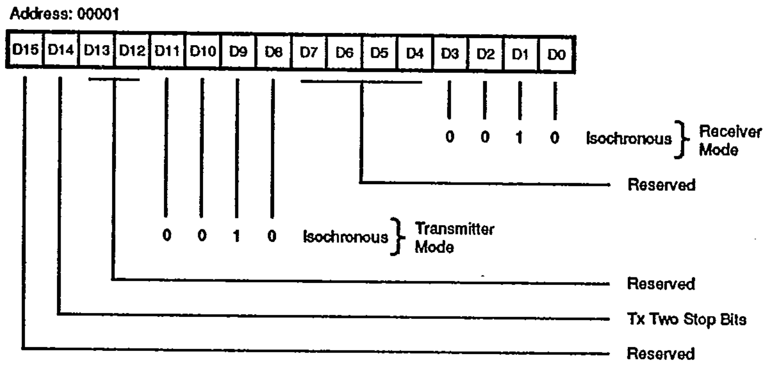

Figure 11. Channel Mode Register, Isochronous Mode

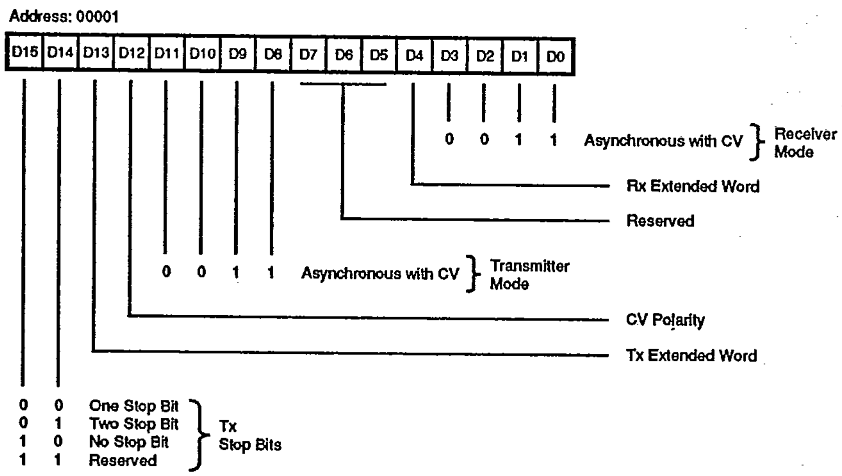

Figure 12. Channel Mode Register, Asynchronous Mode with Code Violation (MIL STD 1553)

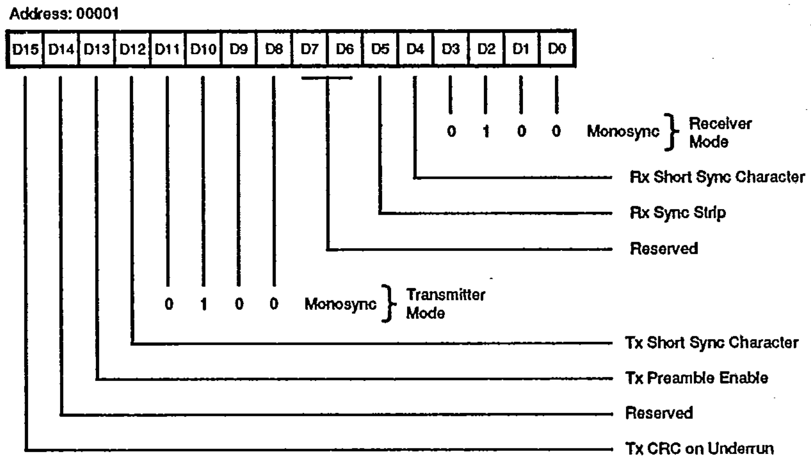

Figure 13. Channel Mode Register, Monosync Mode

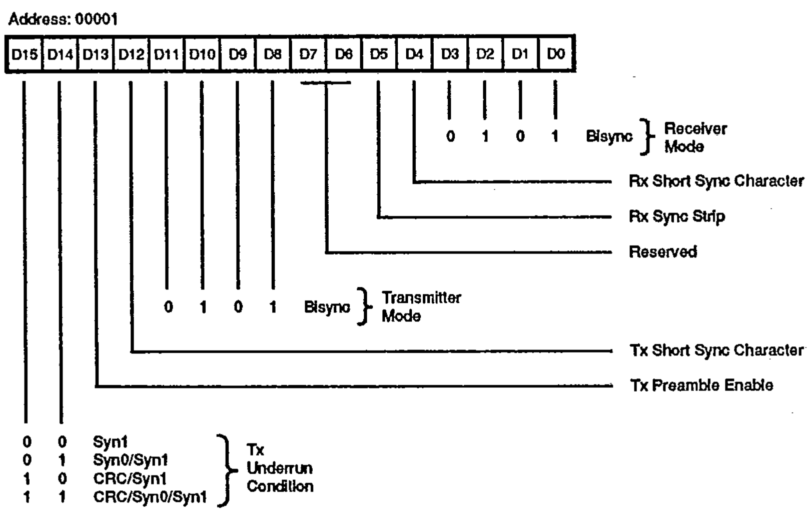

Figure 14. Channel Mode Register, Bisync Mode

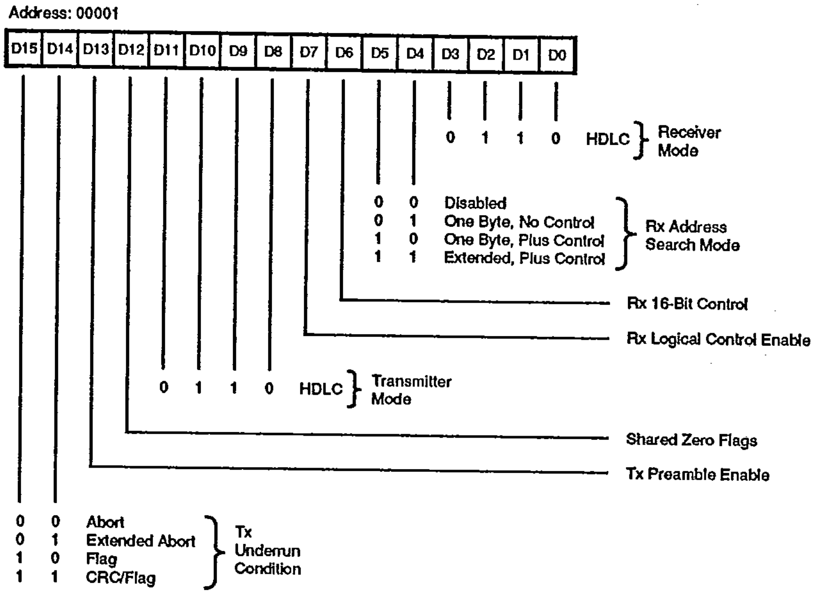

Figure 15. Channel Mode Register, HDLC Mode

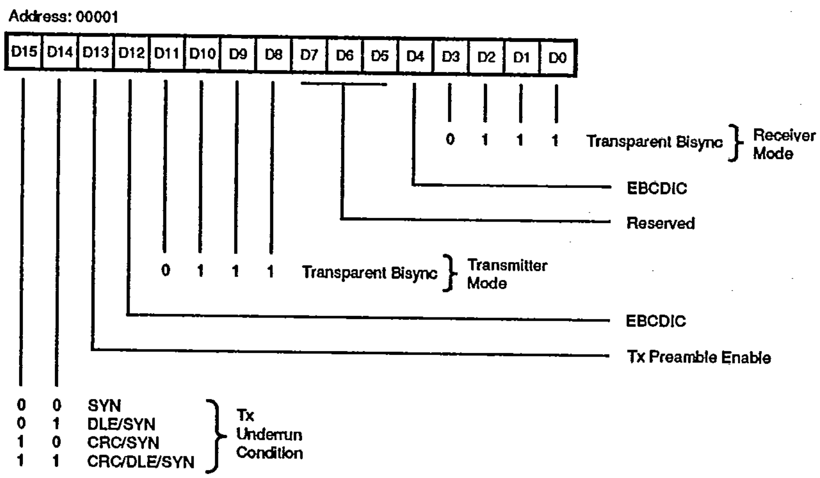

Figure 16. Channel Mode Register, Transparent Bisync Mode

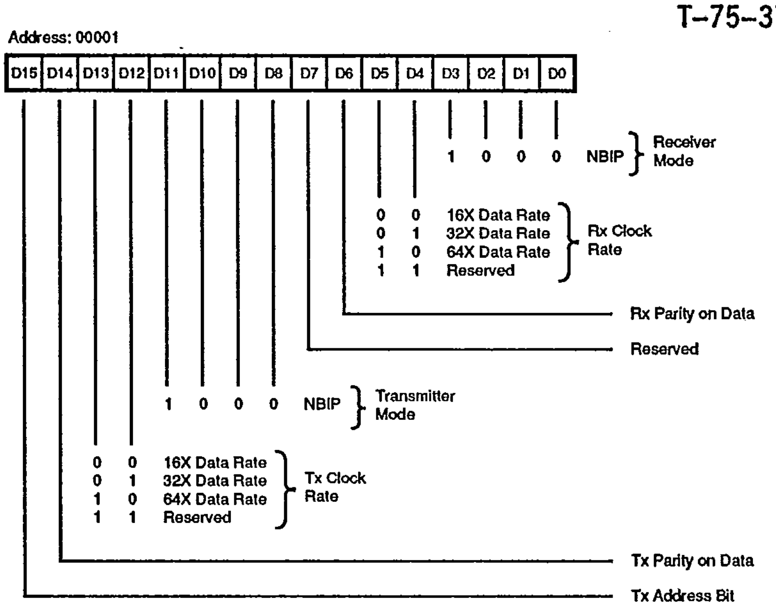

Figure 17. Channel Mode Register, NBIP Mode

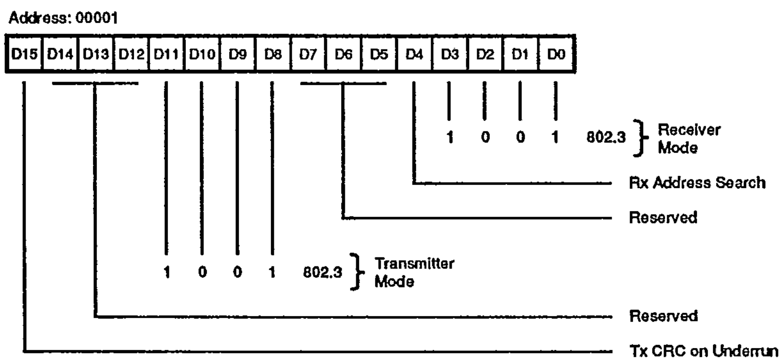

Figure 18. Channel Mode Register, 802.3 Mode

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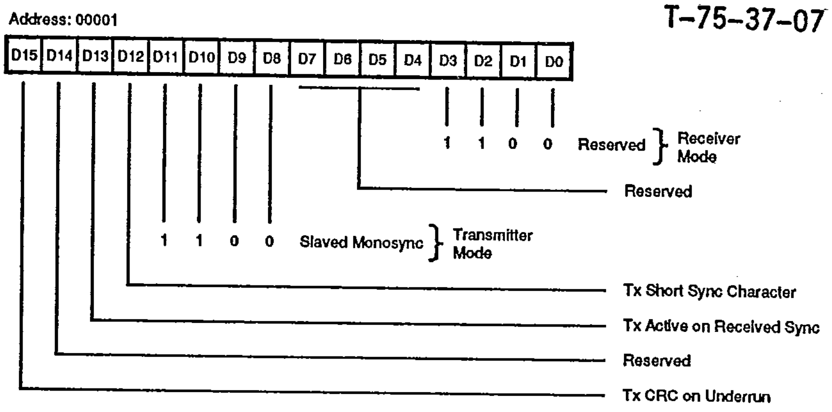

Figure 19. Channel Mode Register, Slaved Monosync Mode

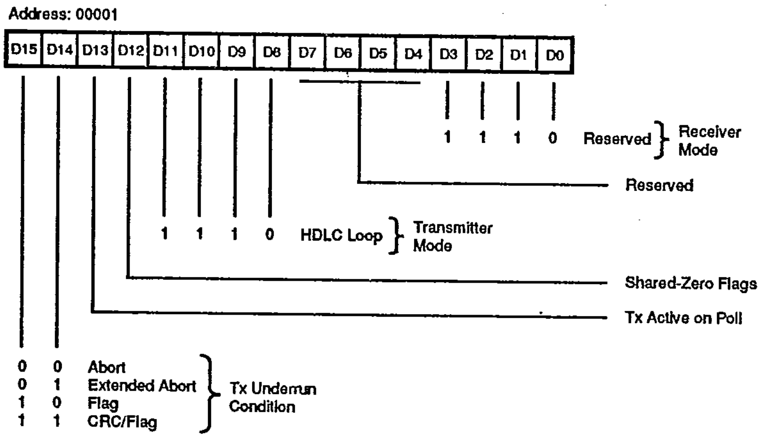

Figure 20. Channel Mode Register, HDLC Loop Mode

T-75-37-07

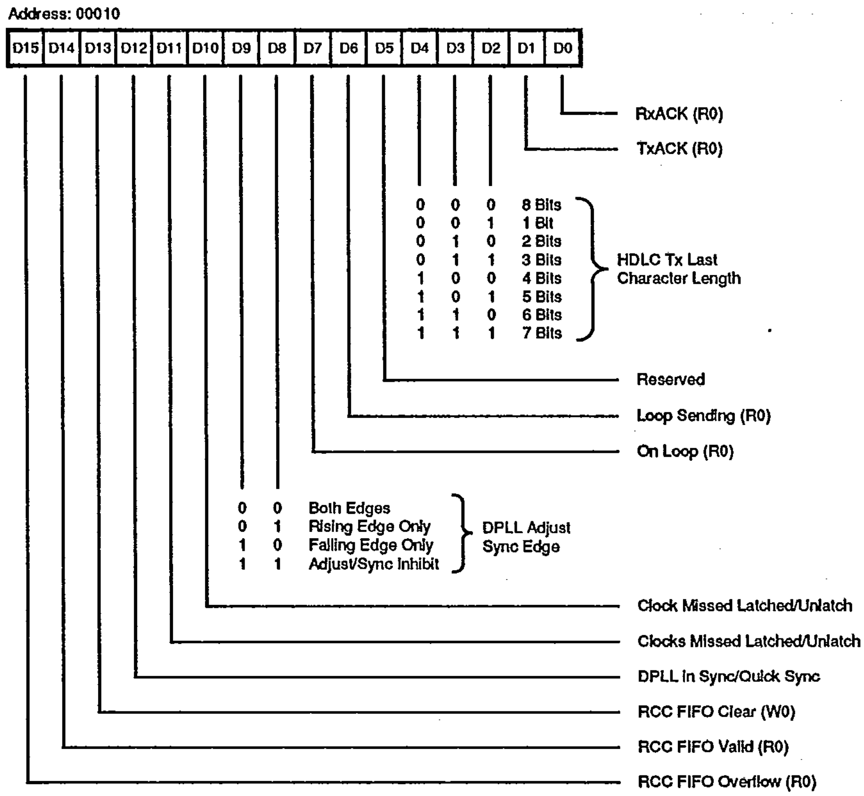

Figure 21. Channel Command/Status Register

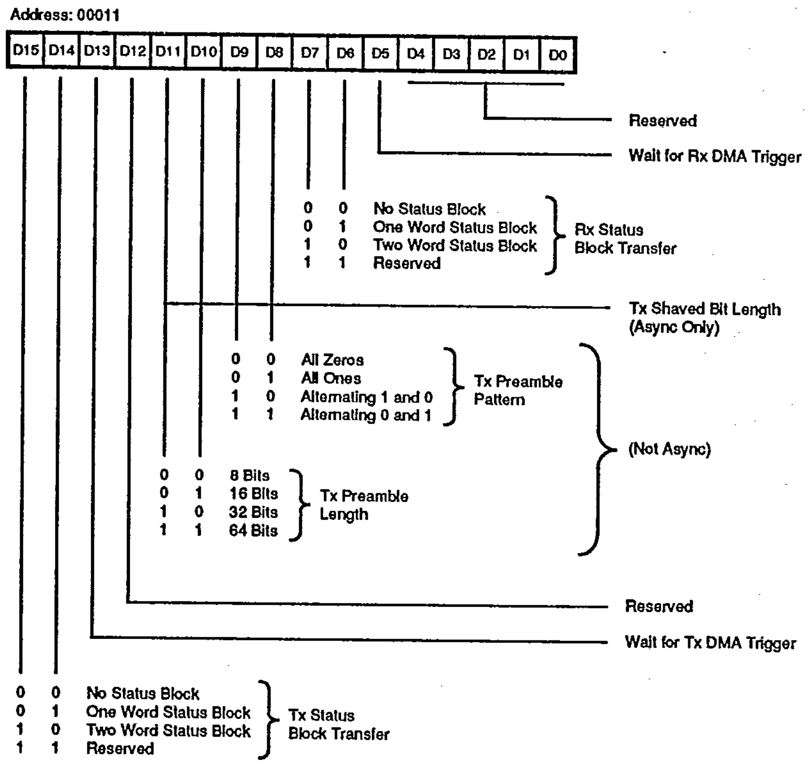

Figure 22. Channel Control Register

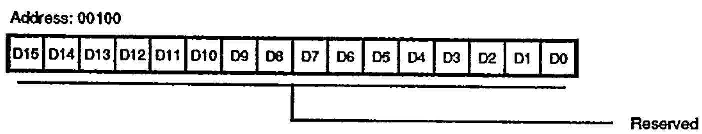

Figure 23. Primary Reserved Register

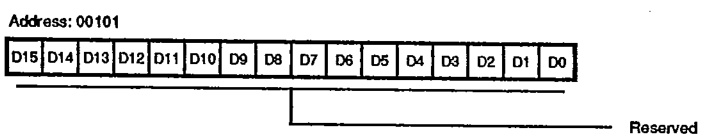

Figure 24. Secondary Reserved Register

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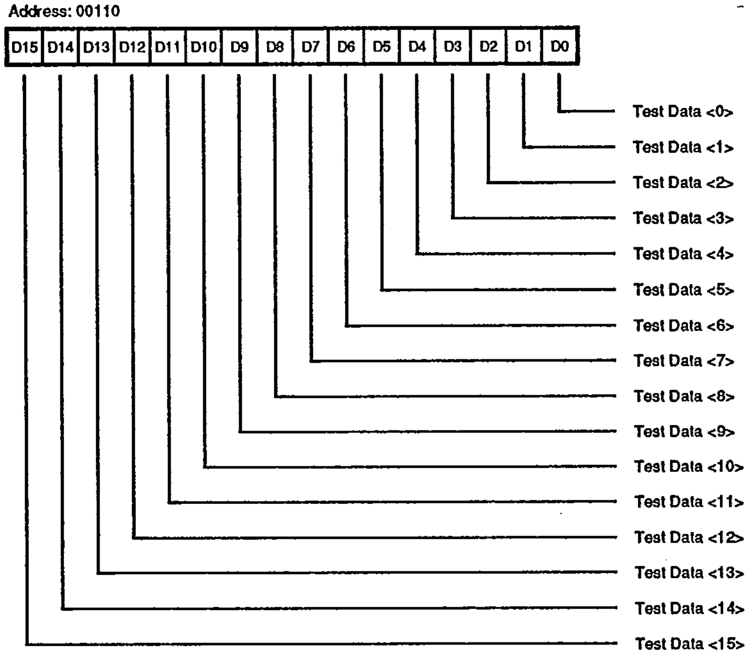

Figure 25. Test Mode Data Register

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Address: 00111

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D15–D5: Reserved

D4–D0: Test Register Address

D4	D3	D2	D1	D0	Test Register Address
0	0	0	0	0	Null Address
0	0	0	0	1	High Byte of Shifters
0	0	0	1	0	CRC Byte 0
0	0	0	1	1	CRC Byte 1
0	0	1	0	0	Rx FIFO (Write)
0	0	1	0	1	Clock Multiplexer Outputs
0	0	1	1	0	CTR0 and CTR1 Counters
0	0	1	1	1	Clock Multiplexer Inputs
0	1	0	0	0	DPLL State
0	1	0	0	1	Low Byte of Shifters
0	1	0	1	0	CRC Byte 2
0	1	0	1	1	CRC Byte 3
0	1	1	0	0	Tx FIFO (Read)
0	1	1	0	1	Reserved
0	1	1	1	0	I/O and Device Status Latches
0	1	1	1	1	Internal Daisy Chain
1	0	0	0	0	Reserved
1	0	0	0	1	Reserved
1	0	0	1	0	Reserved
1	0	0	1	1	Reserved
1	0	1	0	0	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Rx Count Holding Register
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved (4D44H, ASCII "MD")
1	1	0	0	1	Reserved (4D44H, ASCII "MD")
1	1	0	1	0	Reserved (4C42H, ASCII "LB")
1	1	0	1	1	Reserved (4453H, ASCII "DS")
1	1	1	0	0	Reserved (4D44H, ASCII "MD")
1	1	1	0	1	Reserved (4D44H, ASCII "MD")
1	1	1	1	0	Reserved (4C42H, ASCII "LB")
1	1	1	1	1	Reserved (4453H, ASCII "DS")

Figure 26. Test Mode Control Register

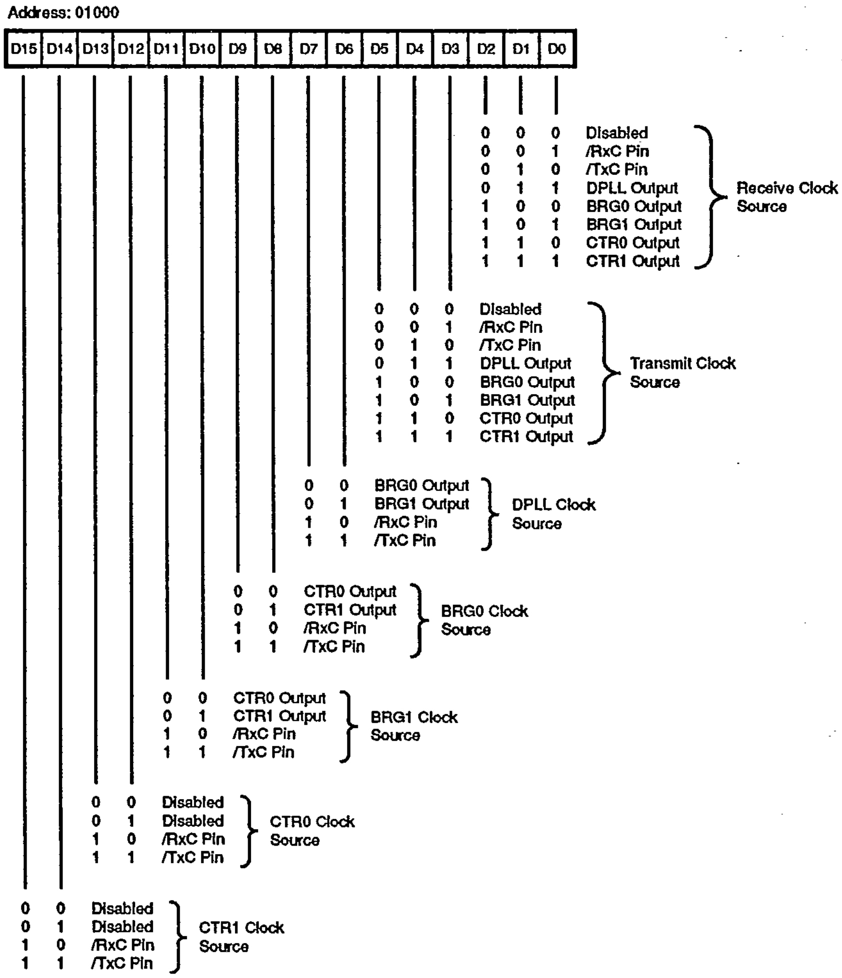

Figure 27. Clock Mode Control Register

T-75-37-07

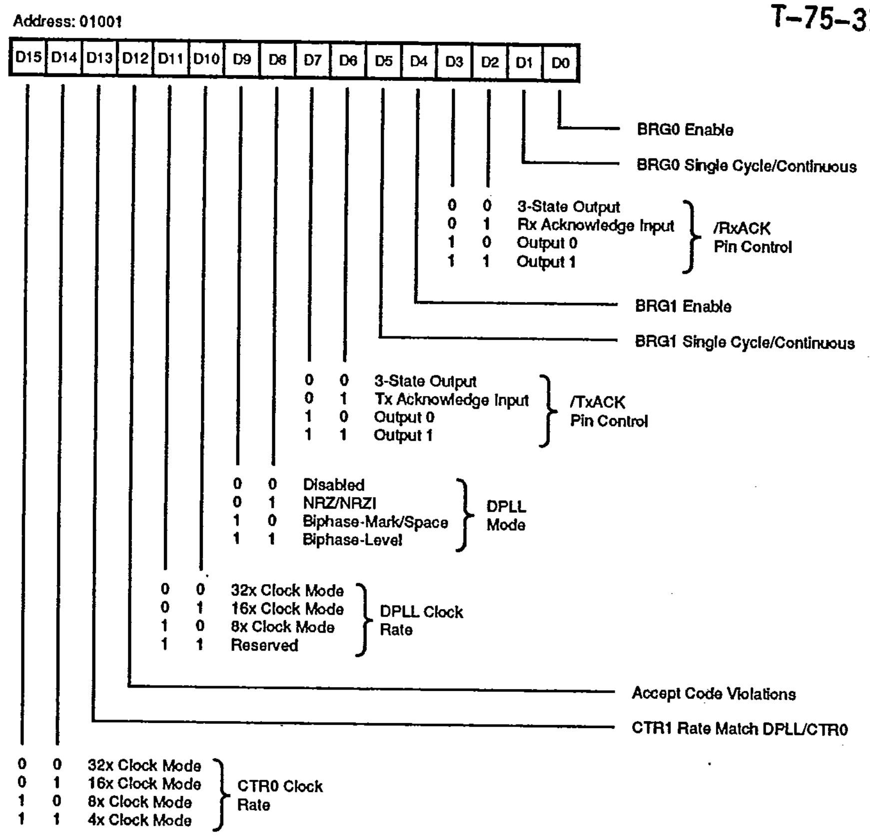

Figure 28. Hardware Configuration Register

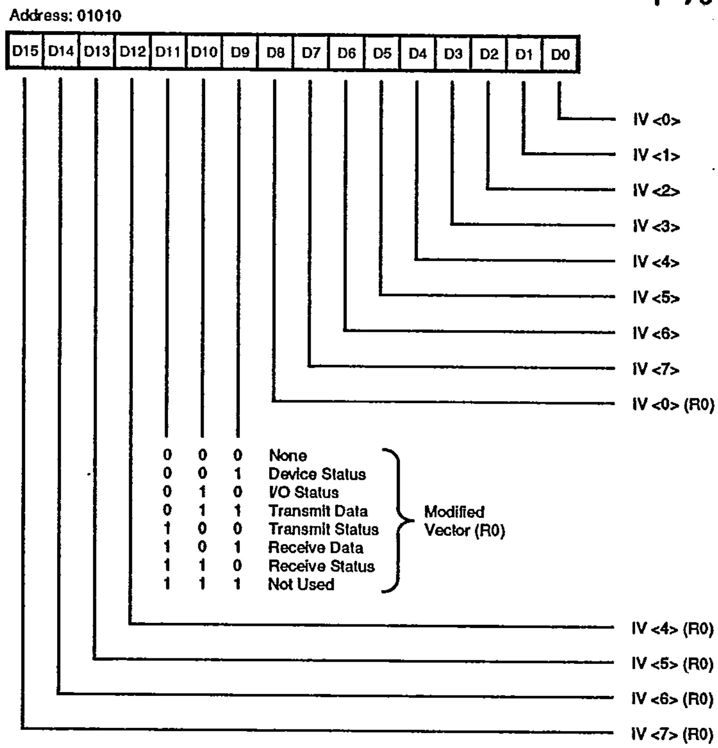

Figure 29. Interrupt Vector Register

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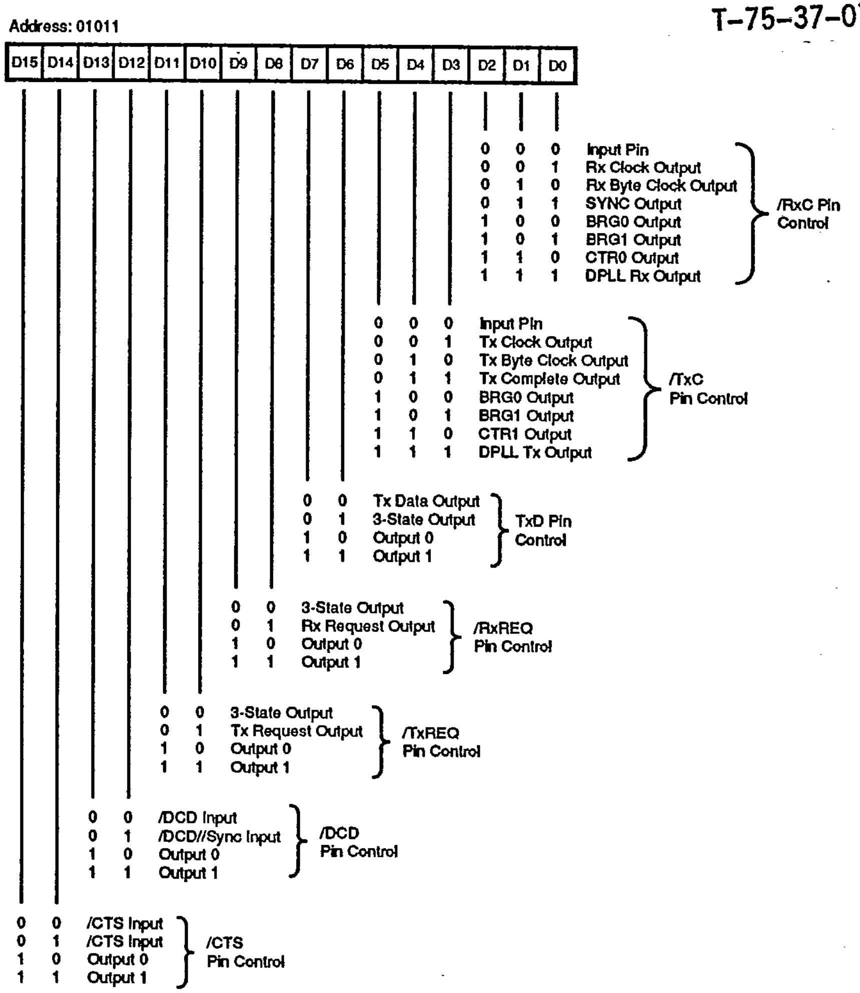

Figure 30. I/O Control Register

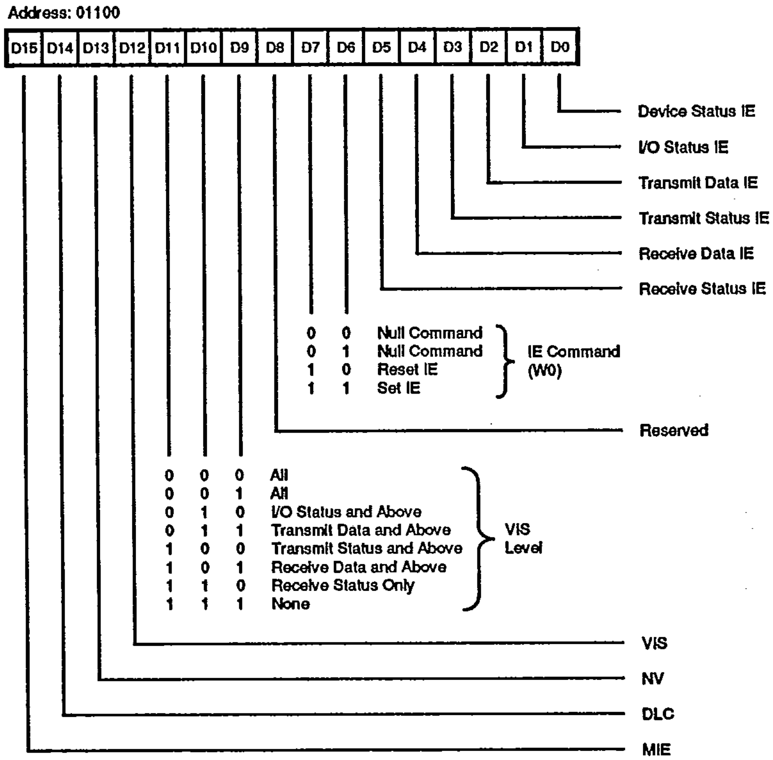

Figure 31. Interrupt Control Register

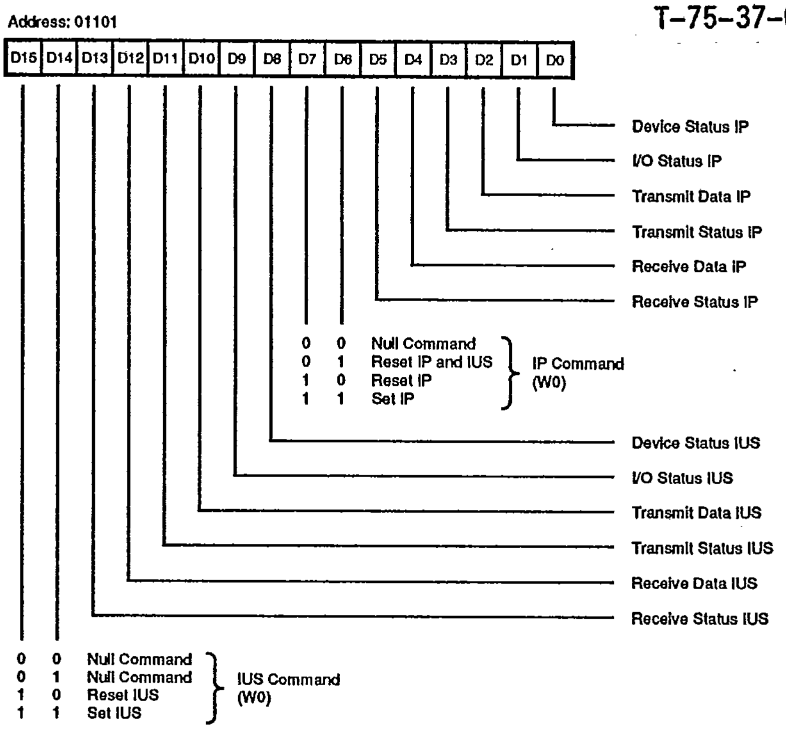

Figure 32. Daisy-Chain Control Register

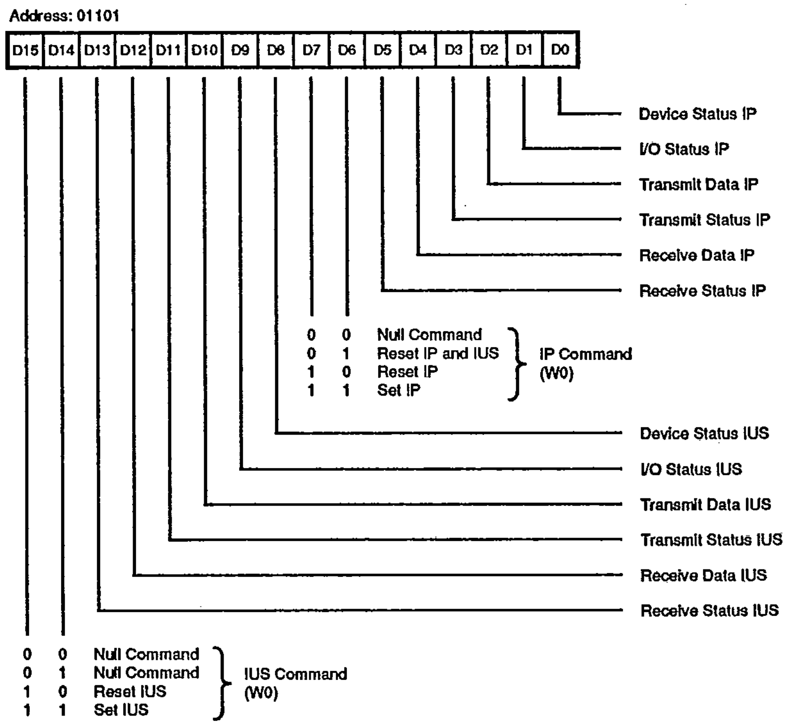

Figure 33. Miscellaneous Interrupt Status Register

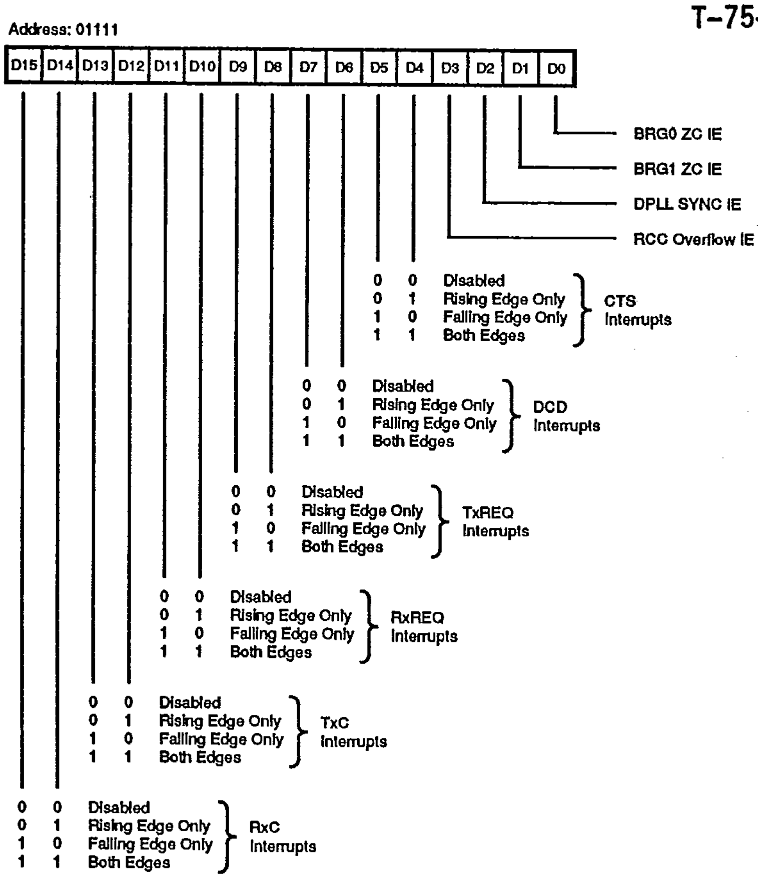

Figure 34. Status Interrupt Control Register

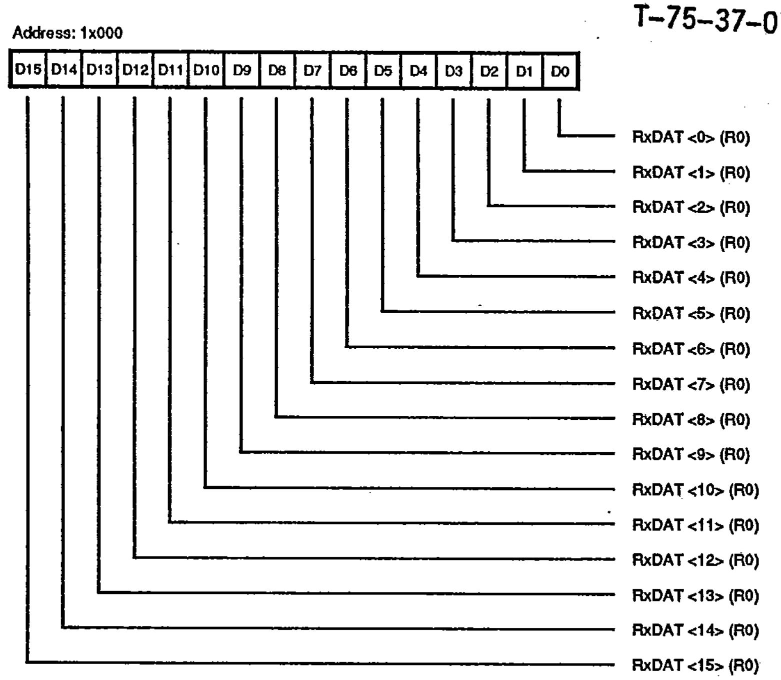

Figure 35. Receive Data Register

Address: 10001

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Rx Enable (D1, D0)

D1	D0	
0	0	Disable Immediately
0	1	Disable After Reception
1	0	Enable Without Auto-Enables
1	1	Enable With Auto-Enables

Rx Character Length (D4, D3, D2)

D4	D3	D2	
0	0	0	8 Bits
0	0	1	1 Bit
0	1	0	2 Bits
0	1	1	3 Bits
1	0	0	4 Bits
1	0	1	5 Bits
1	1	0	6 Bits
1	1	1	7 Bits

D5: Rx Parity Enable

Rx Parity Sense (D7, D6)

D7	D6	
0	0	Even
0	1	Odd
1	0	Space
1	1	Mark

D8: Reserved

D9: Rx CRC Enable

D10: Rx CRC Preset Value

Rx CRC Polynomial (D12, D11)

D12	D11	
0	0	CRC-CCITT
0	1	CRC-16
1	0	CRC-32
1	1	Reserved

Rx Data Encoding (D15, D14, D13)

D15	D14	D13	
0	0	0	NRZ
0	0	1	NRZB
0	1	0	NRZI-Mark
0	1	1	NRZI-Space
1	0	0	Biphase-Mark
1	0	1	Biphase-Space
1	1	0	Biphase-Level
1	1	1	Diff. Biphase-Level

Figure 36. Receive Mode Register

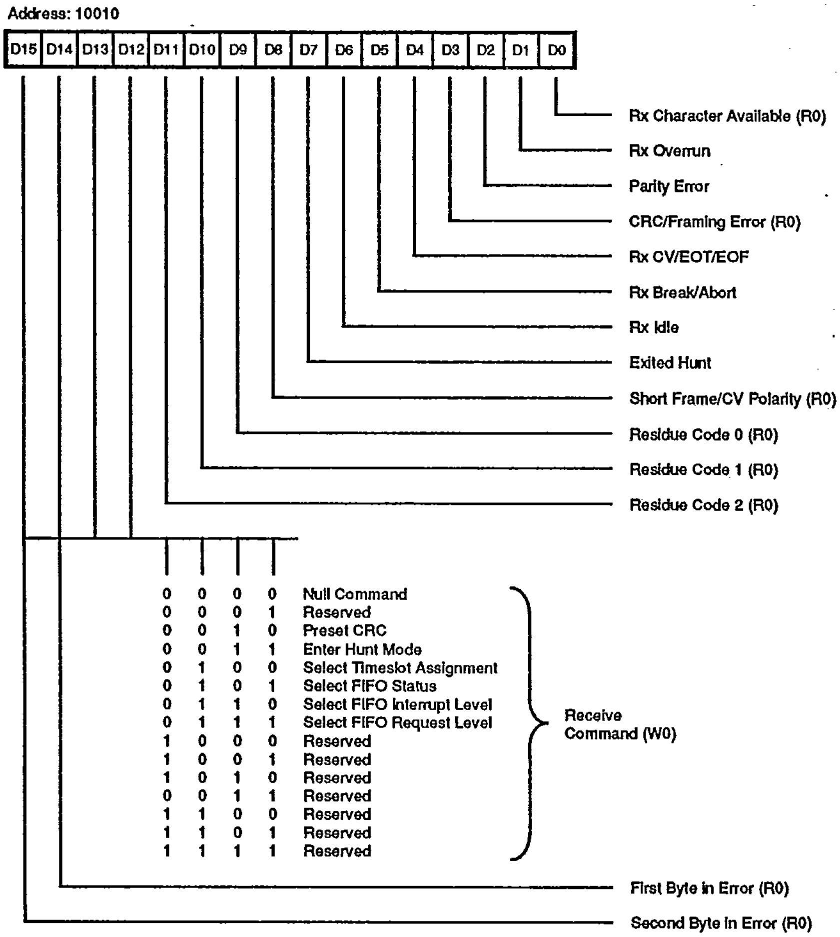

Figure 37. Receive Command Status Register

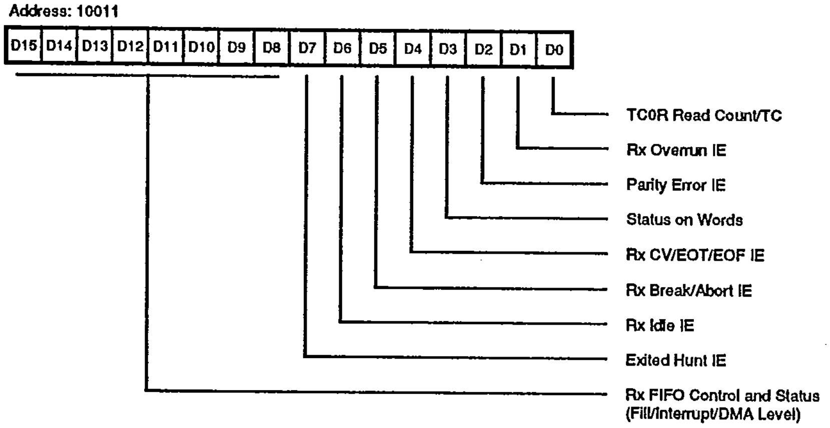

Figure 38. Receive Interrupt Control Register

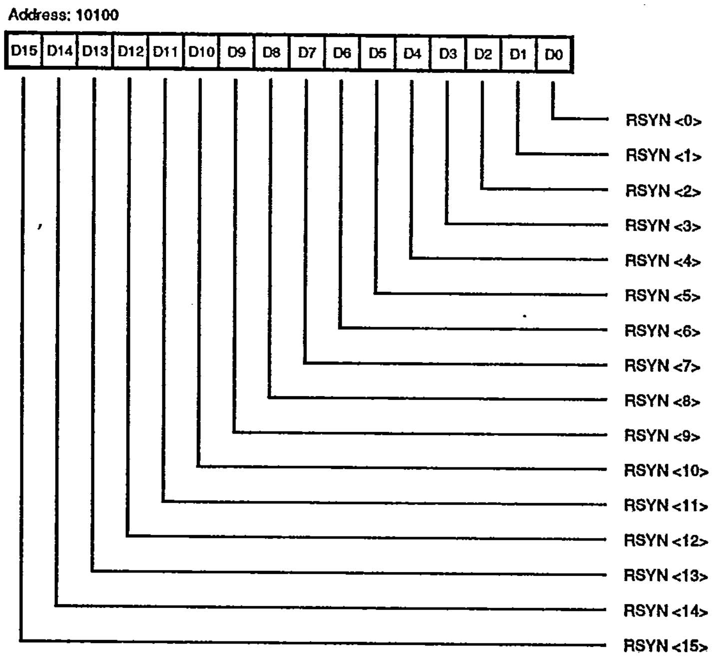

Figure 39. Receive Sync Register

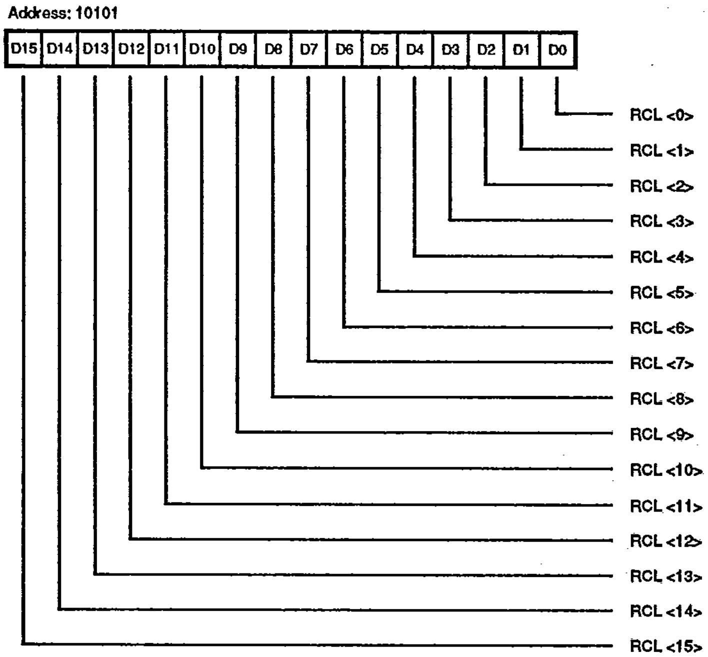

Figure 40. Receive Count Limit Register

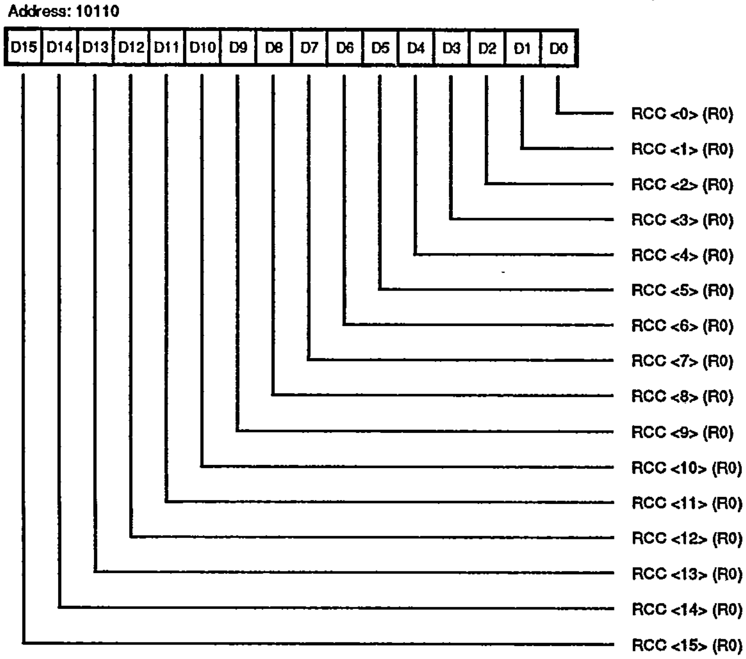

Figure 41. Receive Character Count Register

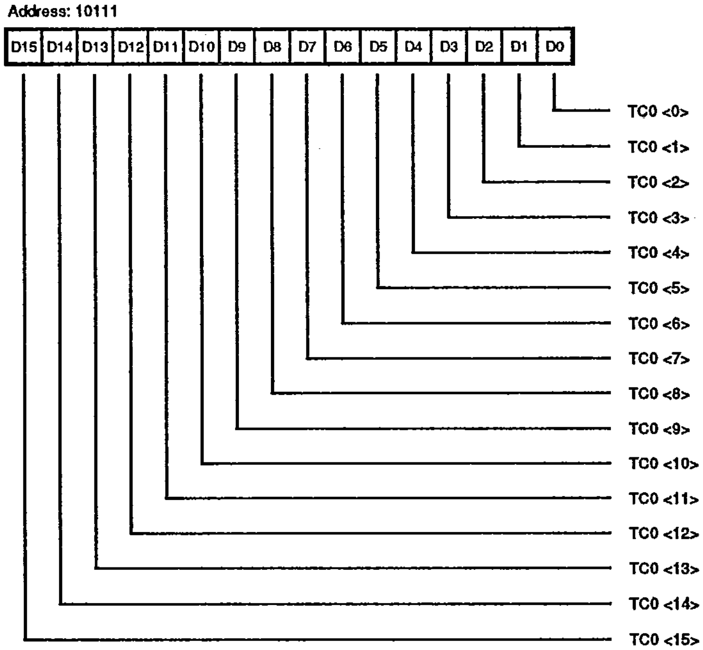

Figure 42. Time Constant 0 Register

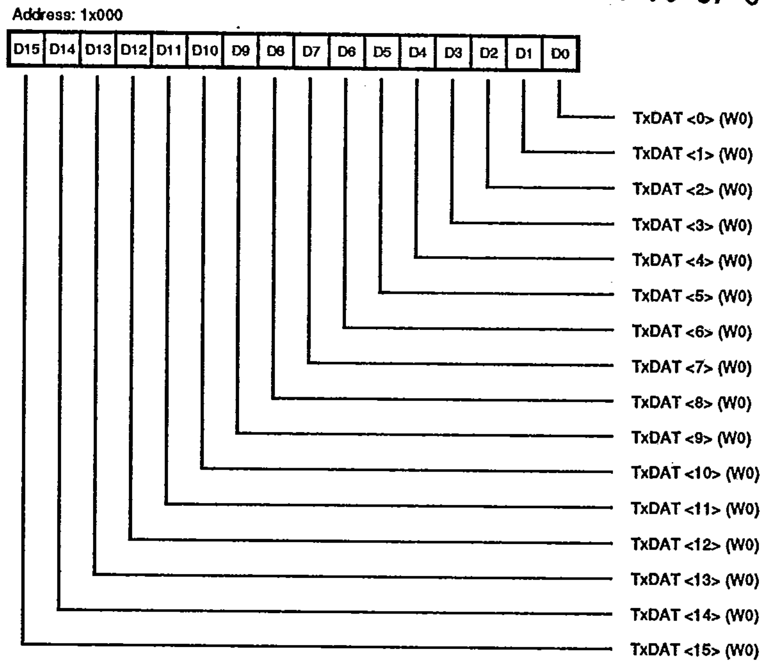

Figure 43. Transmit Data Register

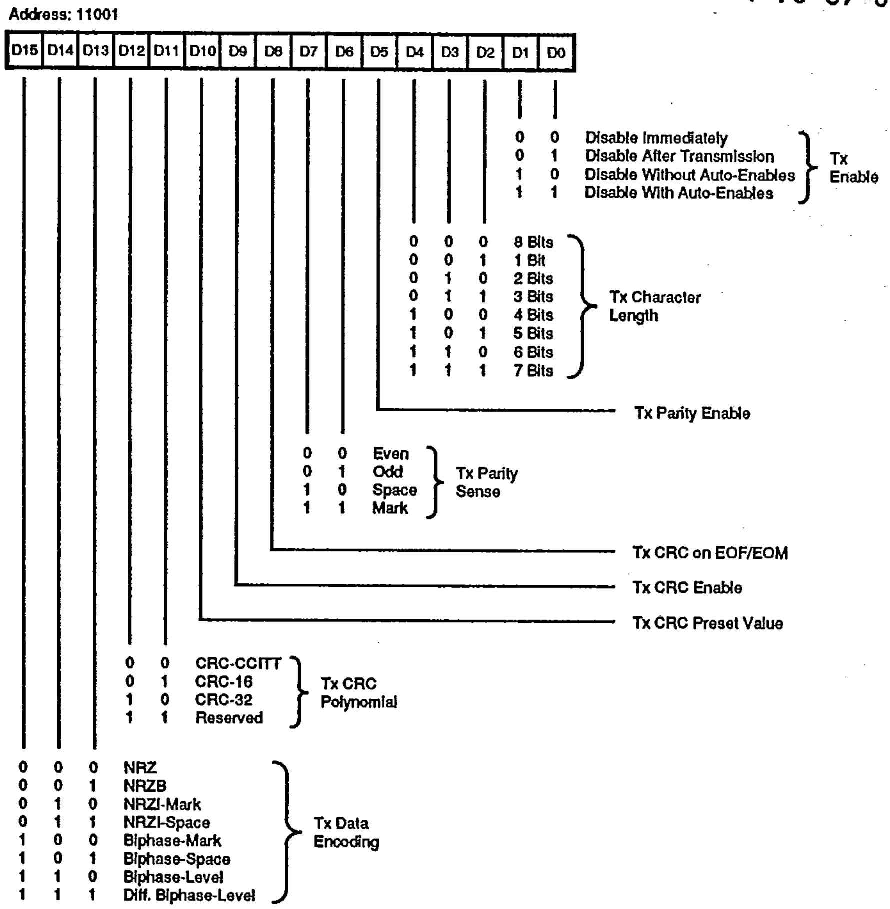

Figure 44. Transmit Mode Register

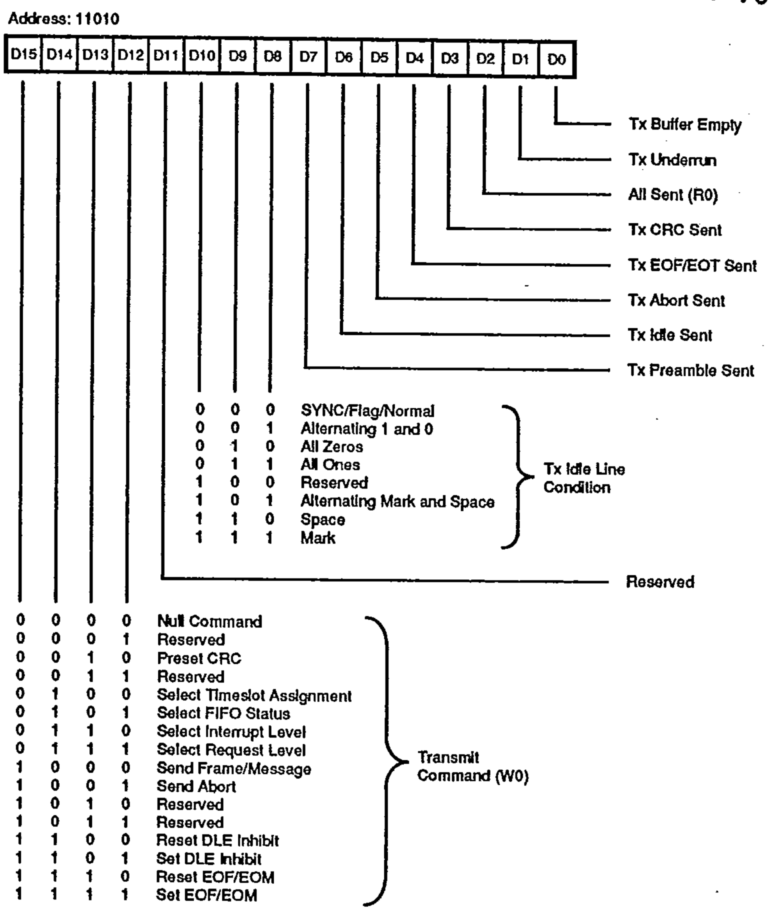

Figure 45. Transmit Command/Status Register

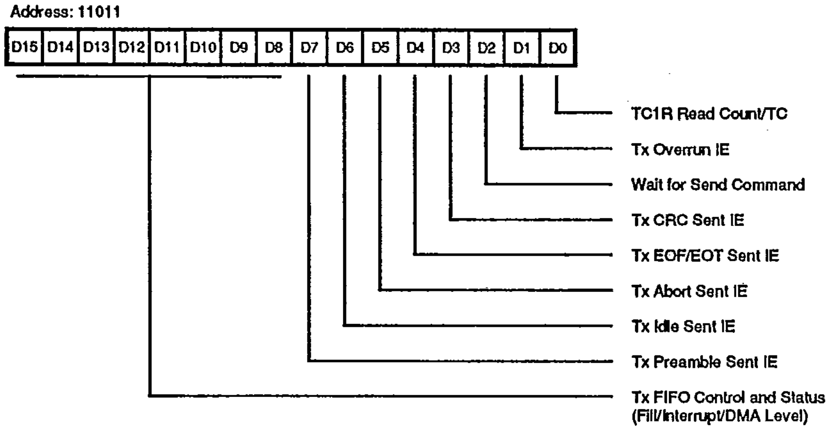

Figure 46. Transmit Interrupt Control Register

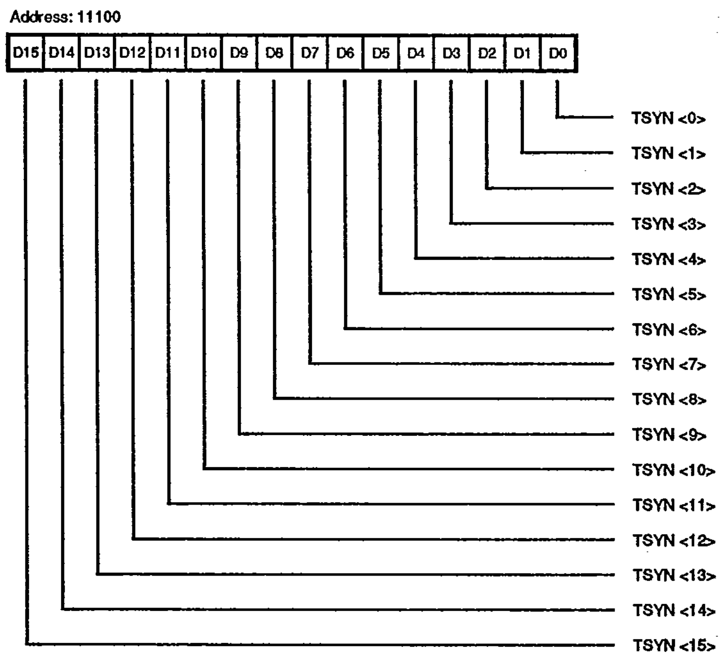

Figure 47. Transmit Sync Register

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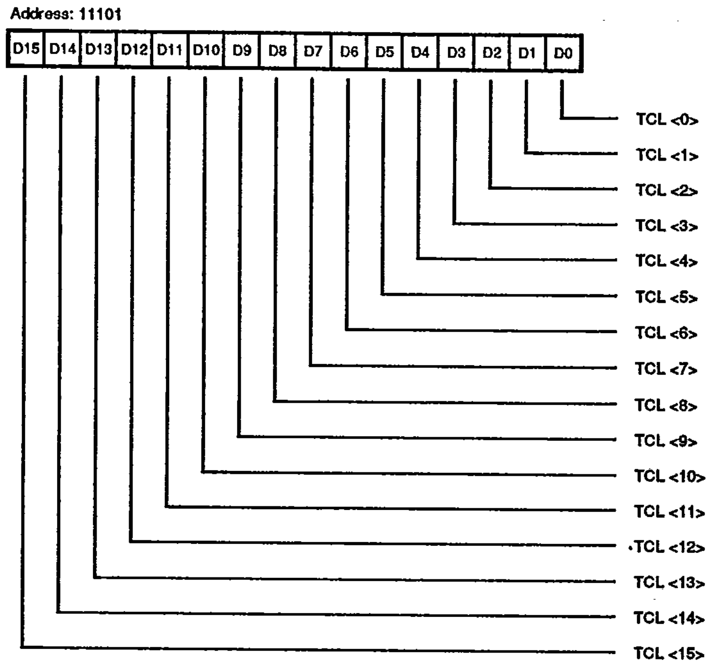


Figure 48. Transmit Count Limit Register

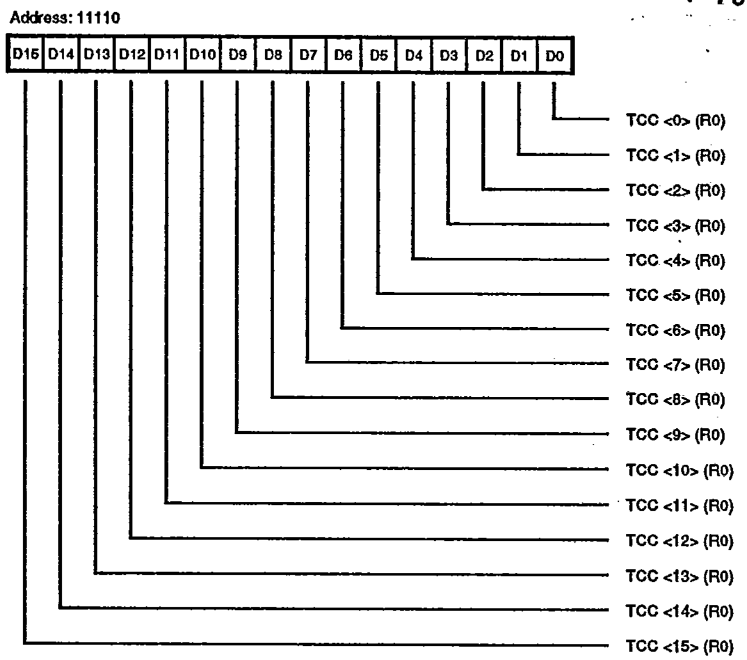


Figure 49. Transmit Character Count Register

T-75-37-07

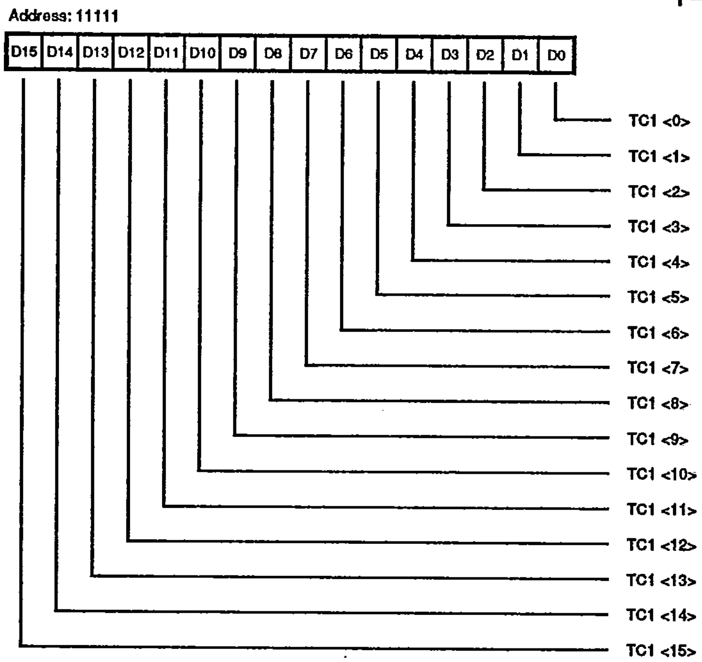
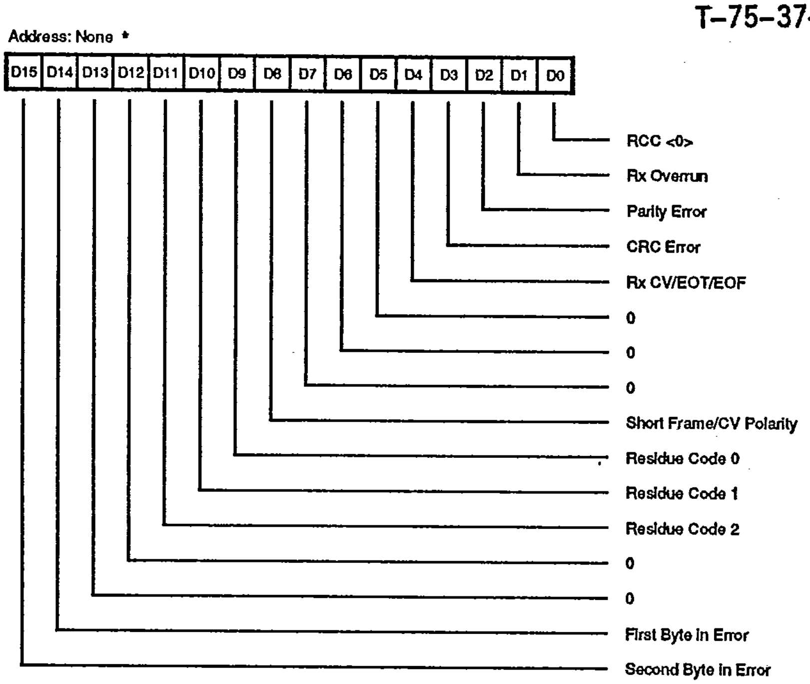


Figure 50. Time Constant 1 Register

T-75-37-07



* Refer to Figure 22 (Channel Control Register)
Bits 6-7 for Access Method

Figure 51. Receive Status Block Register

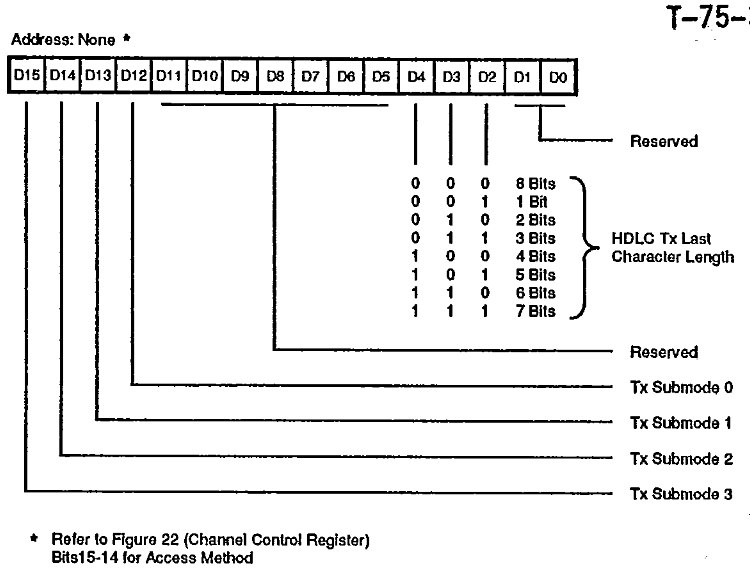


Figure 52. Transmit Status Block Register

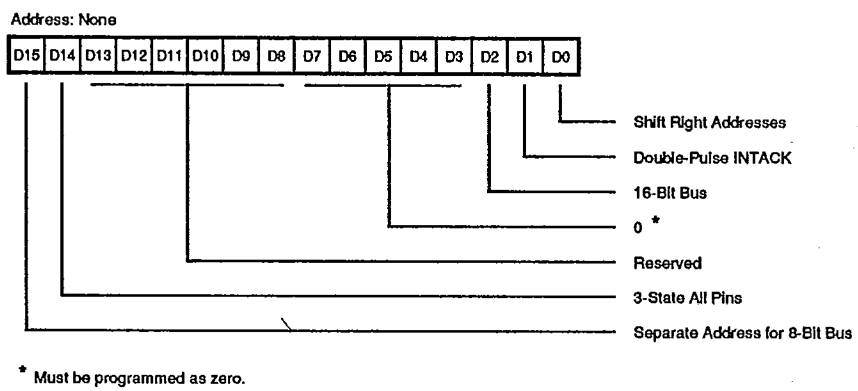


Figure 53. Bus Configuration Register

USC TIMING

The USC interface timing is similar to that found on a static RAM, except that it is much more flexible. Up to eight separate timing strobe signals may be present on the interface: /DS, /RD, /WR, /PITACK, /RxACKA, /RxACKB, /TxACKA and /TxACKB. Only one of these timing strobes may be active at any time. Should the external logic activate more than one of these strobes at the same time the USC will enter a pre-reset state that is only exited by a hardware reset. Do not allow overlap of timing strobes. The timing diagrams, beginning on the next page, illustrate the different bus transactions possible, with the necessary setup, hold and delay times.

ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to Vss .... -0.3 V to +7.0 V
Voltages on all inputs with respect to Vss .... -0.3V to V_{CC} +0.3V
Operating Ambient Temperature .... See Ordering Information
Storage Temperature .... -65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and Capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

$+4.5\text{ V} < V_{CC} < +5.5\text{ V}$
GND = 0 V
T_A as specified in Ordering Information

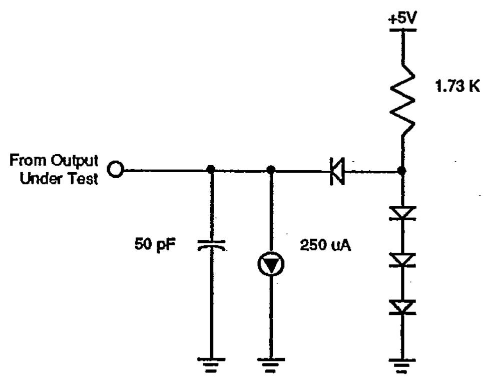


Figure 54. Standard Test Load

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Condition
C_{IN}	Input Capacitance		10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance		15	pf	Returned to Ground
$C_{I/O}$	Bidirectional Capacitance		20	pf	

f= 1MHz, over specified temperature range.
Unmeasured pins returned to ground.

MISCELLANEOUS Transistor Count - 174,000

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DC CHARACTERISTICS
Z16C30

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{OH1}	Output High Voltage	2.4			V	I_{OH}= -1.6mA
V_{OH2}	Output High Voltage	V_{CC}-0.8			V	I_{OH}= -250 µA
V_{OL}	Output Low Voltage			0.4	V	I_{OL}= +2.0 mA
I_{IL}	Input Leakage			+10.00	µA	0.4 < V_{IN} < +2.4V
I_{OL}	Output Leakage			+10.00	µA	0.4 < V_{OUT} < +2.4V
I_{CC1}	V_{CC}Supply Current		7	50	mA	V_{CC}=5V V_{IH}=4.8V V_{IL} -0.2V

V_{CC}= 5V ± 10% unless otherwise specified, over specified temperature range.

AC CHARACTERISTICS
Z16C30

No	Symbol	Parameter	10 MHz Min	10 MHz Max	Note
1	Tcyc	Bus Cycle Time	160		
2	TwASl	/AS Low Width	40		
3	TwASh	/AS High Width	90		
4	TwDSl	/DS Low Width	70		
5	TwDSh	/DS High Width	60		
6	TdAS(DS)	/AS↑ to /DS↓ Delay Time	5		
7	TdDS(AS)	/DS↑ to /AS↓ Delay Time	5		
8	TdDS(DRa)	/DS↓ to Data Active Delay	0		
9	TdDS(DRv)	/DS↓ to Data Valid Delay		85	
10	TdDS(DRn)	/DS↑ to Data Not Valid Delay	0		
11	TdDS(DRz)	/DS↑ to Data Float Delay		20	
12	TsCS(AS)	/CS to /AS↑ Setup Time	15		
13	ThCS(AS)	/CS to /AS↑ Hold Time	0		
14	TsADD(AS)	Direct Address to /AS↑ Setup Time	15		[1]
15	ThADD(AS)	Direct Address to /AS↑ Hold Time	5		[1]
16	TsSIA(AS)	/SITACK to /AS↑ Setup Time	15		
17	ThSIA(AS)	/SITACK to /AS↑ Hold Time	5		
18	TsAD(AS)	Address to /AS↑ Setup Time	15		
19	ThAD(AS)	Address to /AS↑ Hold Time	5		
20	TsRW(DS)	R/W to /DS↓ Setup Time	0		
21	ThRW(DS)	R/W to /DS↓ Hold Time	25		
22	TsDSf(RRQ)	/DS↓ to /RxREQ Inactive Delay		60	[4]
23	TdDSr(RRQ)	/DS↑ to /RxREQ Active Delay	0		
24	TsDW(DS)	Write Data to /DS↑ Setup Time	30		
25	ThDW(DS)	Write Data to /DS↑ Hold Time	0		

AC CHARACTERISTICS (Continued)
Z16C30

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No	Symbol	Parameter	10 MHz Min	10 MHz Max	Note
26	TdDSf(TRQ)	/DS↓ to /TxREQ Inactive Delay		60	[5]
27	TdDSr(TRQ)	/DS↑ to /TxREQ Active Delay	0		
28	TwRDl	/RD Low Width	70		
29	TwRDh	/RD High Width	60		
30	TdAS(RD)	/AS↑ to /RD↓ Delay Time	5		
31	TdRD(AS)	/RD↑ to /AS↓ Delay Time	5		
32	TdRD(DRa)	/RD↓ to Data Active Delay	0		
33	TdRD(DRv)	/RD↓ to Data Valid Delay		85	
34	TdRD(DRn)	/RD↑ to Data Non Valid Delay	0		
35	TdRD(DRz)	/RD↑ to Data Float Delay		20	
36	TdRDf(RRQ)	/RD↓ to /RxREQ Inactive Delay		60	[4]
37	TdRDr(RRQ)	/RD↑ to /RxREQ Active Delay	0		
38	TwWRl	/WR Low Width	70		
39	TwWRh	/WR High Width	60		
40	TdAS(WR)	/AS↑ to /WR↓ Delay Time	5		
41	TdWR(AS)	/WR↑ to /AS↓ Delay Time	5		
42	TsDW(WR)	Write Data to /WR↑ Setup Time	30		
43	ThDW(WR)	Write Data to /WR↑ Hold Time	0		
44	TdWRf(TRQ)	/WR↓ to /TxREQ Inactive Delay		60	[5]
45	TdWRr(TRQ)	/WR↑ to /TxREQ Active Delay	0		
46	TsCS(DS)	/CS to /DS↓ Setup Time	0		[2]
47	ThCS(DS)	/CS to /DS↓ Hold Time	25		[2]
48	TsADD(DS)	Direct Address to /DS↓ Setup Time	5		[1,2]
49	ThADD(DS)	Direct Address to /DS↓ Hold Time	25		[1,2]
50	TsSIA(DS)	/SITACK to /DS↓ Setup Time	5		[2]
51	ThSIA(DS)	/SITACK to /DS↓ Hold Time	25		[2]
52	TsCS(RD)	/CS to /RD↓ Setup Time	0		[2]
53	ThCS(RD)	/CS to /RD↓ Hold Time	25		[2]
54	TsADD(RD)	Direct Address to /RD↓ Setup Time	5		[1,2]
55	ThADD(RD)	Direct Address to /RD↓ Hold Time	25		[1,2]
56	TsSIA(RD)	/SITACK to /RD↓ Setup Time	5		[2]
57	ThSIA(RD)	/SITACK to /RD↓ Hold Time	25		[2]
58	TsCS(WR)	/CS to /WR↓ Setup Time	0		[2]
59	ThCS(WR)	/CS to /WR↓ Hold Time	25		[2]
60	TsADD(WR)	Direct Adress to /WR↓ Setup Time	5		[1,2]
61	ThADD(WR)	Direct Address to /WR↓ Hold Time	25		[1,2]
62	TsSIA(WR)	/SITACK to /WR↓ Setup Time	5		[2]
63	ThSIA(WR)	/SITACK to /WR↓ Hold Time	25		[2]
64	TwRAKl	/RxACK Low Width	70		
65	TwRAKh	/RxACK High Width	60		

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AC CHARACTERISTICS (Continued)
Z16C30

No	Symbol	Parameter	10 MHz Min	10 MHz Max	Note
66	TdRAK(DRa)	/RxACK↓ to Data Active Delay	0		
67	TdRAK(DRv)	/RxACK↓ to Data Valid Delay		85	
68	TdRAK(DRn)	/RxACK↑ to Data Not Valid Delay	0		
69	TdRAK(DRz)	/RxACK↑ to Data Float Delay		20	
70	TdRAKf(RRQ)	/RxACK↓ to /RxREQ Inactive Delay		60	[4]
71	TdRAKr(RRQ)	/RxACK↑ to /RxREQ Active Delay	0		
72	TwTAKl	/TxACK Low Width	70		
73	TwTAKh	/TxACK High Width	60		
74	TsDW(TAK)	Write Data to /TxACK↑ Setup Time	30		
75	ThDW(TAK)	Write Data to /TxACK↑ Hold Time	0		
76	TdTAKf(TRQ)	/TxACK↓ to /TxREQ Inactive Delay		60	[5]
77	TdTAKr(TRQ)	/TxACK↑ to /TxREQ Active Delay	0		
78	TdDSf(RDY)	/DS↓ (Intack) to /READY↓ Delay		200	
79	TdRDY(DRv)	/READY↓ to Data Valid Delay		40	
80	TdDSr(RDY)	/DS↑ to /READY↑ Delay		40	
81	TsIEI(DSI)	IEI to /DS↓ (Intack) Setup Time	60		
82	ThIEI(DSI)	IEI to /DS↑ (Intack) Hold Time	0		
83	TdIEI(IEO)	IEI to IEO Delay		60	
84	TdAS(IEO)	/AS↑(Intack) to IEO Delay		60	
85	TdDSI(INT)	/DS↓ (Intack) to /INT Inactive Delay		200	
86	TdDSI(Wf)	/DS↓ (Intack) to /WAIT↓ Delay		40	
87	TdDSI(Wr)	/DS↓ (Intack) to /WAIT↑ Delay		200	
88	TdW(DRv)	/WAIT↑ to Data Valid Delay		40	
89	TdRDf(RDY)	/RD↓ (Intack) to /READY↓ Delay		200	
90	TdRDr(RDY)	/RD↑ to /READY↑ Delay		40	
91	TsIEI(RDI)	IEI to /RD↓ (Intack) Setup Time	60		
92	ThIEI(RDI)	IEI to /RD↑ (Intack) Hold Time	0		
93	TdRDI(INT)	/RD↓ (Intack) to /INT Inactive Delay		200	
94	TdRDI(Wf)	/RD↓ (Intack) to /WAIT↓ Delay		40	
95	TdRDI(Wr)	/RD↓ (Intack) to /WAIT↑ Delay		200	
96	TwPIAl	/PITACK Low Width	70		
97	TwPIAh	/PITACK High Width	60		
98	TdAS(PIA)	/AS↑ to /PITACK↓ Delay Time	5		
99	TdPIA(AS)	/PITACK↑ to /AS↓ Delay Time	5		
100	TdPIA(DRa)	/PITACK↓ to Data Active Delay	0		
101	TdPIA(DRn)	/PITACK↑ to Data Not Valid Delay	0		
102	TdPIA(DRz)	/PITACK↑ to Data Float Delay		20	
103	TsIEI(PIA)	IEI to /PITACK↓ Setup Time	60		
104	ThIEI(PIA)	IEI to /PITACK↑ Hold Time	0		
105	TdPIA(IEO)	/PITACK↓ to IEO Delay		60	

AC CHARACTERISTICS (Continued)
Z16C30

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No	Symbol	Parameter	10 MHz Min	10 MHz Max	Note
106	TdPIA(INT)	/PITACK↓ to /INT Inactive Delay		200	
107	TdPIAf(RDY)	/PITACK↓ to /READY↓ Delay		200	
108	TdPIAr(RDY)	/PITACK↑ to /READY↑ Delay		40	
109	TdPIA(Wf)	/PITACK↓ to /WAIT↓ Delay		40	
110	TdPIA(Wr)	/PITACK↓ to /WAIT↑ Delay		200	
111	TdSIA(INT)	/SITACK↓ to IEO Inactive Delay		200	[2]
112	TwSTBh	/Strobe High Width	60		[3]
113	TwRESl	/Reset Low Width	170		
114	TwRESh	/Reset High Width	60		
115	Tdres(STB)	/Reset↑ to /Strobe ↓	60		[3]
116	TdDSf(RDY)	/DS↓ to /READY↓ Delay		50	
117	TdWRf(RDY)	/WR↓ to /READY↓ Delay		50	
118	TdWRr(RDY)	/WR↑ to /READY↑ Delay		40	
119	TdRDf(RDY)	/RD↓ to /READY↓ Delay		50	
120	TdRAKf(RDY)	/RxACK↓ to /READY↓ Delay		50	
121	TdRAKr(RDY)	/RxACK↑ to /READY↑ Delay		40	
122	TdTAKf(RDY)	/TxACK↓ to /READY↓ Delay		50	
123	TdTAKr(RDY)	/TxACK↑ to /READY↑ Delay		40	

Notes:
[1] Direct address is any of A//B, D//C or AD15-AD8 used as an address bus.
[2] The parameter applies only when /AS is not present.
[3] Strobe is any of /DS, /RD, /WR, /PITACK, /RxACK or /TxACK.
[4] Parameter applies only if read empties the receive FIFO.
[5] Parameter applies only if write fills the transmit FIFO.

TIMING DIAGRAMS

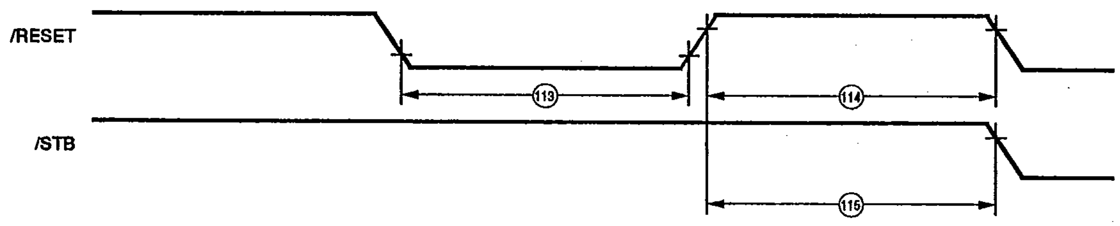

Figure 55. Reset Timing

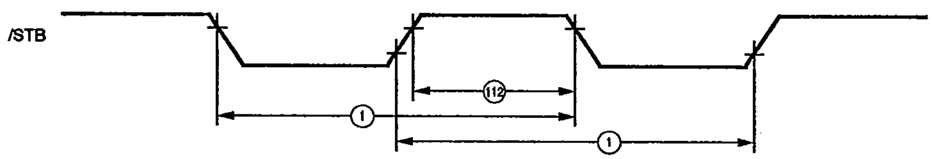

Figure 56. Bus Cycle Timing

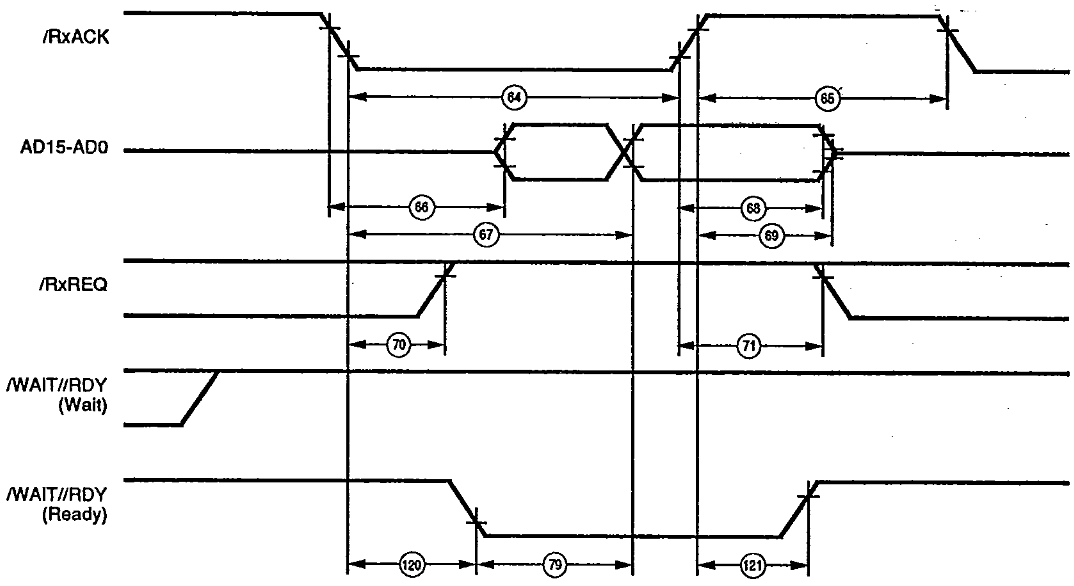

Figure 57. DMA Read Cycle

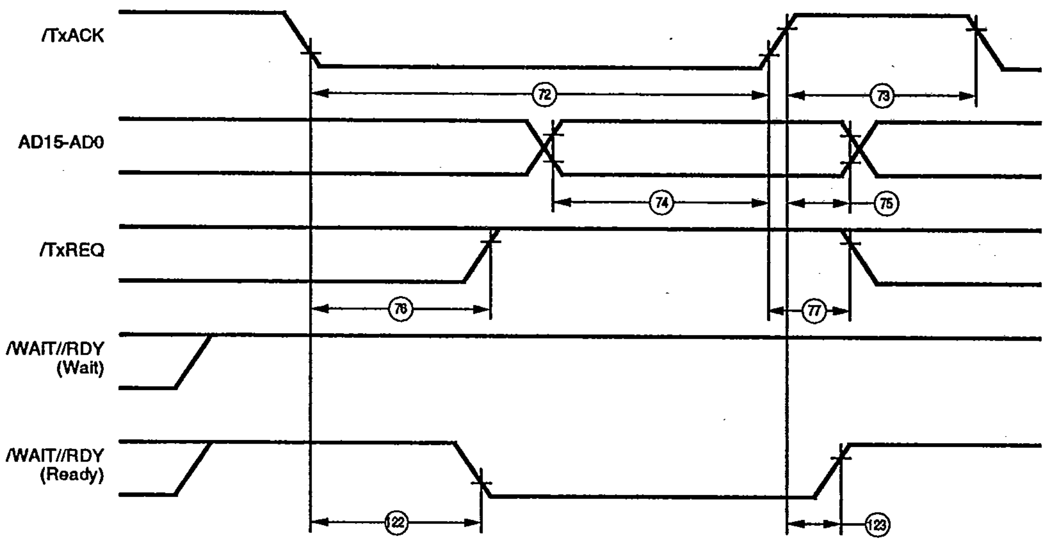

Figure 58. DMA Write Cycle

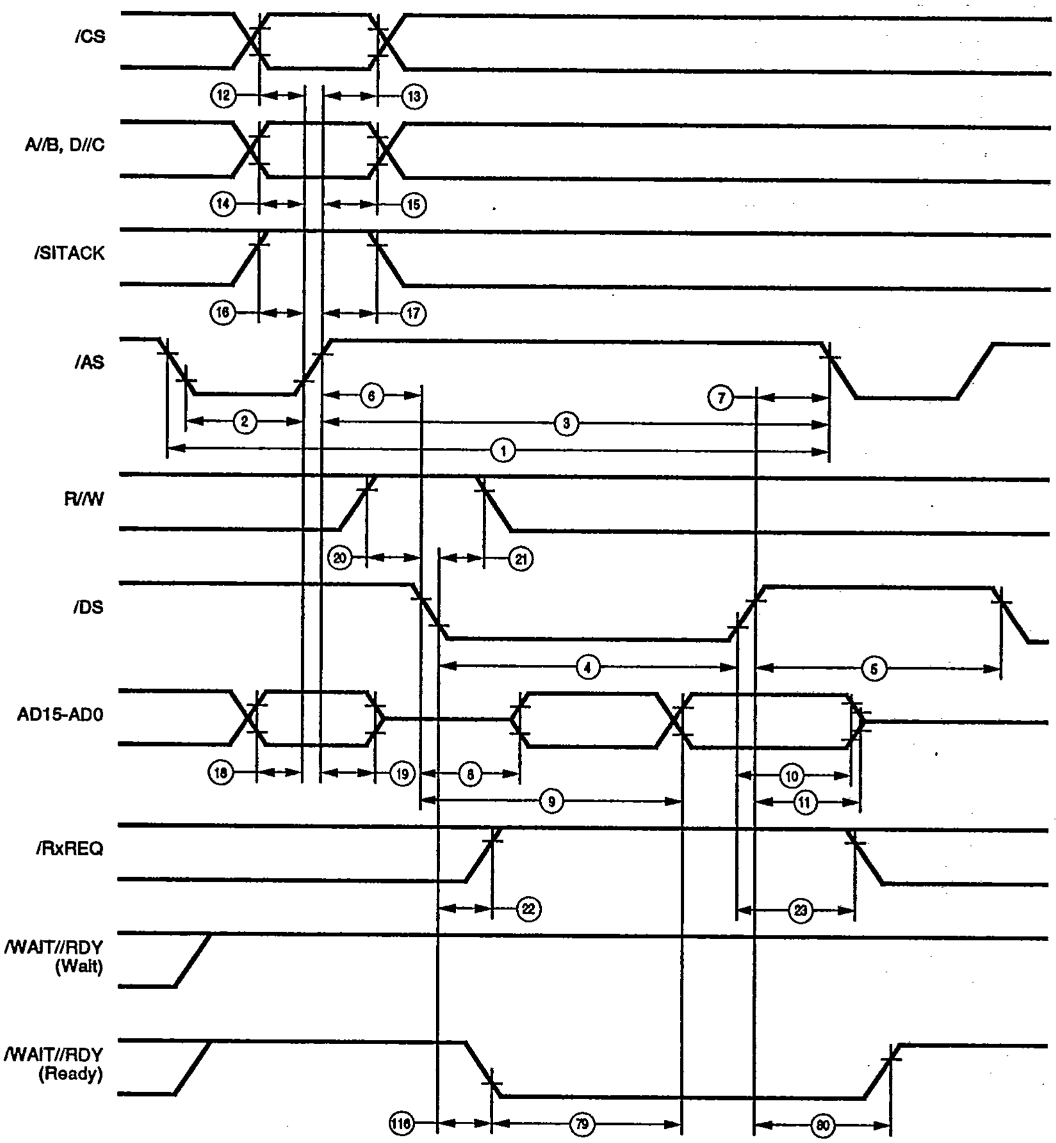

Figure 59. Multiplexed /DS Read Cycle

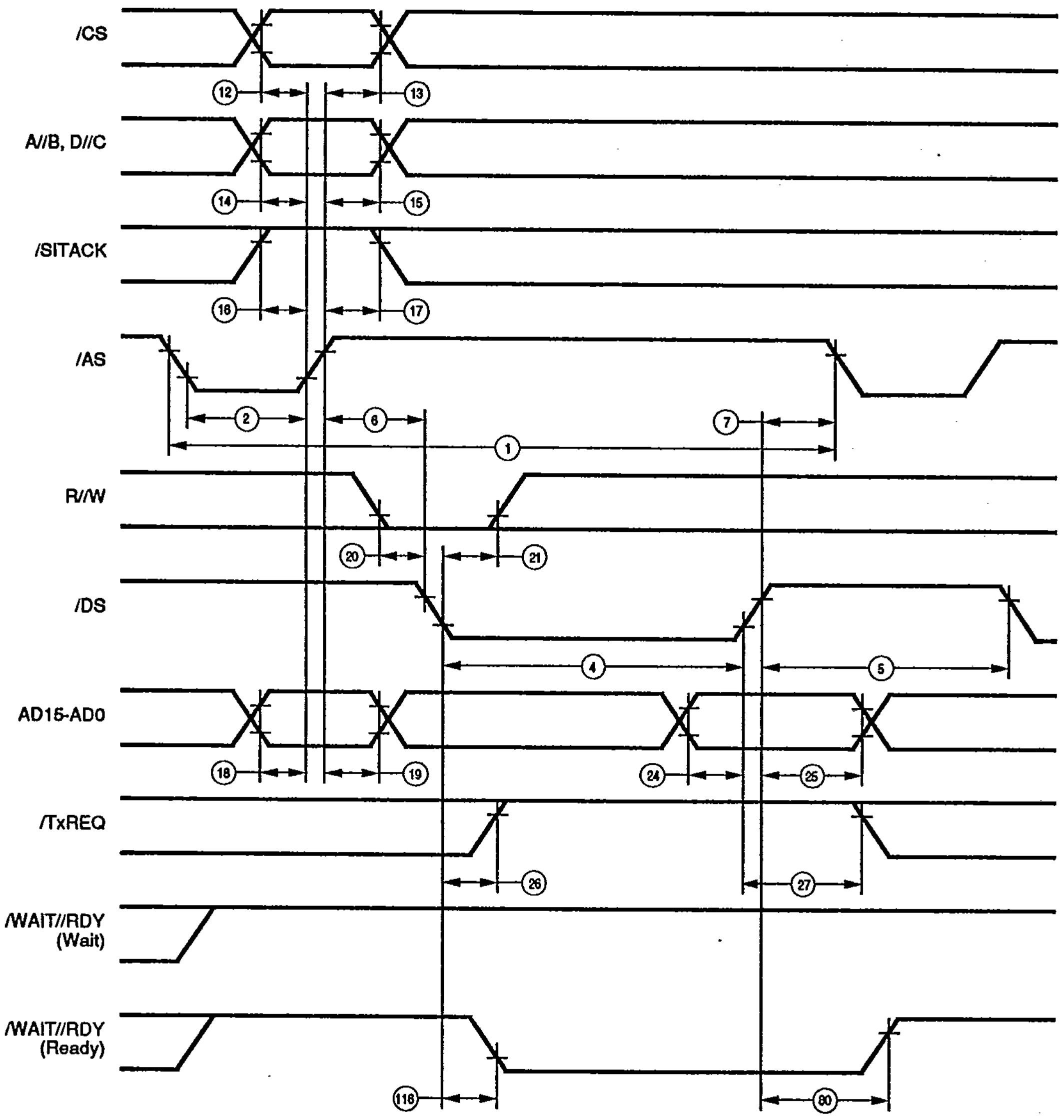

Figure 60. Multiplexed /DS Write Cycle

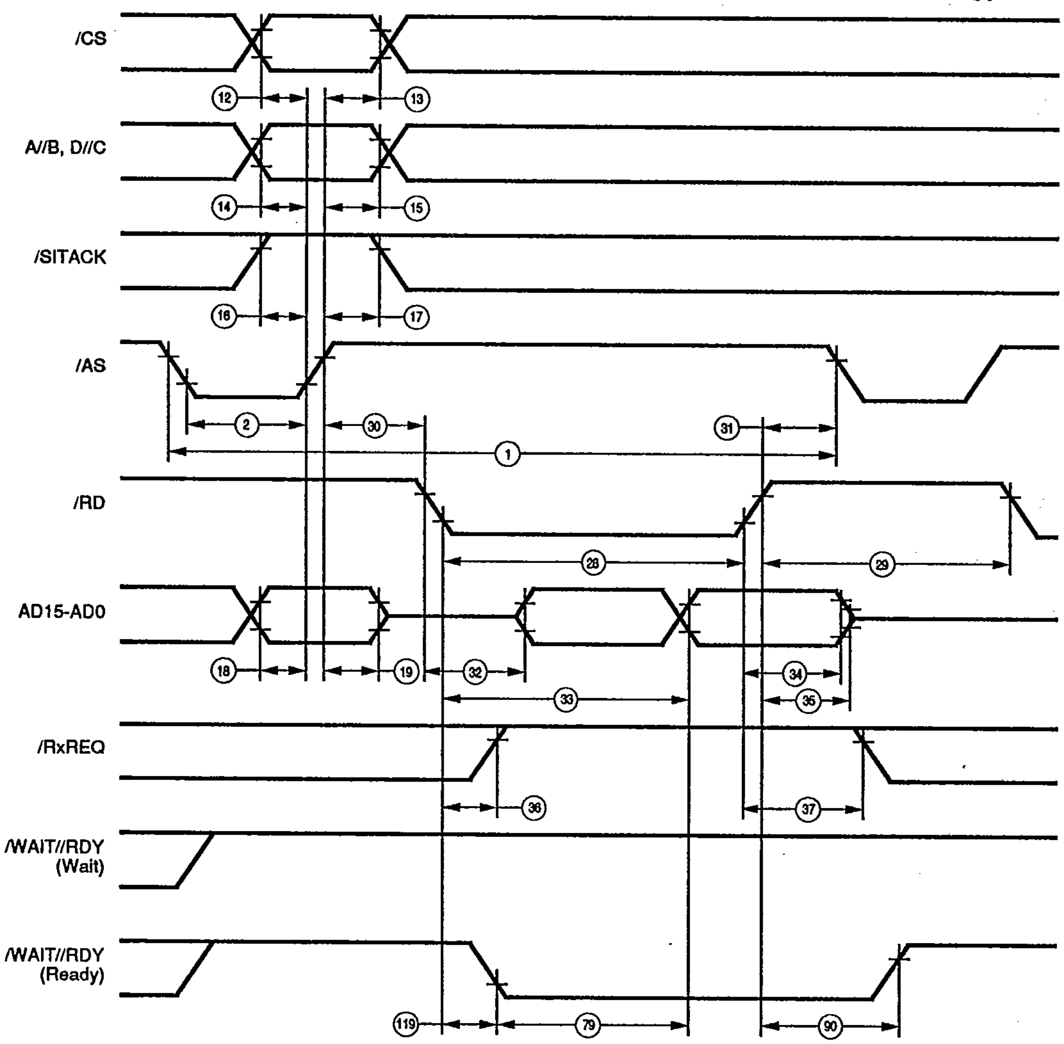

Figure 61. Multiplexed /RD Read Cycle

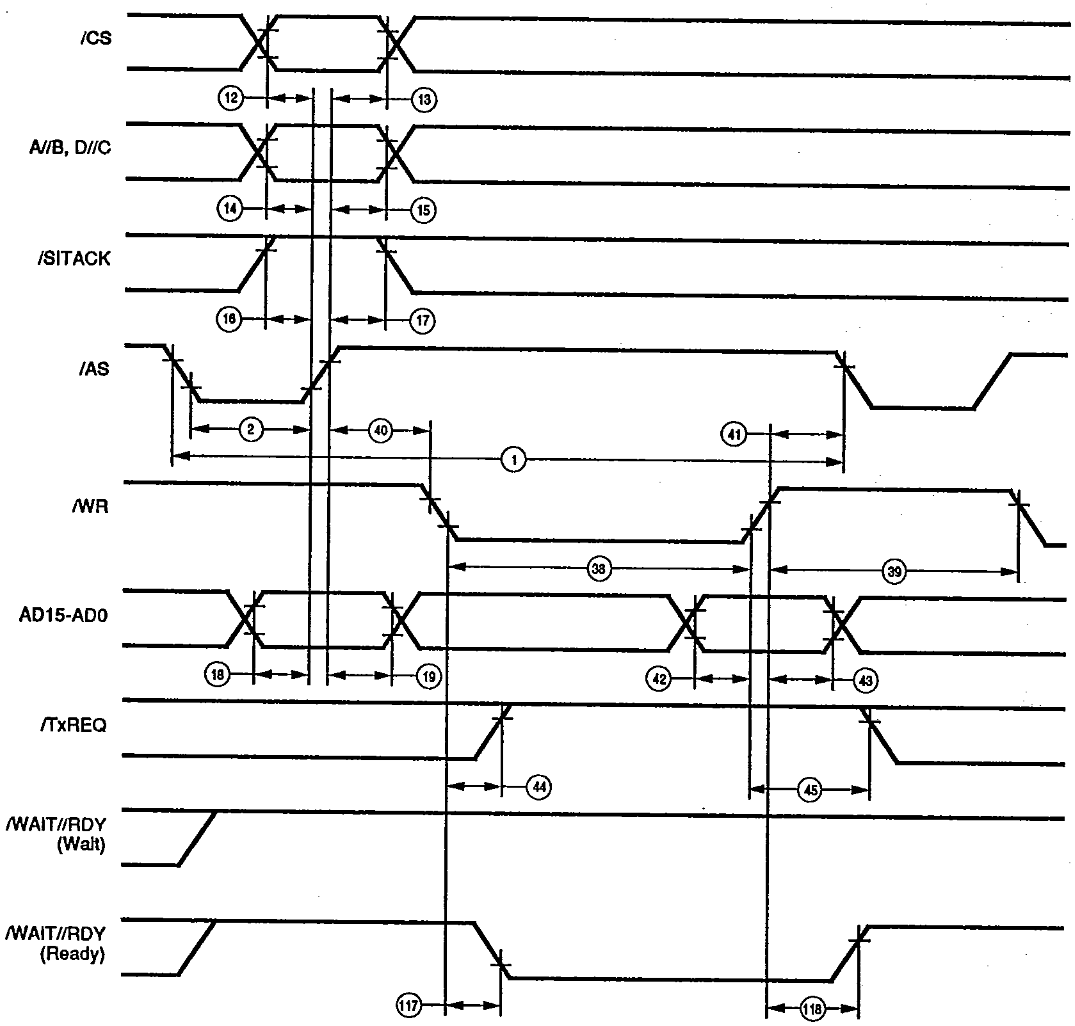

Figure 62. Multiplexed /WR Write Cycle

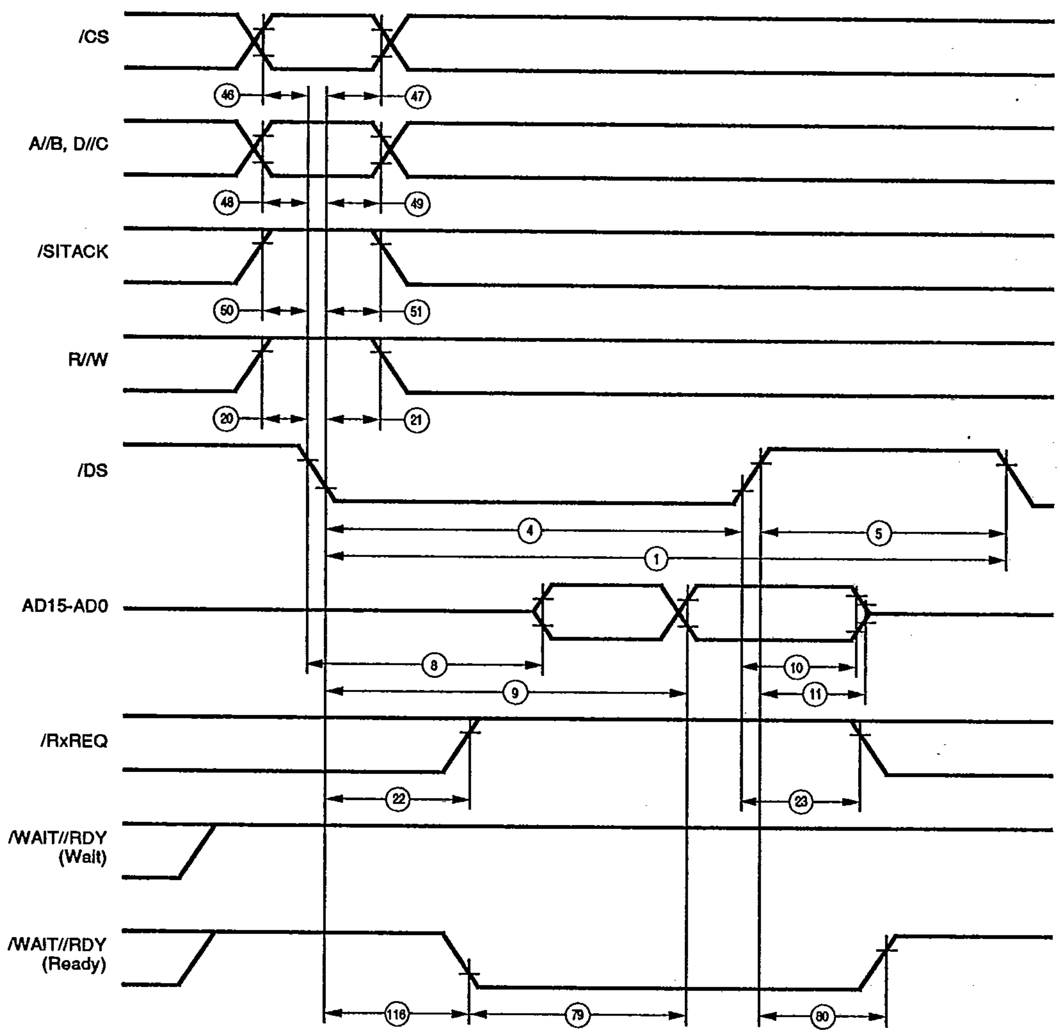

Figure 63. Non-Multiplexed /DS Read Cycle

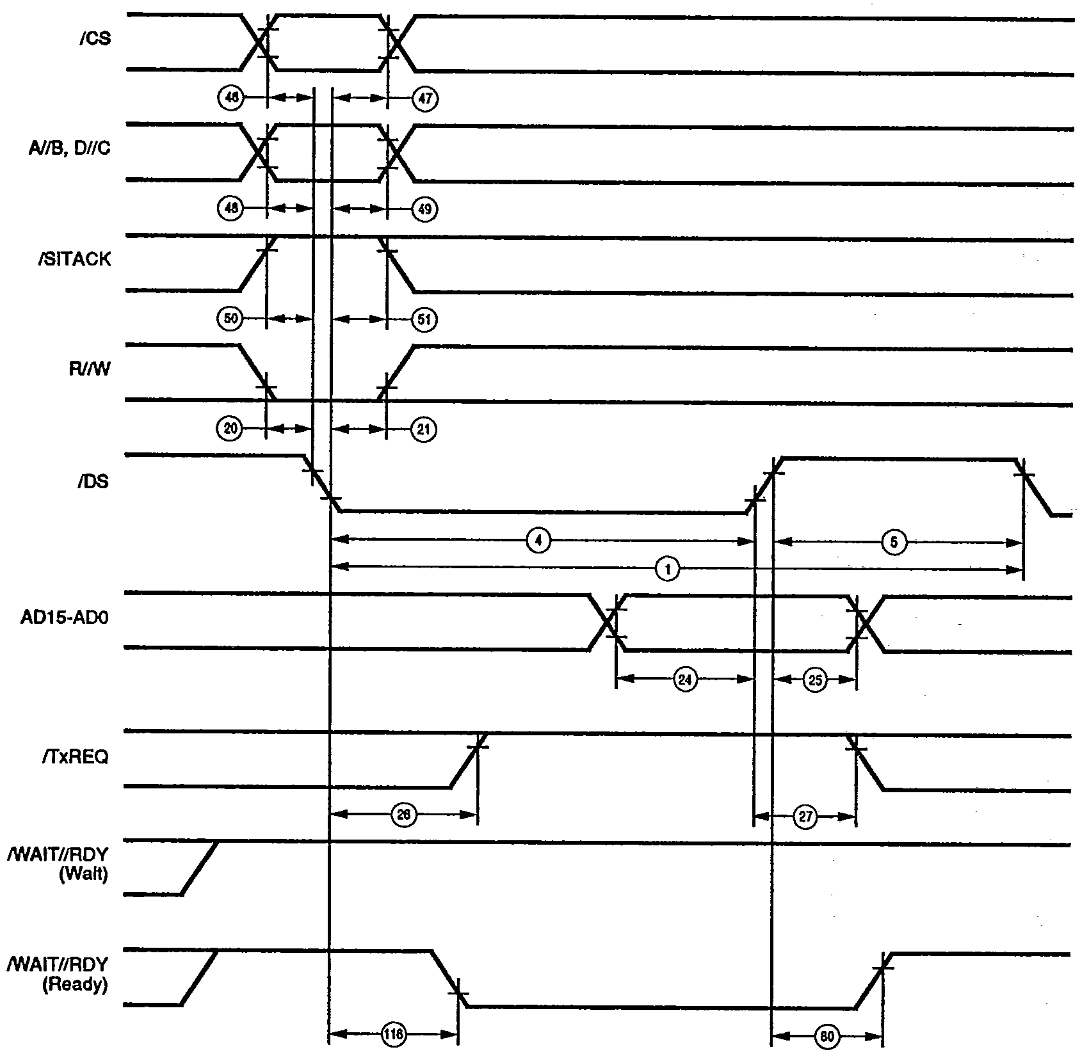

Figure 64. Non-Multiplexed /DS Write Cycle

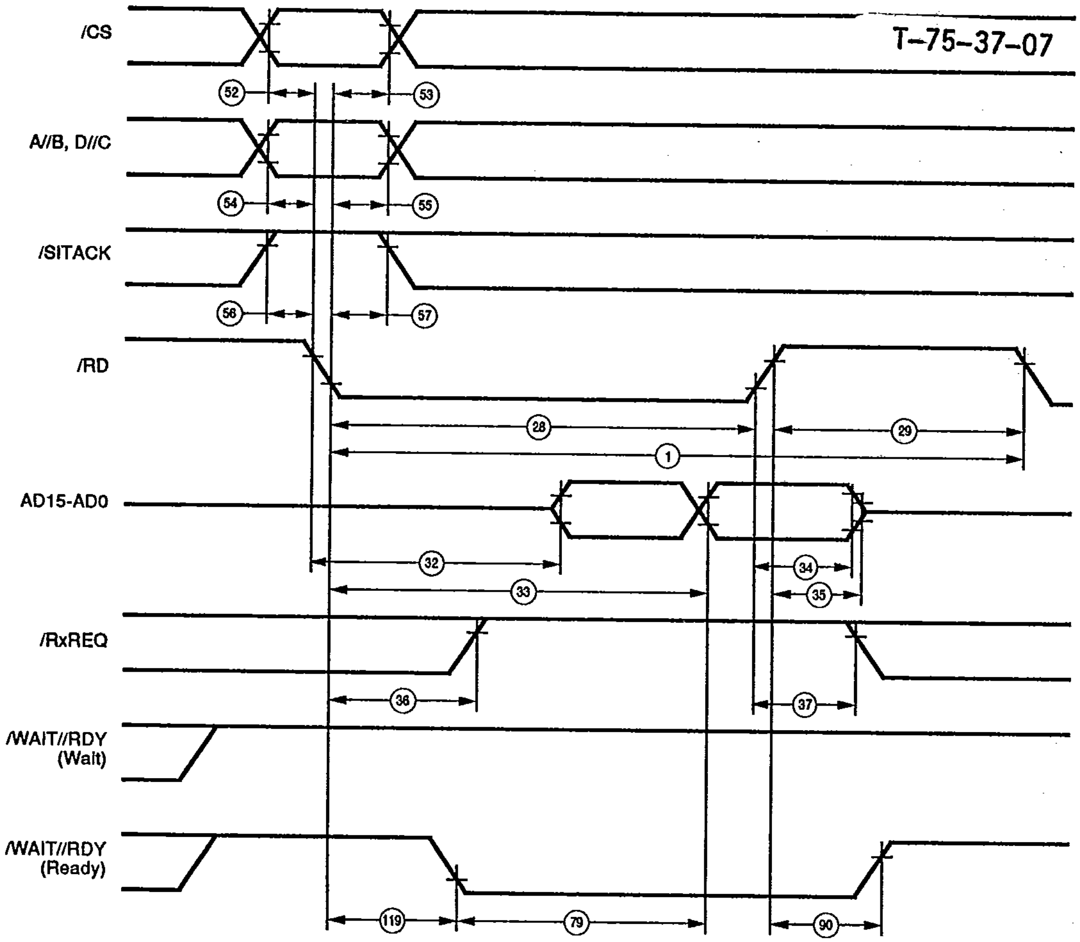

Figure 65. Non-Multiplexed /RD Read Cycle

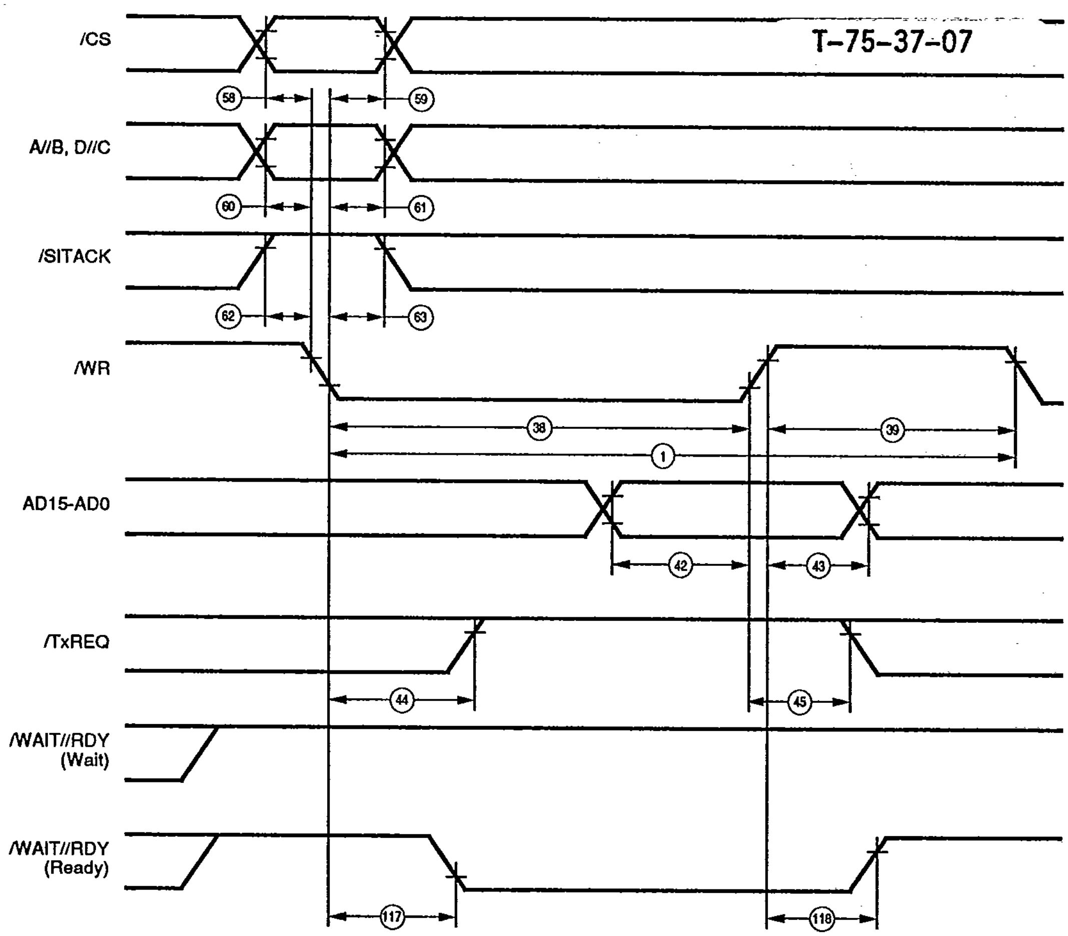

Figure 66. Non-Multiplexed /WR Write Cycle

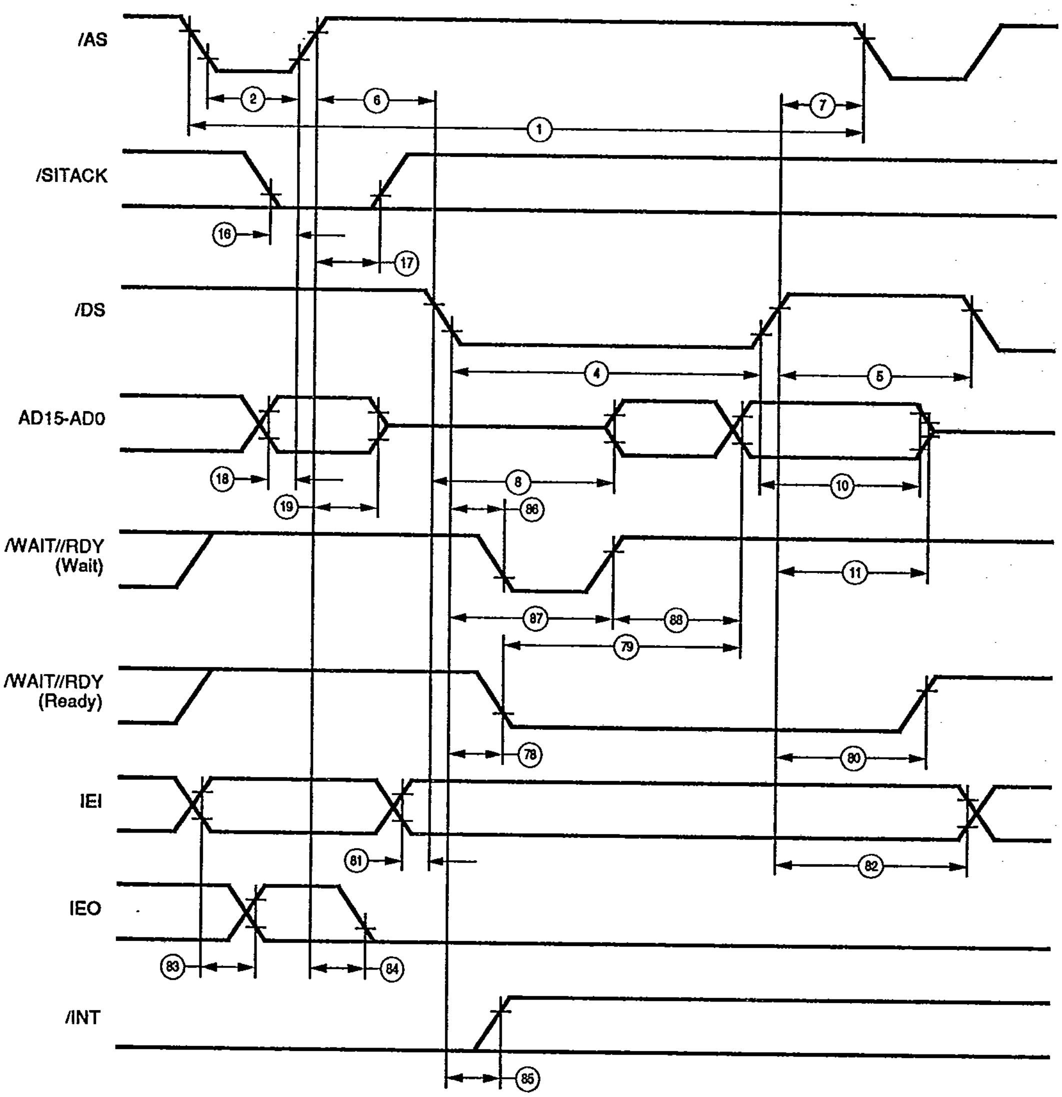

Figure 67. Multiplexed /DS Interrupt Acknowledged Cycle

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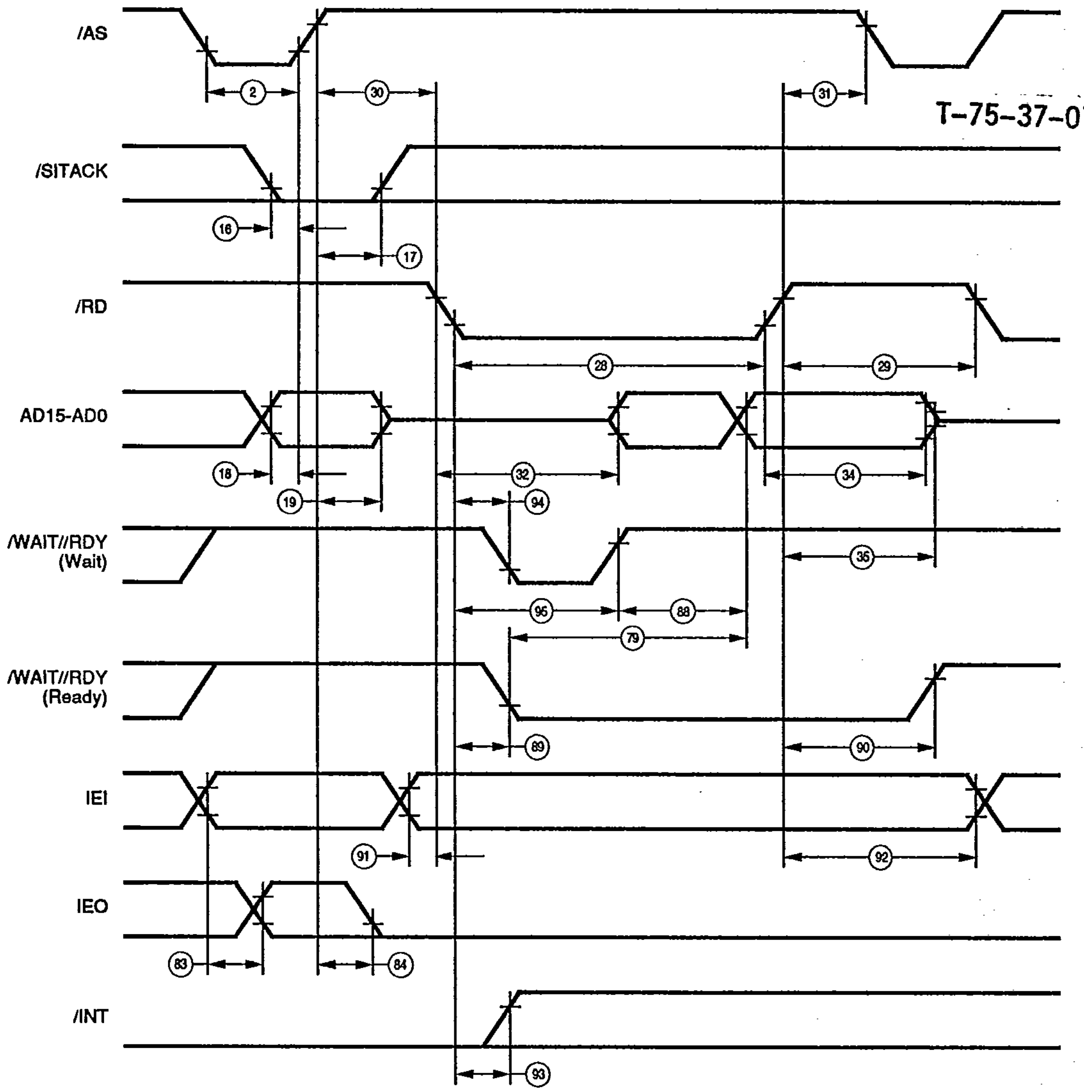

Figure 68. Multiplexed /RD Interrupt Acknowledge Cycle

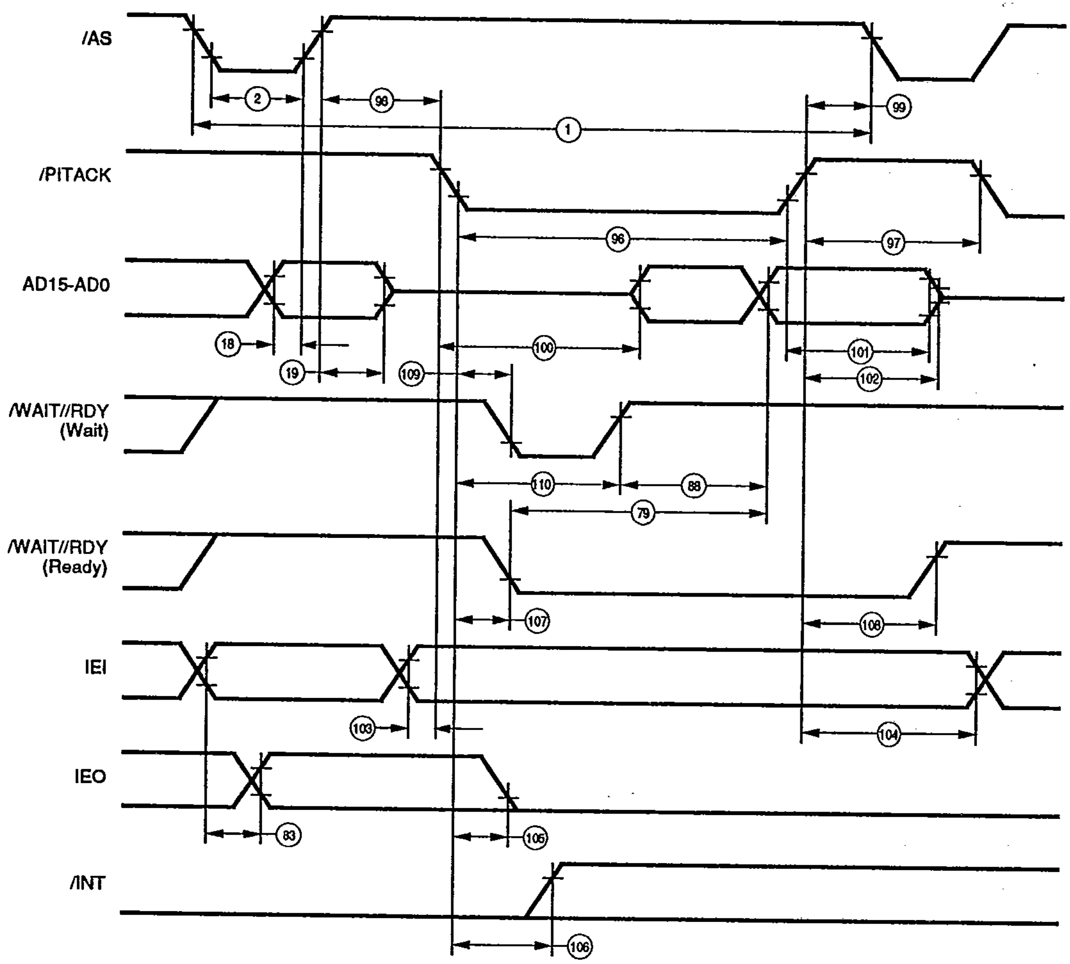

Figure 69. Multiplexed Pulsed Interrupt Acknowledge Cycle

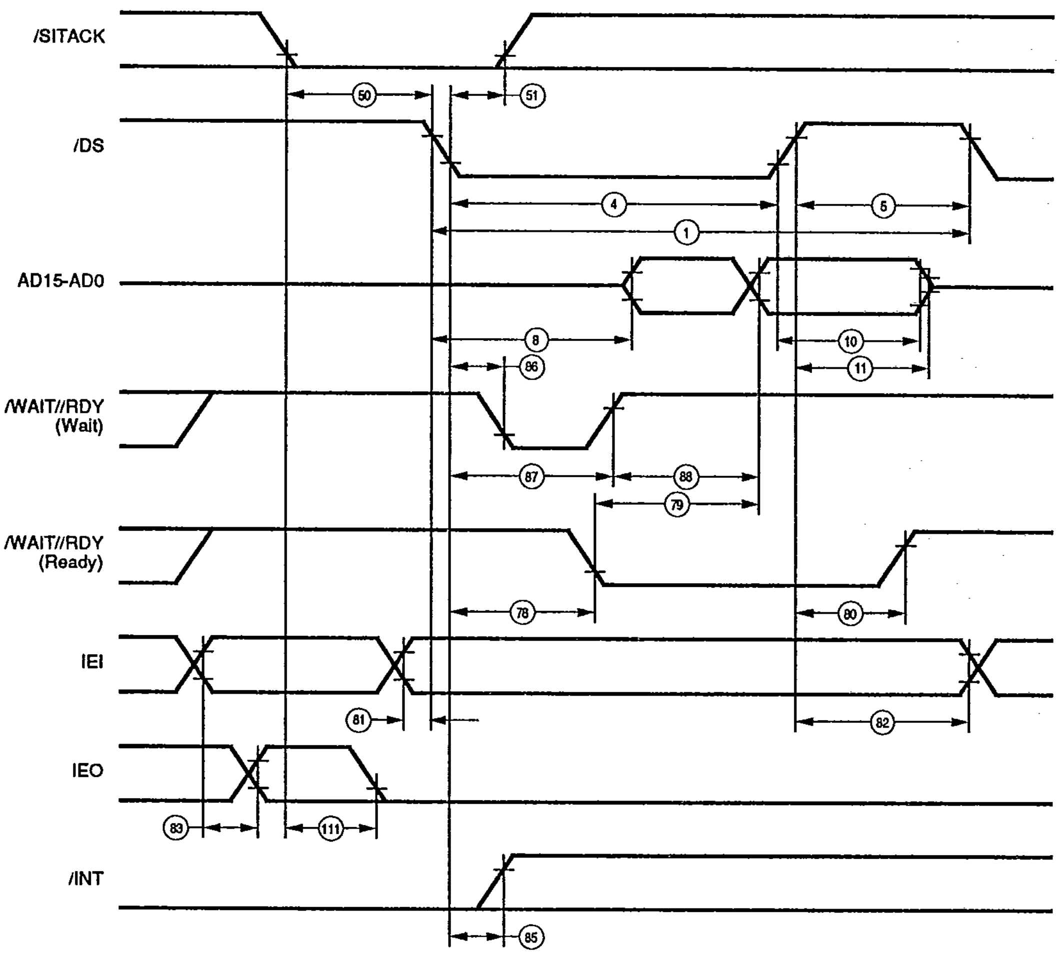

Figure 70. Non-MUX /DS Interrupt Acknowledge Cycle

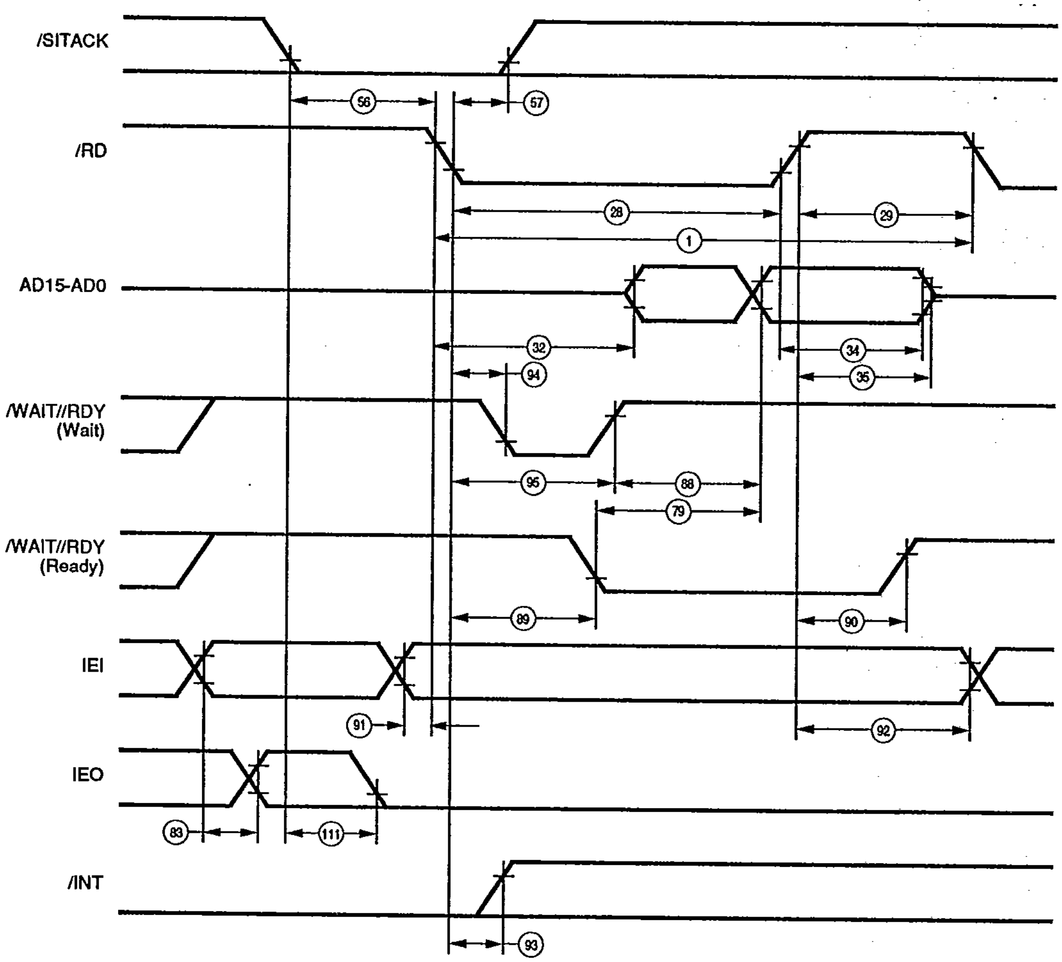

Figure 71. Non-MUX Pulsed Interrupt Acknowledge Cycle

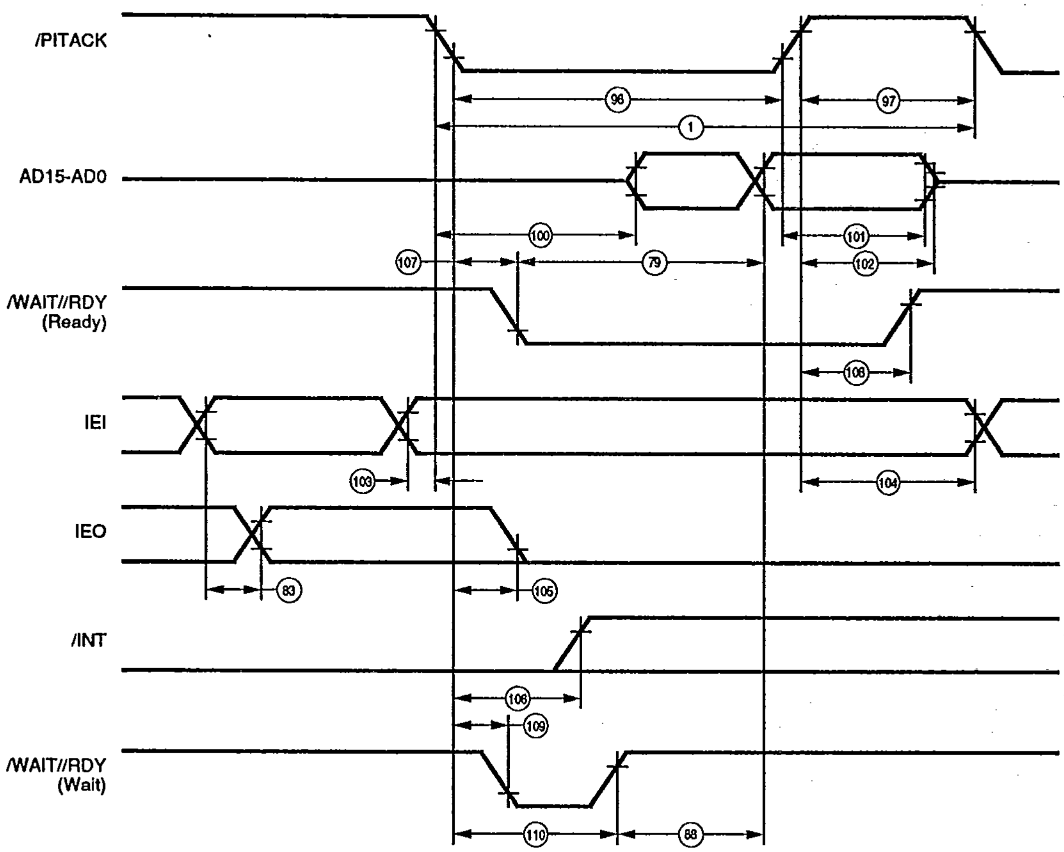

Figure 72. Non-MUX /RD Interrupt Acknowledge Cycle

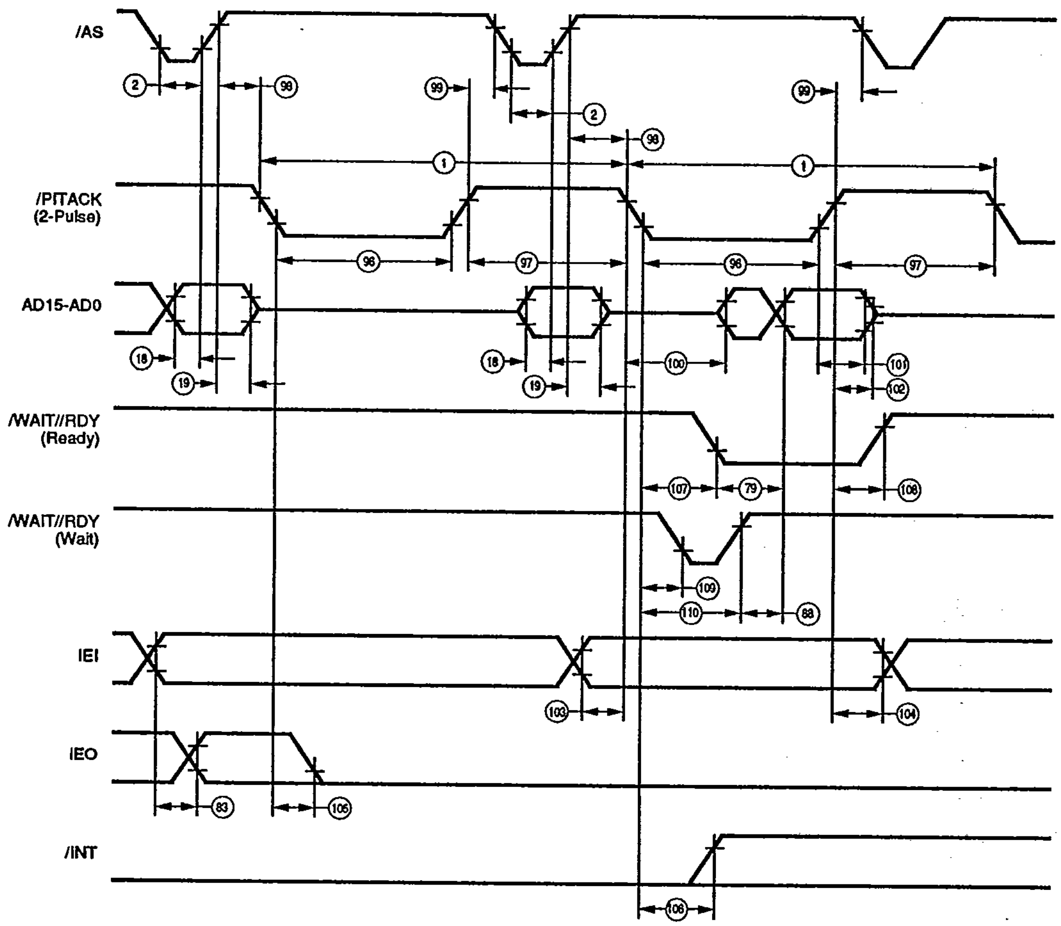

Figure 73. Multiplexed Double-Pulse Intack Cycle

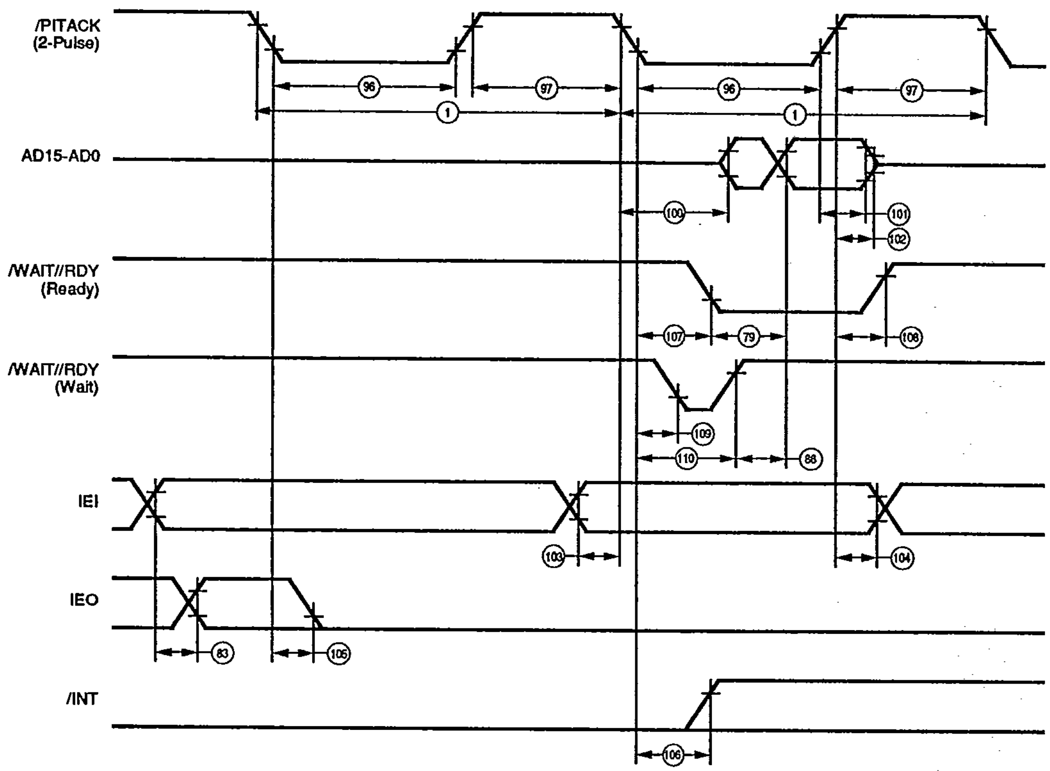

Figure 74. Non-Multiplexed Double-Pulse Intack Cycle

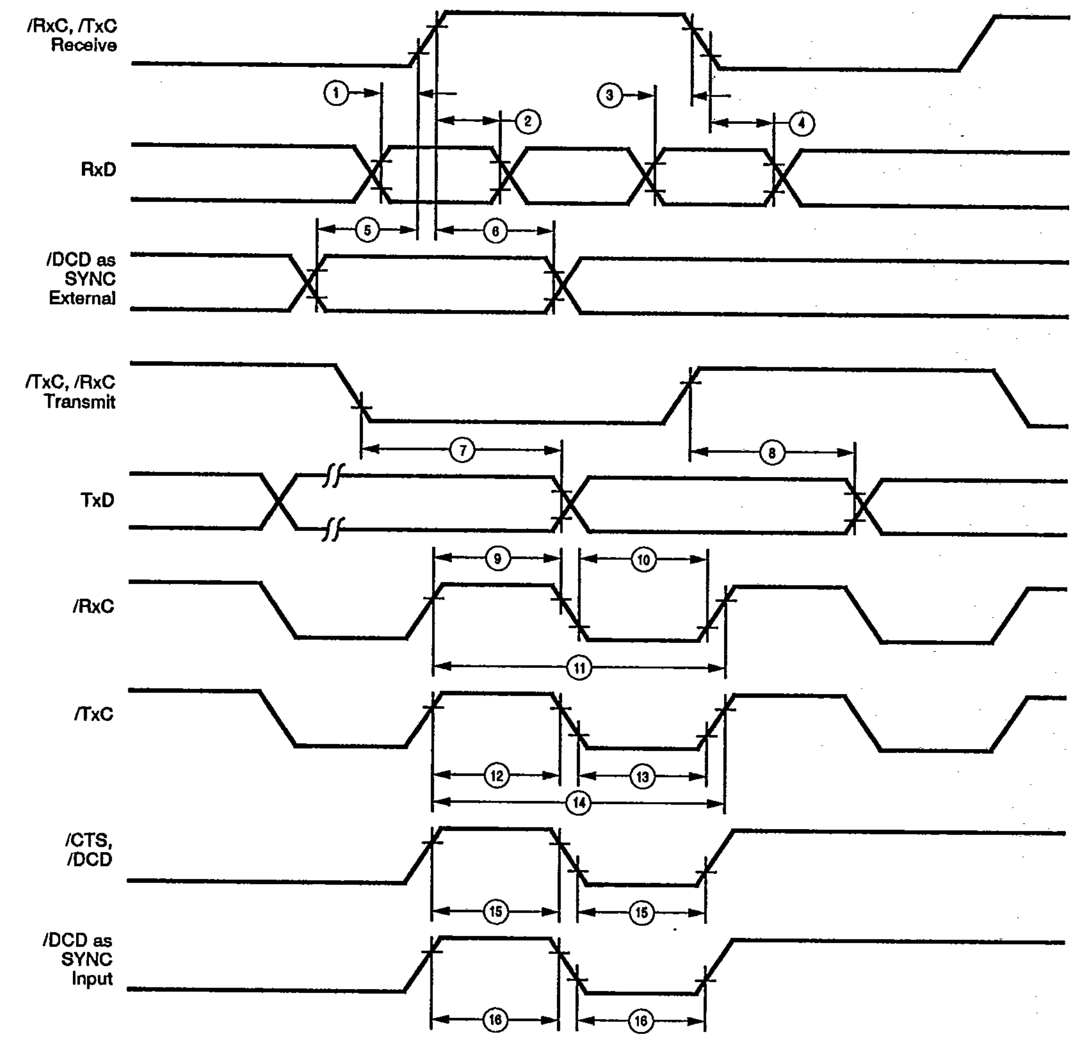

Figure 75. Z16C30 General Timing

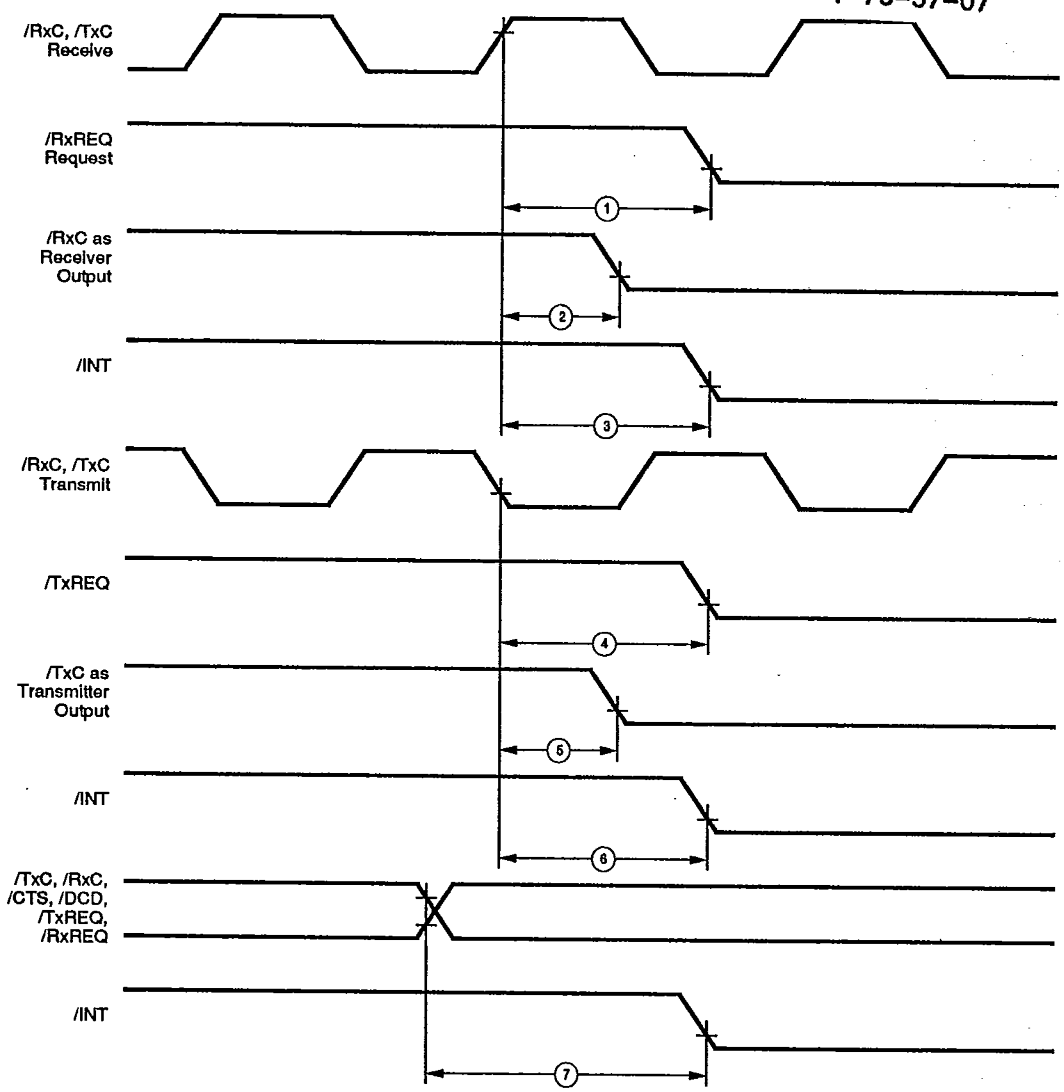

Figure 76. Z16C30 System Timing

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AC CHARACTERISTICS
Z16C30 General Timing

No	Symbol	Parameter	10 MHz Min	10 MHz Max	Notes
1	TsRxD(RxCr)	RxD to /RxC↑ Setup Time (x1 Mode)	0		[1]
2	ThRxD(RxCr)	RxD to /RxC↑ Hold Time (x1 Mode)	40		[1]
3	TsRxd(RxCf)	RxD to /RxC↓ Setup Time (x1 Mode)	0		[1,4]
4	ThRxD(RxCf)	RxD to /RxC↓ Hold Time (x1 Mode)	40		[1,4]
5	TsSy(RxC)	/DCD as /SYNC to /RxC↑ Setup Time	0		[1]
6	ThSy(RxC)	/DCD as /SYNC to /RxC↑ Hold Time (x1 Mode)	40		[1]
7	TdTxCf(TxD)	/TxC↓ to TxD Delay		50	[2]
8	TdTxCr(TxD)	/TxC↑ to TxD Delay		50	[2,4]
9	TwRxCh	/RxC High Width	40		
10	TwRxCl	/RxC Low Width	40		
11	TcRxC	/RxC Cycle Time	100		
12	TwTxCh	/TxC High Width	40		
13	TwTxCl	/TxC Low Width	40		
14	TcTxC	/TxC Cycle Time	100		
15	TwExT	/DCD or /CTS Pulse Width	70		
16	TWSY	/DCD as /SYNC Input Pulse Width	70		

AC CHARACTERISTICS
Z16C30 System Timing

No	Symbol	Parameter	10 MHz Min	10 MHz Max	Notes
1	TdRxC(REQ)	/RxC↑ to /RxREQ Valid Delay		100	[2]
2	TdRxC(RxC)	/TxC↑ to /RxC as Receiver Output Valid Delay		100	[2]
3	TdRxC(INT)	/RxC↑ to /INT Valid Delay		100	[2]
4	TdTxC(REQ)	/TxC↓ to /TxREQ Valid Delay		100	[3]
5	TdTxC(TxC)	/RxC↓ to /TxC as transmitter Output Valid Delay		100	
6	TdTxC(INT)	/TxC↓ to /INT Valid Delay		100	[3]
7	TdEXT(INT)	/CTS, /DCD, /TxREQ, /RxREQ transition to /INT Valid Delay		100	

Notes:
[1] /RxC is /RxC or /TxC, whichever is supplying the receive clock.
[2] /TxC is /TxC or /RxC, whichever is supplying the transmit clock.
[3] /TxC is /TxC or /RxC, whichever is supplying the transmit clock.
[4] Parameter applies only to FM encoding/decoding.

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MIL-STD-883 MILITARY PROCESSED PRODUCT

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/Quality Conformance testing required.

Zilog Military Product Flow

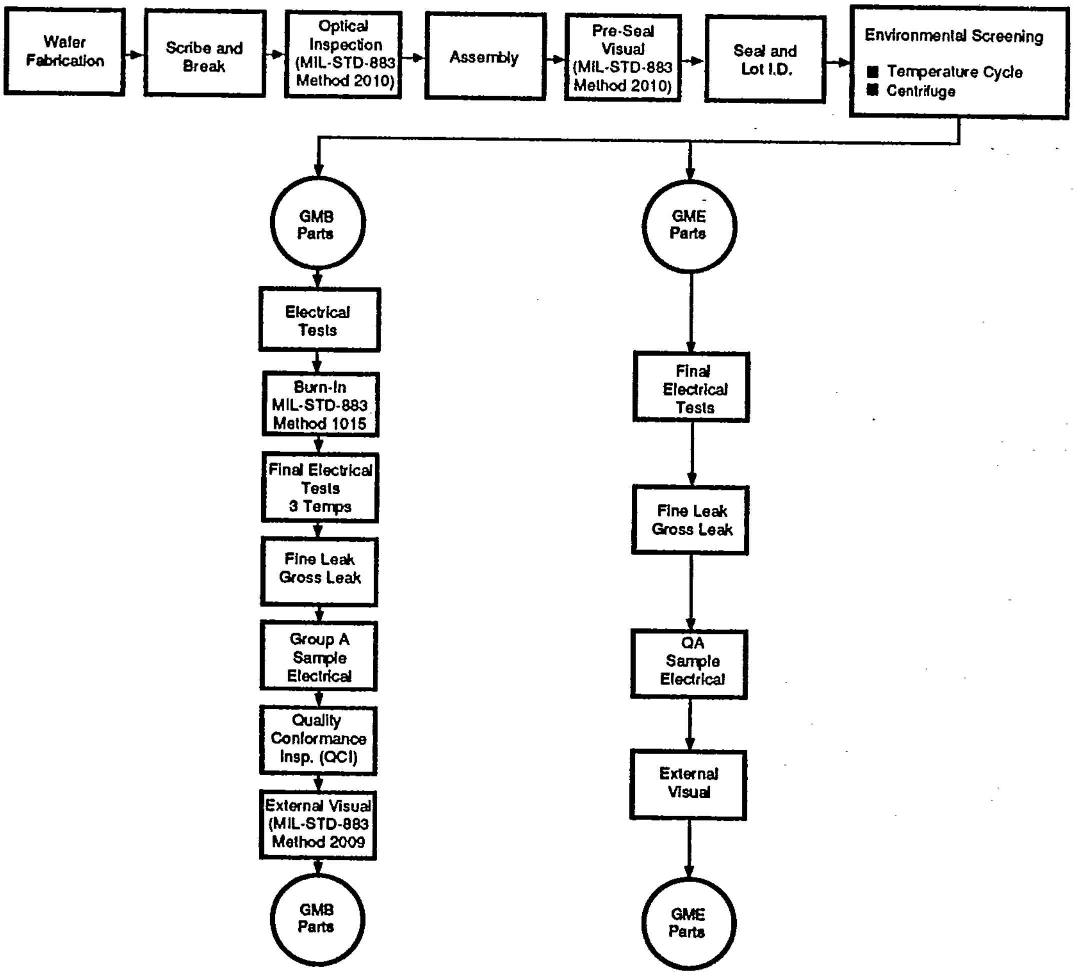

Table I
MIL-STD-883 Class B Screening Requirements
Method 5004

Test		Mil-Std-883 Method	Test Condition	Requirement
Internal Visual		2010	Condition B	100%
Temperature Cycle		1010	Condition C	100%
Constant Acceleration (Centrifuge)		2001	Condition E or D(Note 1), Y_1 Axis Only	100%
Initial Electrical Tests			Zilog Military Electrical Specification Static/DC $T_C = +25°C$	100%
Burn-In		1015	Condition D(Note 2), 160 hours, $T_A = +125°C$	100%
Interim Electrical Tests			Zilog Military Electrical Specification Static/DC $T_C = +25°C$	100%
PDA Calculation			PDA = 5%	100%
Final Electrical Tests			Zilog Military Electrical Specification Static/DC $T_C = +125°C, -55°C$ Functional, Switching/AC $T_C = +25°C$	100%
Fine Leak		1014	Condition B	100%
Gross Leak		1014	Condition C	100%
Quality Conformance Inspection (QCI)				
Group A	Each Inspection Lot	5005	(See Table II)	Sample
Group B	Every Week	5005	(See Table III)	Sample
Group C	Periodically (Note 3)	5005	(See Table IV)	Sample
Group D	Periodically (Note 3)	5005	(See Table V)	Sample
External Visual		2009		100%
QA—Ship				100%

NOTES:
1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).

Table II Group A

Sample Electrical Tests
MIL-STD-883 Method 5005

Subgroup	Tests	Temperature (T_C)	LTPD Max Accept = 2
Subgroup 1	Static/DC	+25°C	2
Subgroup 2	Static/DC	+125°C	3
Subgroup 3	Static/DC	−55°C	5
Subgroup 7	Functional	+25°C	2
Subgroup 8	Functional	−55°C and +125°C	5
Subgroup 9	Switching/AC	+25°C	2
Subgroup 10	Switching/AC	+125°C	3
Subgroup 11	Switching/AC	−55°C	5

NOTES:
- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

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Table III Group B

Sample Test Performed Every Week to Test Construction and Insure Integrity of Assembly Process. MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1 Physical Dimensions	2016		2/0
Subgroup 2 Resistance to Solvents	2015		4/0
Subgroup 3 Solderability	2003	Solder Temperature $+245°C \pm 5°C$	15(Note 1)
Subgroup 4 Internal Visual and Mechanical	2014		1/0
Subgroup 5 Bond Strength	2011	C	15(Note 2)
Subgroup 6(Note 3) Internal Water Vapor Content	1018	1000 ppm. maximum at +100°C	3/0 or 5/1
Subgroup 7(Note 4) Seal 7a) Fine Leak 7b) Gross Leak	1014	 7a) B 7b) C	5
Subgroup 8(Note 5) Electrostatic Discharge Sensitivity	3015	Zilog Military Electrical Specification Static/DC $T_C = +25°C$ A = 20-2000V B = >2000V Zilog Military Electrical Specification Static/DC $T_C = +25°C$	15/0

NOTES

1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

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Table IV Group C

Sample Test Performed Periodically to Verify Integrity of the Die.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Steady State Operating Life	1005	Condition D(Note 1), 1000 hours at +125°C	5
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	

NOTE
1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.

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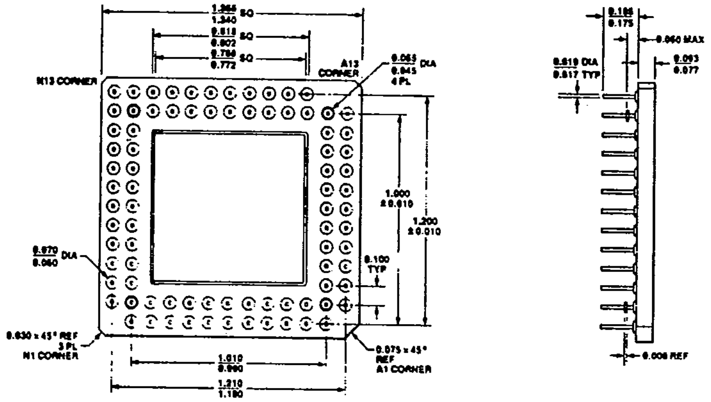
Table V Group D

Sample Test Performed Periodically to Insure Integrity of the Package.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Condition B_2 or D(Note 1)	15
Subgroup 3			
Thermal Shock	1011	Condition B minimum, 15 cycles minimum	
Temperature Cycling	1010	Condition C, 100 cycles minimum	15
Moisture Resistance	1004		
Seal	1014		
3a) Fine Leak		3a) Condition B	
3b) Gross Leak		3b) Condition C	
Visual Examination	1004 or 1010		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 4			
Mechanical Shock	2002	Condition B minimum	
Vibration Variable Frequency	2007	Condition A minimum	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	15
Seal	1014		
4a) Fine Leak		4a) Condition B	
4b) Gross Leak		4b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 5			
Salt Atmosphere	1009	Condition A minimum	
Seal	1014		15
5a) Fine Leak		5a) Condition B	
5b) Gross Leak		5b) Condition C	
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm. maximum water content at +100°C	3/0 or 5/1
Subgroup 7(Note 3)			
Adhesion of Lead Finish	2025		15(Note 4)
Subgroup 8(Note 5)			
Lid Torque	2024		5/0

NOTES:
1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

PACKAGE INFORMATION



68-Pin PGA Package

ORDERING INFORMATION

T-75-37-07

Z16C30 USC

10 MHz
68-Pin PGA Package
Z16C3010GMB
Z16C3010GME

CODES

PACKAGE
G = PGA Package

TEMPERATURE
M = -55°C to +125°C

ENVIRONMENTAL
E = Hermetic Standard
B = 833 Class B Military Flow

Example:
Z16C3010GMB is a 16C30, 10 MHz, 68-Pin PGA, -55°C to +125°C, Processed to Class B, Mil-Std-883C

Z 16C30 10 G M B

- B — Environmental Flow
- M — Temperature
- G — Package
- 10 — Speed
- 16C30 — Product Number
- Z — Zilog Prefix