PRELIMINARY PRODUCT SPECIFICATION

Z16C50

DDPLL DUAL DIGITAL PHASE LOCKED LOOP MICROCONTROLLER

FEATURES

- Two independent Digital Phase Locked Loops in one package.
- 10 MHz and 20 MHz Clock operation
- Selectable clock rate, clock sampling edge, and data decoding.
- Synchronous status output
- Accept Code Violation input
- Implemented in 1.6µ CMOS technology
- 28-pin DIP package

GENERAL DESCRIPTION

The 16C50 DDPLL is a fully static CMOS device that packs two independent Digital Phase Locked Loops, with separate controls for selecting the decoding mode, clock rate, and synchronization edge, in one integrated package (Figure 1). The only common input between the two phase locked loops is /RESET (/ denotes active low signal).

The DDPLL is used in many communication applications requiring detection and extraction of clock from data. It can be used together with Serial Communication Controllers to allow operation at higher data rates. The data rate is programmable at 1/8, 1/16, or 1/32 clock rate. The DDPLL is offered in two speed grades: 10MHz and 20MHz maximum clock speed, which translates to a maximum data rate of 1.25 Mbps and 2.5 Mbps, respectively.

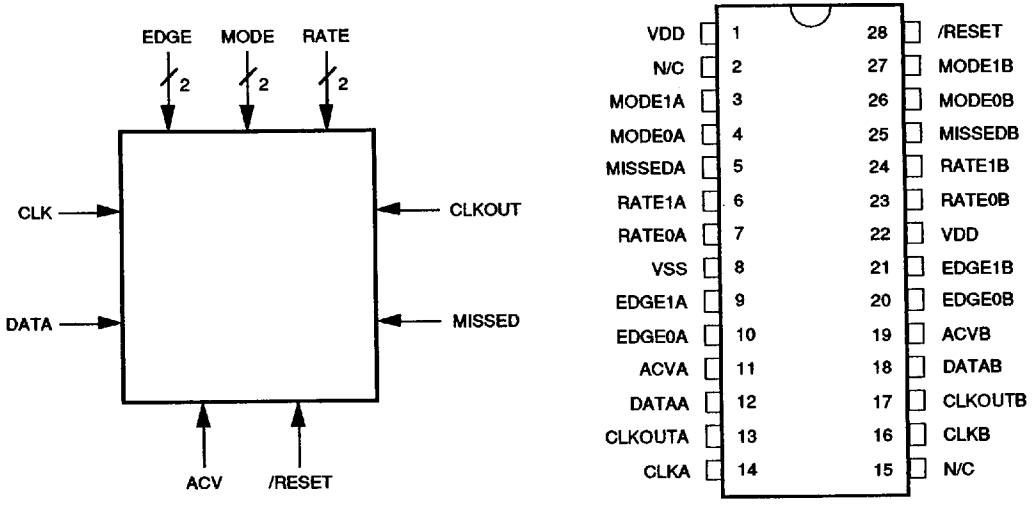

Figure 1. DDPLL Block and Pin Diagrams

PIN DESCRIPTION

The following is a list of DDPLL pins and their descriptions. "A" and "B" at the end of pin names designate the signal connecting to the A- or B-channel of the DDPLL.

ACVA, ACVB. *Accept Code Violation* (input, active HIGH). The ACV signal is used to control the response of the DDPLL to code violations present in the received data stream.

CLKA, CLKB Clock. *Input* (input, active HIGH). The Clock runs at 8-, 16-, or 32-times the received data rate and is used by the DDPLL to generate the CLKOUT signal.

CLKOUTA, CLKOUTB. *Clock Output* (output, active HIGH). CLKOUT is the recovered clock for the receive data stream. The receiver should use this clock to sample and decode the received data.

DATAA, DATAB. *Receive Data* (input, active HIGH). The DATA signal is the received data stream that the DDPLL is attempting to synchronize with. The DDPLL will provide the CLKOUT signal for use by a receiver attempting to decode this data stream.

EDGE0A, EDGE0B, EDGE1A, EDGE1B. *Adjust/Synchronize Edge Controls* (input, active HIGH). These signals select which edge is used by the DDPLL to achieve and maintain synchronization.

MISSEDA, MISSEDB. *Clock Missed* (output, active HIGH). MISSED signal is activated when the DDPLL detects missing edge(s) in the data stream.

MODE0A, MODE0B, MODE1A, MODE1B. *DDPLL Mode Controls* (input, active HIGH). MODE0 and MODE1 are used to control the mode of operation of the DDPLL with respect to the encoded format of the incoming data.

RATE0A, RATE0B, RATE1A, RATE1B. *Clock Rate Selects* (input, active HIGH). RATE inputs are used to select the data rate divisor to generate the DDPLL clock.

/RESET. *Reset* (input, active LOW). This input resets the DDPLL to a known state and must be active for at least two cycles of the slowest CLK signal. This is the only common input to the two Digital Phase Locked Loops.

VDD. +5V supply.

VSS. 0V (GND) supply.

FUNCTIONAL DESCRIPTION

Prior to device operation, the control inputs of the DDPLL must be set to known states corresponding to the desired mode of operation.

Data decoding format is programmed via MODE0 and MODE1 inputs. Table 1 demonstrates the truth table for these inputs. NRZ, NRZI, FM1 (biphase mark), FM0 (biphase space) and Manchester (biphase level) formats are supported. MODE1-MODE0 of LOW-LOW disables the DDPLL, setting the CLKOUT output LOW. In NRZ format, a "1" is represented by a HIGH level and a "0" is represented by a LOW level. In NRZI format, a "1" is represented by no change in level and a "0" is represented by a change in level. A MODE1-MODE0 of LOW-HIGH selects the NRZ or NRZI decoding modes.

Table 1. Mode Selection Truth Table

MODE1	MODE0	Selected Mode
0	0	Disable/Sync
0	1	NRZ/NRZI
1	0	Biphase-Mark/Space
1	1	Biphase-Level

In both of these modes, transitions on the input may only occur on bit cell boundaries and the DDPLL provides CLKOUT to match these bit cell boundaries. In FM1 (biphase mark) and FM0 (biphase space) formats, a transition occurs at the beginning of every bit cell. In addition to this, in FM1, a "1" is represented by an additional transition at the center of the bit cell and a "0" is represented by the absence of such transition. In contrast, in FM0, a "0" is represented by an additional transition at the center of the bit cell and a "1" is represented by the absence of such transition. MODE1-MODE0 of HIGH-LOW selects the biphase-mark (FM1) or biphase-space (FM0) modes.

In Manchester (biphase level) mode, a transition occurs at the center of every bit cell. If the bit is "1", the transition is HIGH to LOW, and if the bit is "0", the transition is LOW to HIGH. Additionally, a LOW to HIGH transition occurs at the boundary of a "1" bit. A HIGH-HIGH selects the Manchester (biphase level) mode. Figure 2 demonstrates an example of a serial data stream with its corresponding encoded waveforms in NRZ, NRZI, FM1, FM0, and Manchester modes.

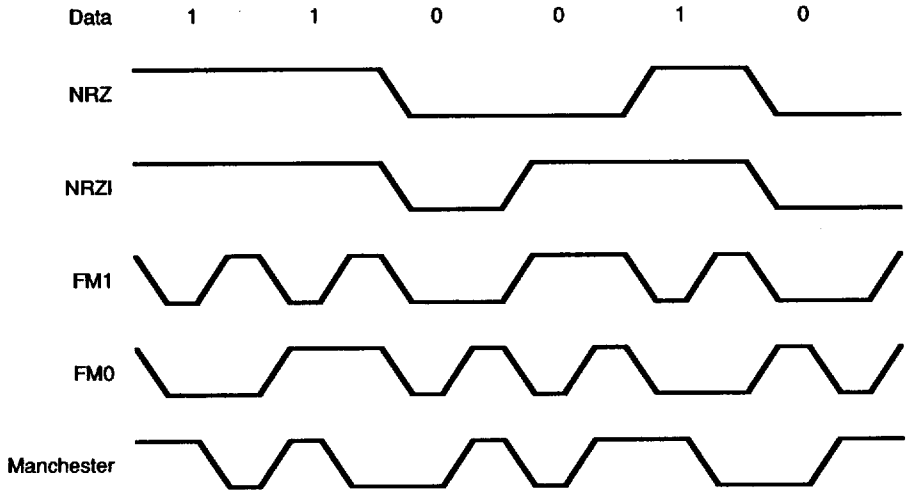

Figure 2. Data Decoding Formats

Clock rate is programmed through RATE1-RATE0 inputs. Clock rate can be set for 8-, 16-, or 32-times the data rate. With maximum clock operation of 20MHz in 8X mode, data rates of 2.5Mbps is achieved. Table 2 illustrates clock rate divisor's truth table. Note that RATE1-RATE0 of HIGH-HIGH is illegal. All DDPLL inputs (with the exception of /RESET) are sampled by the rising edge of CLK and all outputs change state in response to the rising edge of the CLK signal. The two DPLLs are completely independent except for the /RESET input.

Table 2. Data Rate Divisor Truth Table

RATE1	RATE0	Data Rate Divisor
0	0	32X Clock Mode
0	1	16X Clock Mode
1	0	8X Clock Mode
1	1	Not Allowed

EDGE1 and EDGE0 select the edge(s) in the receive data stream used by the DDPLL to achieve and maintain synchronization. Table 3 shows how the rising edge, the falling edge, or both edges of the receive data stream can be used for synchronization. A HIGH on both EDGE inputs inhibits the DDPLL from using either edge for synchronization. As far as the DDPLL is concerned, edges that are not used to achieve or maintain synchronization are not present. They are reported as missing edges when they occur where an edge is expected.

Table 3. Clock Edge Selection Truth Table

EDGE1	EDGE0	Selected Edge
0	0	Both Edges
0	1	Rising Edge
1	0	Falling Edge
1	1	Adjust/Sync Inhibit

The response of the DDPLL to code violations present in the received data stream can be controlled using the ACV input. This signal is ignored in the NRZ/NRZI mode, where code violations are not possible. In all other modes, however, a HIGH on the ACV allows the DDPLL to recognize an isolated code violation without losing synchronization. Code violations are then used by the receiver for synchronization.

When the DDPLL detects missing edge(s) in the data stream, it activates the MISSED output. If the DDPLL is configured to accept code violations, two consecutive code violations will activate the MISSED output. If the DDPLL is configured not to accept code violations, this output is activated on any missing clock. MISSED will never be activated in the NRZ/NRZI modes of operation, as code violations are not possible in these modes. The DDPLL re-enters the sync-up phase when the MISSED output is activated.

The CLKOUT is the recovered Clock for the receive data stream. The receiver uses this clock to sample and decode the received data.

The only common input between the two phase locked loops in the DDPLL is the /RESET input. This signal must remain active for at least two cycles of the slowest CLK signal and resets the device to a known state: MISSED=LOW and CLKOUT=LOW. Synchronization attempt begins once the /RESET signal is deactivated.

ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to GND ..... -0.3V to +7.0V
Operating Ambient Temperature ..... See Ordering Information
Storage Temperature ..... -65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and Capacitance section below apply for the following standard test conditions, unless otherwise noted (Figure 3). All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

$+4.5\ V < V_{CC} < +5.5\ V$
GND = 0 V
T_A as specified in Ordering Information

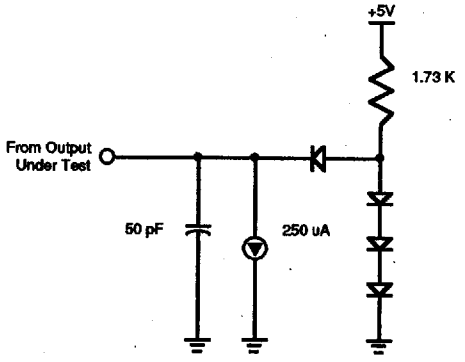

Figure 3. Standard Test Load

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Conditions
V_{IH}	Input High Voltage	2.0	V_{DD}+0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{OL}	Output High Voltage	2.4		V	1OH = -1.6mA
I_{IL}	Input Leakage Current		±10	µA	$0.4V \le V_{IN} \le 2.4V$
I_{CC}	Supply Current		40	mA	V_{DD}=5, V_{IH}=4.8V, V_{IL}=0.2V
C_{IN}	Input Capacitance		10	pf	Unmeasured pins returned to GND
C_{OUT}	Output Capacitance		15	pf	Unmeasured pins returned to GND

Notes:

1. V_{DD}=5V ±10% unless otherwise specified, over specified temperature range.
2. Capacitance values specified at f=1MHz.

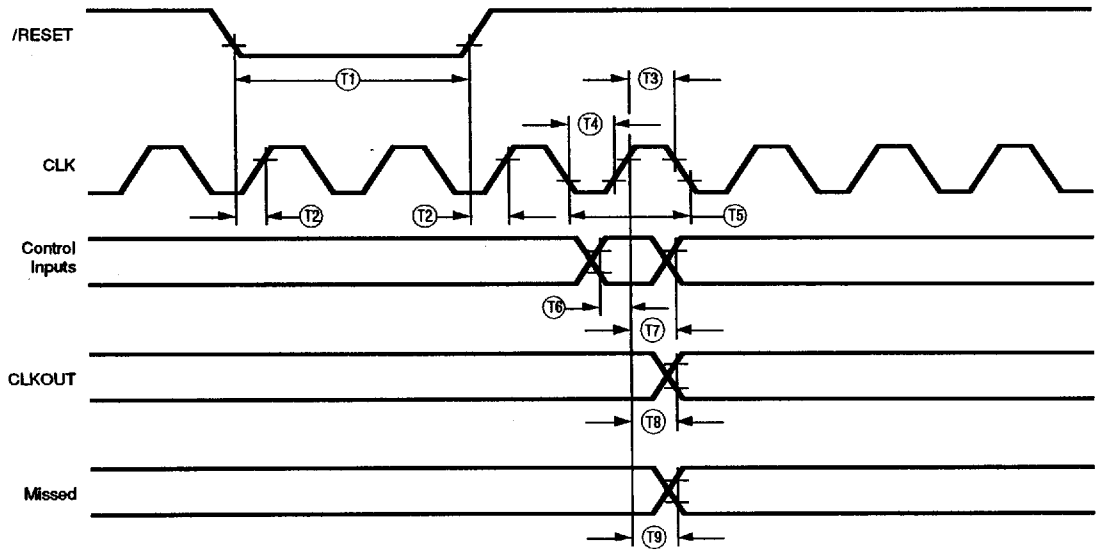

Figure 4. DDPLL Timing Diagram

Figure 2 illustrates the DDPLL timings. "Control Inputs" in Figure 4 refer to MODE1-MODE0, RATE1-RATE0, EDGE1-EDGE0, and ACV inputs.

AC CHARACTERISTICS

Timing	Symbol	Parameter	Z16C5010 Min	Z16C5010 Max	Z16C5020 Min	Z16C5020 Max	Units	Notes
T1	TwRESl	/RESET LOW Width	2TcC		2TcC			
T2	TsRES(CLK)	/RESET to CLK Setup Time	15		15		ns	
T3	TwCLKh	CLK HIGH Time	40		20		ns	
T4	TwCLKl	CLK Low Time	40		20		ns	
T5	TcC	CLK Cycle Time	100		50		ns	
T6	TsIN(CLK)	Input Valid to CLK Setup Time	15		15		ns	1,2,3
T7	ThIN(CLK)	Input Valid to CLK Hold Time	10		10		ns	1,2,3
T8	TdCLK(OUT)	CLK to CLKOUT Delay Time		30		30	ns	
T9	TdCLK(MIS)	CLK to MISSED Delay Time		30		30	ns	