SGS-THOMSON MICROELECTRONICS

ST75C540

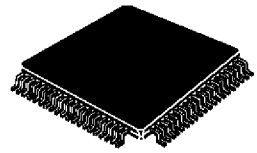
HIGH SPEED FAX, MODEM, ANSWERING MACHINE, HANDS-FREE DEVICE

PRELIMINARY DATA

- SINGLE CHIP FAX :
  - ITU-T V.17, V.29, V.27ter, V.21 WITH FAX SUPPORT
  - V.17, V.29 (T104), V.27ter SHORT TRAINS, V.33 HALF-DUPLEX
  - V.21 FLAG DETECTION AND 4 TONE DETECTION DURING HIGH SPEED RECEPTION MODES
  - V.21 FLAG DETECTION, DTMF DETECTION AND 4 TONE DETECTION DURING V.21 CHANNEL 2 RECEPTION MODES
  - PROGRAMMABLE CALL PROGRESS AND CALL WAITING DETECTION
  - PARALLEL DATA HANDLING
  - HDLC AND UART FRAMING SUPPORT
  - 1700Hz AND 1800Hz CARRIER
  - FULL IMPLEMENTATION OF THE V.17, V.33, V.29 AND V.27 HANDSHAKES
  - 0 TO -15dBm PROGRAMMABLE TRANSMIT POWER
  - 0 TO -47dBm RECEIVER DYNAMIC RANGE
- FULL DUPLEX DATA MODEM
  - ITU-T V.32BIS, V.32 (14400, 12000, 9600, 7200, 4800bps)
  - MAXIMUM ROUND TRIP DELAY : 1.2s (SATELLITE HOPS)
  - UP TO 10Hz OF PHASE ROLL ON FAR END ECHO
  - ITU-T V.22BIS, V.22 (2400, 1200bps)
  - V.32BIS/V.32/V.22BIS/V.22AUTOMODE
  - ITU- V.23, V.21, BELL 103 FULL-DUPLEX
  - -10 TO -25dBm PROGRAMMABLE TRANSMIT POWER
  - -10 TO -45dBm RECEIVER DYNAMIC RANGE
  - HDLC AND UART FRAMING SUPPORT
  - TRAIN AND RETRAIN BASED ON QUALITY LINE SAMPLING
- DIGITAL ANSWERING MACHINE :
  - LOW BIT RATE SPEECH CODER (4800bps)
  - VARIABLE PLAYBACK SPEED (+50% to -50%)
  - ARAM COMPATIBILITY (ERROR CORRECTION)
  - ADPCM 32, 24, 16Kbps
  - LINE ECHO CANCELLATION
  - VOICE ACTIVITY DETECTOR
  - CONCURRENT DTMF AND TONE DETECTION
- HANDSET MODE :
  - Rx AND Tx AGC VERSUS LINE CURRENT FOR LINE LOSSES COMPENSATION COMPLY WITH MOST OF COUNTRY REGULATIONS
  - DYNAMIC LIMITER IN TRANSMIT PATH TO PREVENT DISTORTION
  - TWO WAY CONVERSATION RECORDING
- HANDS-FREE MODE :
  - FULL DUPLEX SPEAKERPHONE USING LMS ADAPTATIVE FILTERING INCLUDING LINE ECHO CANCELLATION AND ACOUSTIC ECHO CANCELLATION
  - Rx AND Tx AGC VERSUS LINE CURRENT FOR LINE LOSSES COMPENSATION COMPLY WITH MOST OF COUNTRY REGULATIONS
  - DYNAMIC LIMITER IN TRANSMIT PATH TO PREVENT DISTORTION
  - LOUDSPEAKER VOLUME CONTROL
  - TWO WAY CONVERSATION RECORDING
- EXTENDED MODES OF OPERATIONS :
  - PROGRAMMABLE RING DETECTION
  - 16 PROGRAMMABLE TONE DETECTORS
  - TONE AND DTMF GENERATORS
  - CALLER ID RECEPTION
  - DTMF DETECTION
  - WIDE DYNAMIC RANGE (>48dB)
- VERSATILE INTERFACES :
  - PARALLEL 128 x 8-BIT DUAL PORT RAM
  - GENERAL PURPOSE 16 I/O PORTS
  - 2 RELAY DRIVE OUTPUTS
  - FULL DIAGNOSTIC CAPABILITY
  - DUAL 8-BIT DAC FOR CONSTELLATION DISPLAY
- SINGLE 5V POWER SUPPLY :
  - TYPICAL ACTIVE POWER CONSUMPTION : 725mW
  - LOW POWER MODE < 30mW
- 80 PINS TQFP PACKAGE (14mm x 14mm)

DESCRIPTION

The ST75C540 chip is a fully featured voice/modem engine suited for high-end computer telephony products, providing high speed fax and modem, digital answering machine and hands-free functions.

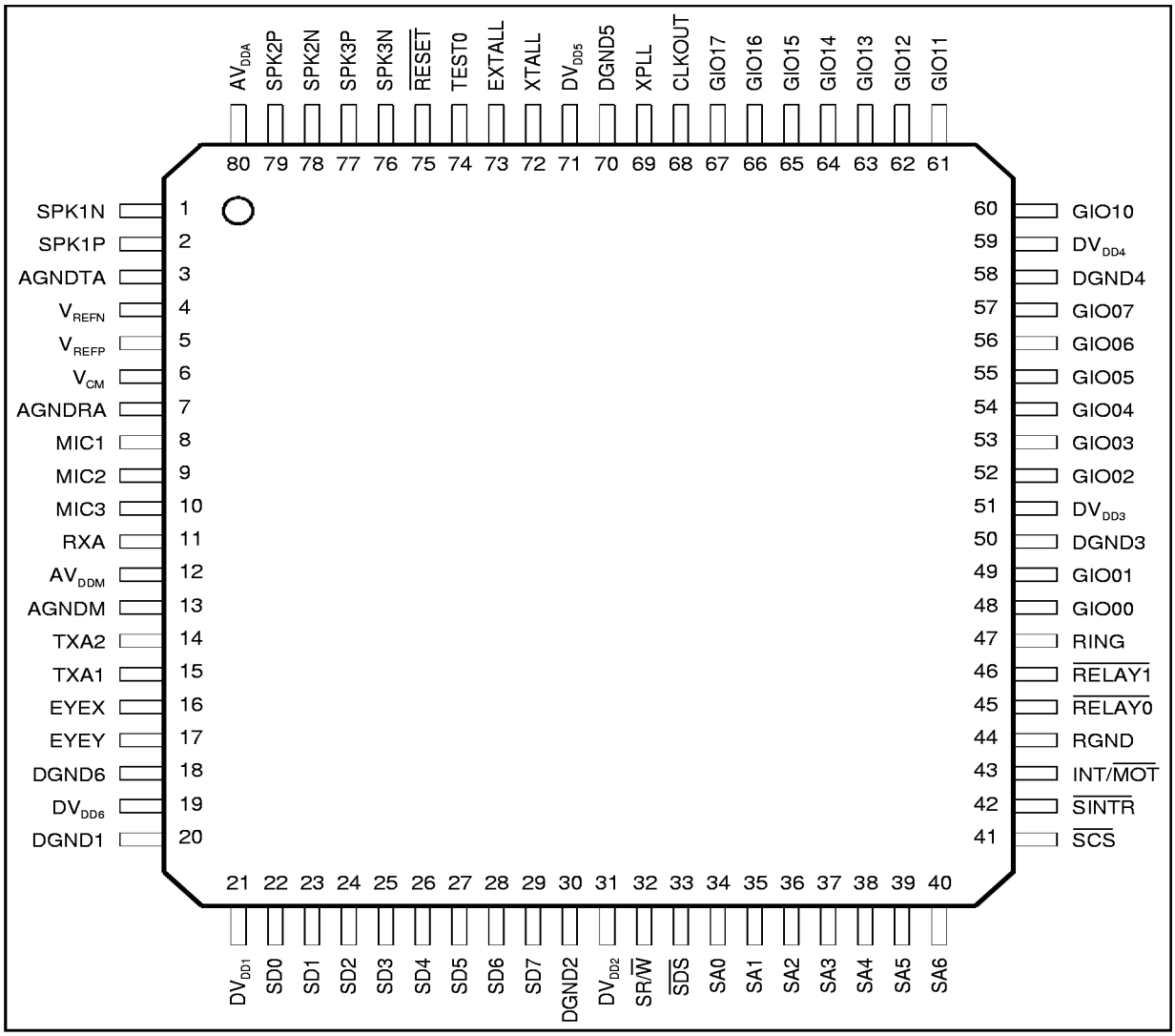


TQFP80
(Plastic Quad Flat Pack)
ORDER CODE : ST75C540 TQFP

CONTENTS

I - PIN DESCRIPTION

I.1 - Pin Connections



I - PIN DESCRIPTION (continued)

I.2 - Host Interface

The exchanges with the control processor proceed through a 128 x 8 DUAL port RAM shared between the ST75C540 and the Host. The signals associated with this interface are :

Pin Name	Type	Description
SD0..SD7	I/O	System Data Bus. 8-bit data bus used for asynchronous exchanges between the ST75C540 and the Host through the dual port RAM. High impedance when exchanges are not active.
SA0..SA6	I	System Address Bus. 7-bit address bus for dual port RAM, IO and interrupt registers.
$\overline{SDS}$ ($\overline{SRD}$)	I	System Data Strobe. In Motorola mode $\overline{SDS}$ initiates the exchange, active low. In Intel mode $\overline{SRD}$ initiates a read exchange, active low.
SR/$\overline{W}$ ($\overline{SWR}$)	I	System Read/Write. In Motorola mode SR/$\overline{W}$ defines the type of exchange read/write. In Intel mode $\overline{SWR}$ initiates a write exchange, active low.
$\overline{SCS}$	I	System Chip Select. Active low.
$\overline{SINTR}$	OD	System Interrupt Request. Open drain. Active low. This signal is asserted by the ST75C540 and negated by the host.
$\overline{RESET}$	I	Reset. Active low.
INT/$\overline{MOT}$	I	Select Intel or Motorola Interface.

I.3 - Analog Interface

Pin Name	Type	Description
TXA1	O	Transmit Analog Output 1
TXA2	O	Transmit Analog Output 2.
RXA	I	Receive Analog Input.
SPK1P	O	Speaker Output 1, (differential positive), must be connected through Amplifier to the loudspeaker.
SPK1N	O	Speaker Output 1, (differential negative).
SPK2P	O	Speaker Output 2, (differential positive), must be connected through Amplifier to the Handset loudspeaker.
SPK2N	O	Speaker Output 2, (differential negative).
SPK3P	O	Speaker Output 3, (differential positive).
SPK3N	O	Speaker Output 3, (differential negative).
MIC1	I	Microphone Input 1.
MIC2	I	Microphone Input 2.
MIC3	I	Microphone Input 3.
V_{CM}	I/O	Analog Common Voltage (nominal +2.5V). This input must be decoupled with respect to AGND.
V_{REFN}	I	Analog Negative Reference (nominal 1.25V). This input must be decoupled with respect to V_{CM}.
V_{REFP}	I	Analog Positive Reference (nominal 3.75V). This input must be decoupled with respect to V_{CM}.

I.4 - General Purpose IO and Relay

Pin Name	Type	Description
GIO[0,7]	I/O	General Purpose I/O Pins, can be independently selected as input or output.
GIO[10,17]	I/O	General Purpose I/O Pins, can be independently selected as input or output.
$\overline{RELAY0}$, RELAY1	OD	Relay Outputs, Open Drain, Active Low. Can sink -10mA to RGND.
$\overline{RING}$	I	Ring detect signal. Active low. If the ST75C540 is in low power mode, a low level will awake the chip. This input is a Schmidt's trigger.
RGND	PWR	Relay Digital Ground. To connect to GND.

I - PIN DESCRIPTION (continued)

I.5 - Miscellaneous

Pin Name	Type	Description
EYEX	O	Constellation X analog coordinate
EYEY	O	Constellation Y analog coordinate
XTAL	O	Internal Oscillator Output. Left open if not used.
EXTAL	I	Internal Oscillator Input, or External Clock Input.
XPLL	I	Reserved for future use, must be connected to digital ground.
CLKOUT	O	Output Clock, EXTAL/2 (not available in low power mode).
TEST0	I	Test pin for normal operation, must be connected to digital ground.

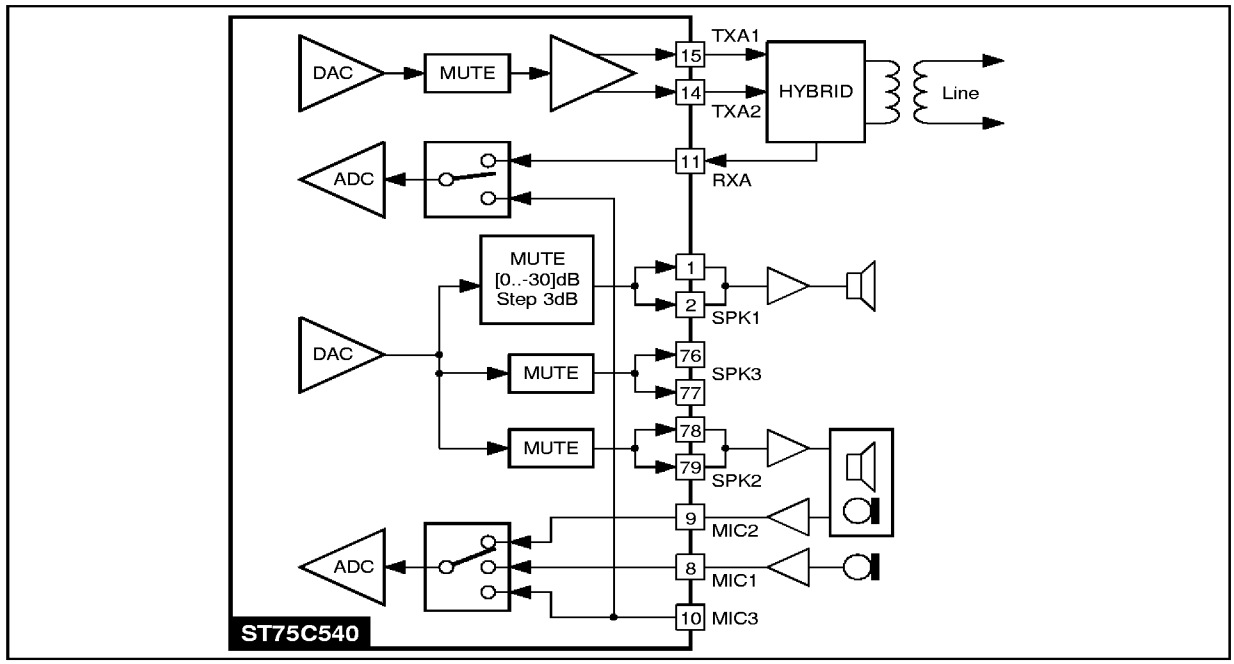
Note : The nominal frequency of the crystal oscillator is 44.2368MHz with a precision better than ± 100ppm.

I.6 - Power Supply

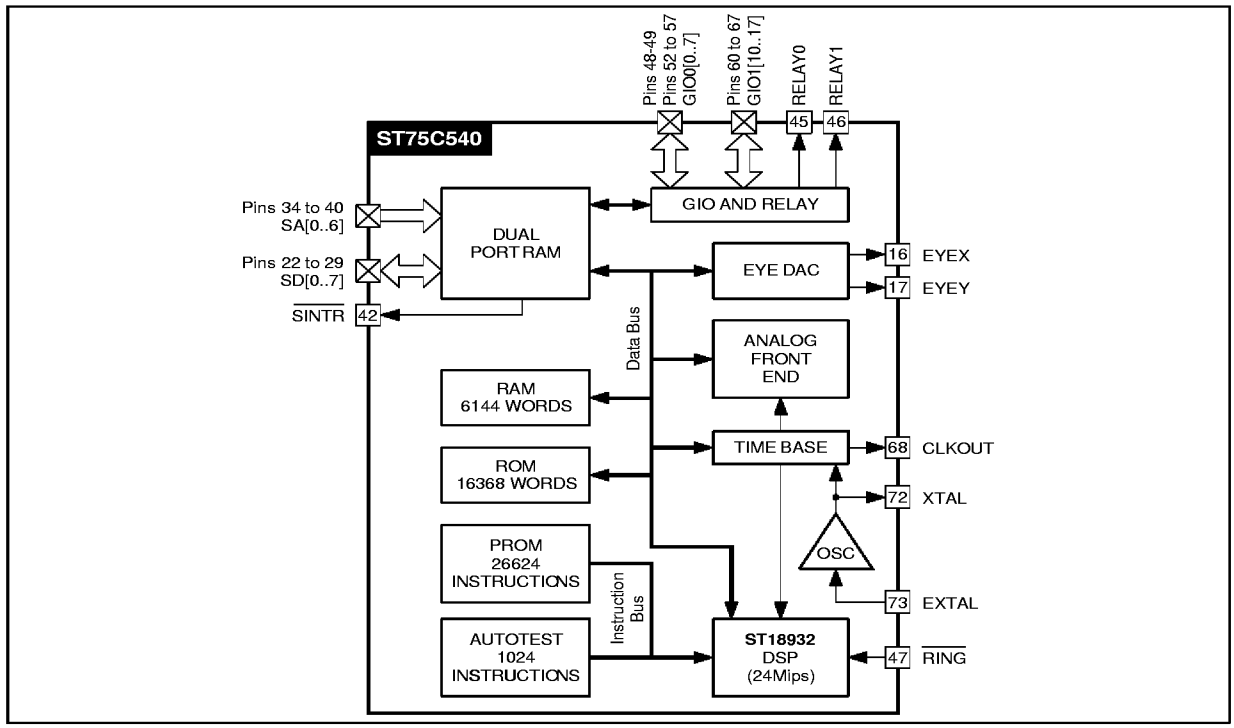
Symbol	Nber	Parameter
DV_{DD}	6	Digital +5V.
DGND	6	Digital Ground.
AV_{DD}	2	Analog +5V.
AGND	3	Analog Ground.

II - BLOCK DIAGRAMS

II.1 - Analog Interface



II.2 - Internal Block Diagram



III - ELECTRICAL SPECIFICATIONS

III.1 - Maximum Ratings (AGND = DGND = RGND = 0V, all voltages with respect to 0V)

Symbol	Parameter	Value	Unit
AV_{DD}	Analog Power Supply	-0.3, 6.0	V
DV_{DD}	Digital Power Supply	-0.3, 6.0	V
I_I	Input Current per Pin (except supply pins and $\overline{RELAY0}$ and $\overline{RELAY1}$)	-10, +10	mA
I_O	Output Current per Pin (except supply pins and $\overline{RELAY0}$ and $\overline{RELAY1}$)	-20, +20	mA
I_{O2}	Output Current per Pin $\overline{RELAY0}$ or $\overline{RELAY1}$ (respect to RGND)	-40, 0	mA
V_{IA}	Analog Input Voltage	-0.3, AV_{DD} + 0.3	V
V_{ID}	Digital Input Voltage	-0.3, DV_{DD} + 0.3	V
V_{IDGPIO}	Digital Input Voltage at GPIO	5.25	V
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	- 40, +125	°C
P_{tot}	Maximum Power Dissipation	1500	mW

Warning : Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranted at these extremes.

III.2 - Recommended Operating Conditions

(AGND = DGND = RGND = 0V, all voltages with respect to 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current		145	165	mA
P_{DLP}	Low Power			30	mW
P_D	Power		725	866	mW
V_{CM}	Common Mode Voltage Output (refer to $AV_{DD}/2$)	-5		+5	%
I_{CM}	Common Mode Current (see Note 1)		100		µA

Note 1 : DC current only. If dynamic load exists, the V_{CM} output must be buffered or the performances of ADCs and DACs will be degraded.

III - ELECTRICAL SPECIFICATIONS (continued)

III.3 - Digital Interface

(AV_{DD} = DV_{DD} = 5V, AGND = DGND = RGND = 0V) except XTAL, EXTAL, $\overline{RING}$.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage	2.2			V
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{OH}	High Level Output Voltage (I_{load} = -2mA, I_{load} = -4mA for SD[7..0])	2.4			V
V_{OL}	Low Level Output Voltage (I_{load} = 2mA, I_{load} = 4mA for SD[7..0])			0.4	V
I_{LEAK}	Input Leakage Current	-10		10	µA
I_{OL}	Low Level Output Current (0 < V_{OL} < $V_{OLMax.}$) (except $\overline{RELAY0}$ and $\overline{RELAY1}$, and $\overline{SINTR}$).	-2			mA
I_{OH}	High Level Output Current (0 < V_{OL} < $V_{OLMax.}$) (except $\overline{RELAY0}$ and $\overline{RELAY1}$, and $\overline{SINTR}$).			2	mA
I_{OZ}	GIO Three State Input Leakage Current (GND < V_O < V_{DD})	-50	0	50	µA
I_{OZ}	SD Three State Input Leakage Current (GND < V_O < V_{DD})	-50	0	50	µA
$I_{OLRELAY}$	Low Level Output Current $\overline{RELAY0}$ or $\overline{RELAY1}$ (V_{OL} = 0.8V)	-10		0	mA

CRYSTAL OSCILLATOR

V_{IH}	High Level Input Voltage	3.5			V
V_{IL}	Low Level Input Voltage			1.5	V
I_H	High Level Input Current	-20			µA
I_L	Low Level Input Current			20	µA

$\overline{RING}$: this input have hysteresis

V_{IH}	High Level Input Voltage		2.4	2.8	V
V_{IL}	Low Level Input Voltage	1	1.2		V
I_H	High Level Input Current	-20			µA
I_L	Low Level Input Current			20	µA

III - ELECTRICAL SPECIFICATIONS (continued)

III.4 - Modem Analog Interface

$AV_{DD} = DV_{DD} = 5V$, $T_{amb} = 25^{o}C$
Measurement bandwidth is flat from 100Hz to 4800Hz ;Load impedance 10kΩ, 20pF
For differential output (TxA1/TxA2) : 0dBr = $1.77V_{RMS}$ 1kHz sinwave (equivalent to $5V_{PP}$).
For single input (RxA) : 0dBr = $886mV_{RMS}$ 1kHz sinwave (equivalent to $2.5V_{PP}$).

Symbol	Pin Name	Parameter	Min.	Typ.	Max.	Unit
RXrin	RXA	Input Impedance	100			kΩ
RXmac		Maximum AC Input Voltage = 0dBr			2.5	V_{PP}
RXdc		DC Reference Voltage		2.5		V
RXsndr		Signal to (Noise + Distortion), at -6dBr	75			dB
RXin		Idle Noise			-81	dBr
RXov		DC Offset Voltage (Input = V_{CM})	-50		50	mV
TXAdrl	TXA1/TXA2	Minimum Differential Load	10			kΩ
TXAcl		Maximum Differential Load			20	pF
TXArout		Output Impedance			50	Ω
TXAmac		Maximum AC Differential Output = 0dBr			5	V_{PP}
TXAdc		DC Reference Voltage		2.5		V
TXAov		DC Offset Voltage	-200		200	mV
TXAsndr		Signal to (Noise + Distortion), at -6dBr	79			dB
TXAin		Idle Noise			-85	dBr

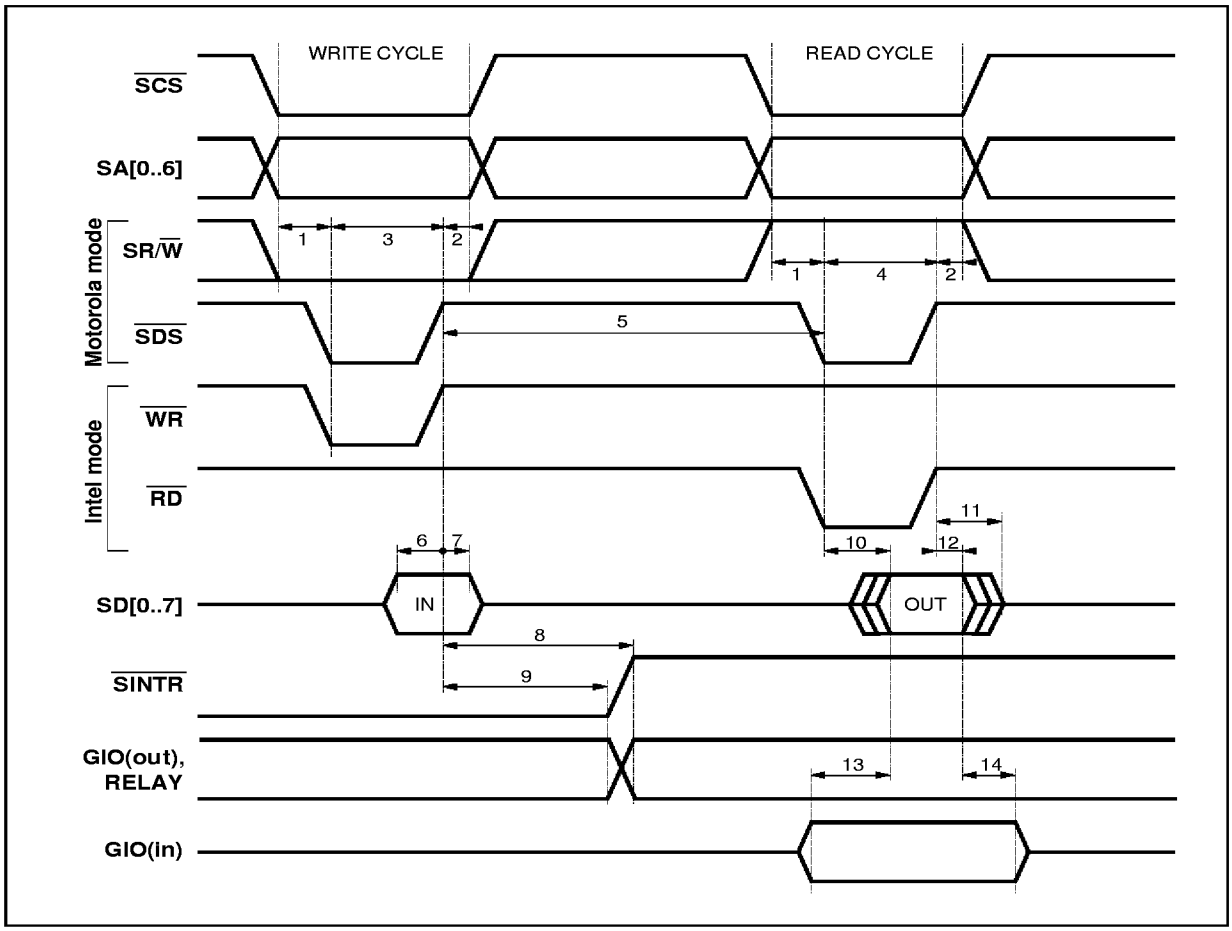
III.5 - Audio Analog Interface

$AV_{DD} = DV_{DD} = 5V$, $T_{amb} = 25^{o}C$
Measurement bandwidth is flat from 100Hz to 4800Hz ;Load impedance 10kΩ, 20pF
For differential output (SPK1N/SPK1P, SPK2N/SPK2P, SPK3N/SPK3P) : 0dBr = $1.77V_{RMS}$ 1kHz sinwave (equivalent to $5V_{PP}$).
For single input (MIC1, MIC2, MIC3) : 0dBr = $886mV_{RMS}$ 1kHz sinwave (equivalent to $2.5V_{PP}$).

Symbol	Pin Name	Parameter	Min.	Typ.	Max.	Unit
RArin	MIC1, MIC2, MIC3	Input Impedance	100			kΩ
RAmac		Maximum AC Input Voltage = 0dBr			2.5	V_{PP}
RAdc		DC Reference Voltage		2.5		V
RAdis		Distortion at -6dBr			2	%
RAin		Idle Noise			-81	dBr
RAov		DC Offset Voltage (Input = V_{CM})	-50		50	mV
TAdrl	SPK1N/SPK1P, SPK2N/SPK2P, SPK3N/SPK3P	Minimum Differential Load	10			kΩ
TArout		Output Impedance			50	Ω
TAmac		Maximum AC Differential Output = 0dBr			5	V_{PP}
TAdc		DC Reference Voltage		2.5		V
TAov		DC Offset Voltage	-200		200	mV
TAdis		Distortion at -6dBr			1	%
TAin		Idle Noise			-81	dBr

III - ELECTRICAL SPECIFICATIONS (continued)

III.6 - AC Electrical Characteristics



Number	Description	Min.	Typ.	Max.	Unit
1	Address and Control Set-up Time	5			ns
2	Address and Control Hold Time			20	ns
3	Write Enable Low State	45			ns
4	Read Enable Low State	45			ns
5	Access Inhibition High State	70			ns
6	Data Set-up Time	10			ns
7	Data Hold Time	5			ns
8	GIO Output, Relay, $\overline{\text{SINTR}}$ Clear Delay			50	ns
9	GIO Output Hold Time	0			ns
10	Read Data Access Time			35	ns
11	Data Valid to Tristate Time			15	ns
12	Data Hold Time	5			ns
13	GIO Input Delay Time			40	ns
14	GIO Input Hold Time	0			ns

IV - FUNCTIONAL DESCRIPTION

IV.1 - System Architecture

The chip allows the design of a complete FAX, Data Modem, Hands-Free Telephone and Answering Machine system. A versatile dual port RAM allows an easy interface with most micro-controllers.

IV.2 - Modes of Operation

Refer to Appendix A for Block Diagrams.

IV.3 - Operations

IV.3.1 - Modem Transmitter Description

The signal pulses are shaped in a dedicated filter further combined with a compromise transmit equalizer suited for transmission over strongly distorted lines. 3 different compromise equalizers are available and can be selected by software.

IV.3.2 - Modem Receiver Description

The receiver section handles complex signals and uses a fractionally spaced complex equalizer. It is able to cope with distant modem timing drifts up to 10^{-4} as specified in the ITU-T recommendations. It also compensates for frequency drift up to 10Hz and for phase jitter at multiple and simultaneous frequencies.

IV.3.3 - Tone Generator Description

Four tones can be simultaneously generated by the ST75C540. These tones are determined by their frequencies and by the output amplitude level. A set of specific commands are also available for DTMF generation. Any of the 4 tone generators can be output independently either on the Audio DAC or the line DAC.

IV.3.4 - Tone Detector Description

During TONE (respectively TONECID) Mode sixteen (respectively eight) tones can be simultaneously detected by the ST75C540. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR. Detection thresholds are programmable from -51dBm up to -6dBm. These primary detectors can detect tone up to 3.3kHz (sampling rate 7.2kHz in all modes). They also have a programmable internal wiring feature (see Chapter VIII).

In all modes, except Handset (HANDSET) and Full Duplex V.32bis/V.32/V.22bis/V.22 (Modem) modes, 4 additional tone detectors (each of them being a 4th order programmable IIR) are concurrently running. In Handset mode only 2 additional tone detectors are available. Detection thresholds are programmable from -51dBm up to -6dBm. This secondary programmable detector can detect tones up to 1.8kHz by default set-up with a sampling rate at 4.8kHz. But this 4 additional tone detectors can also detect tones up to 3.3kHz with a sampling rate at 9.6kHz. In order to avoid wrong detectgion, relative detectgion is also provided.

IV.3.5 - V.21 Channel 2 Flag Detector Description

In all the Receive FAX Modes, including V.21 Channel 2 Mode, the ST75C540 processes a V.21 Flag "7E" detector, either in the idle state, the train sequence or the data mode. The detection time is 3 consecutive flags to detect and 1 byte to loose the detection.

IV.3.6 - HDLC Description

In all FAX Modes (MODEM), including V.21 Channel 2 Mode, and also Full Duplex V.32bis/V.32/V.22bis/V.22 (Modem) modes, a HDLC framing and deframing is supported by the ST75C540. The number of transmitted flags can be programmed.

IV.3.7 - UART Description

In Full Duplex V.32bis/V.32/V.22bis/V.22 Modem Modes and TONECID V.23 receive mode, a parallel UART is performed by the ST75C540. This UART manage the Break signal either at the transmit and the receive bit stream. The Data format supported are 7 and 8 bit of Data; even, odd or no Parity, 1 or 2 stop bits.

IV.3.8 - DTMF Detector Description

A DTMF Detector is included in the ST75C540, it allows detection of valid DTMF Digits. A valid DTMF Digit is defined as a dual tone with a total power higher than -43dBm, a duration higher than 40ms and a differential amplitude within ±8dB. This DTMF Detector is enabled in all modes except in Fax Modem, Data Modem and Handset modes. It is also enabled in V.21 Channel 2 Receive Mode. The DTMF thresholds and duration can be changed from they default value by overwriting DSP's RAM locations. In the default setup, this detector is compliant with the NET4 standard. The frequency deviation can be changed by overwriting the default DTMF's filters coefficients.

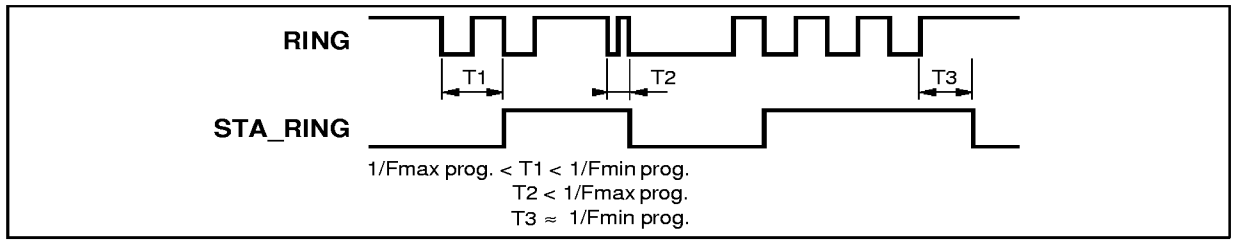
IV.3.9 - Ring Detector

This detector detects RING signal from 15Hz to 68Hz, it can be programmed to expand the minimum and maximum detection frequency up to 12Hz (for min) and 144Hz (for max). The detection time is equal to one period of the ring signal, and the loose time to the minimum between one period of the ring signal and the inverse of the minimum frequency.

The associated STA_RING status is as Figure 1.

IV - FUNCTIONAL DESCRIPTION (continued)

Figure 1



IV.3.10 - VOCODER Description

The Vocoder mode allows the implementation of an answering machine function. In the CODER mode the received samples from one of the two analog inputs, Line or Audio, are compressed by the ST75C540 and written into the dual port RAM Vocoder Buffer (VOCxxx). At the same time the ST75C540 is looking for an incoming DTMF tone and 4 different programmable tones.

In the DECODER mode the compressed samples are read from the dual port RAM, decompressed and transmitted to one of the two analog output, Line or Micx. The ST75C540 synthesises an estimation of its echo and subtracts it from the received signal. At the same time the ST75C540 is looking for an incoming DTMF tone and 4 different tones.

Two algorithms of voice coding are implemented :

- Low bit rate speech coder (4800bps or 5300bps with forward error correction).
- ADPCM (ST proprietary algorithm) at 32, 24 and 16Kbps.

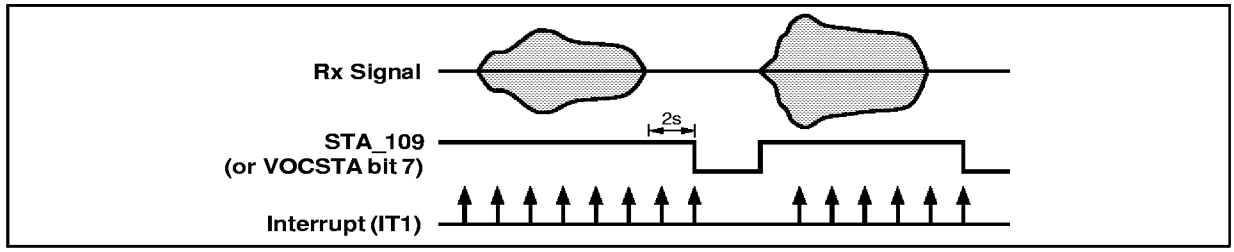
If the low bit rate coder algorithm is selected the ST75C540 has the capability to slow down or speed up the DECODER flow up to ±50%. This function allows a quick message listening if speed up is used, or at the opposite if slow down is used, an enhancement of the voice intelligibility.

IV.3.11 - Voice Activity Detector (VAD)

In CODER Mode, for both of the Voice Coding algorithms, a Voice Activity Detector is implemented while coding by the ST75C540. The STA_109 bit and STA_109F bit reflect the state of the VAD. After the CONF command the VAD is on (assume voice). The default time-out to detect silence is 2 seconds and the set-up time to detect the voice is 15ms. This VAD information is also copied into the Receive Buffer Status Word MSB (VOCSTA bit7). This detector is fully programmable in level sensitivity (down to -60dBm), hysteresis, and various criteria.

An optional silence suppressor is implemented in the Coder section to suppress long silence in the incoming message. When enabled (CONF_SUPSIL equal 1) if a long silence is detected (STA_109 equal 0) the ST75C540 stops generating Buffer Interrupts. After that if a voice is again detected the ST75C540 will resume the Buffer Interrupt mechanism.

Figure 2



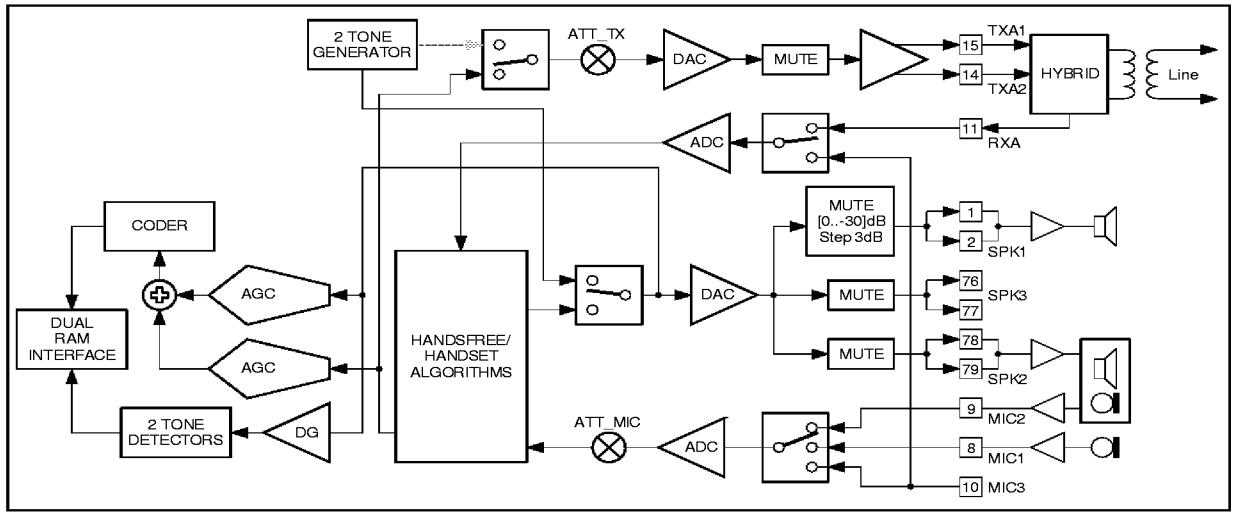
IV - FUNCTIONAL DESCRIPTION (continued)

IV.3.12 - Telephony Functions

ST75C540 telephony software provides both handset and handsfree modes. ST75C540 is connected to the phone line through a D.A.A., handset and loudspeaker are connected to ST75C540 through amplifiers.

Though the D.A.A. has to comply with modem/fax regulations in most of the applications, the microphone and the earphone amplifier gains will be adjusted in compliance with the telephony regulations. The software implemented in ST75C540 allows functions such as softclipping, AGC in both modes, and full duplex mode in handsfree (see figure 3).

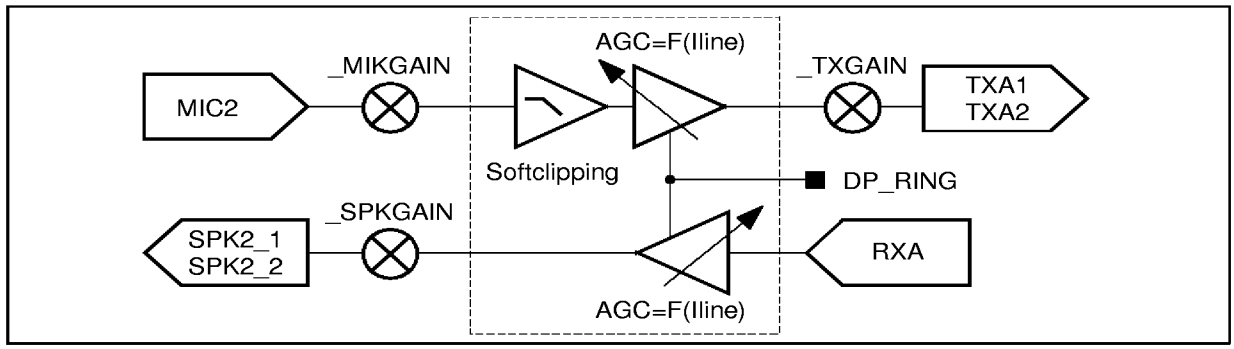
Figure 3 : Handset/Handsfree Mode Operation



IV.3.12.1 - Handset Mode

In handset mode, all the attenuations (_SPKGAIN, _TXGAIN, _MIKGAIN) are from 0db to -inf (32768 steps). AGC and softclipping functions can be enabled and disabled by software (see figure 4).

Figure 4 : Handset Mode



IV - FUNCTIONAL DESCRIPTION (continued)

Tx Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Gtx	Transmit Gain	_MIKGAIN=7FFF,_TXGAIN=7FFF, AGC disabled V_{MIC2} = -21dBV V_{MIC2} = -9dBV		 18 8		 dB dB
Ntx	Transmit noise	2kΩ between MIC2 and GND		-73		dBmp
Mmic	Microphone mute	V_{MIC2} = -21dBV		60		dB
VLpeak	Transmit softclipping level on TXA1-TXA2	_MIKGAIN=7FFF,_TXGAIN=7FFF, AGC disabled see Figure 3, V_{MIC2} = -9dBV		2.5		Vpp
Dtx	Transmit distortion	_MIKGAIN=7FFF,_TXGAIN=7FFF, AGC disabled see Figure 3, V_{MIC2} = -9dBV			2	%

Rx Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Grx	Receive Gain	_SPKGAIN=7FFF, AGC disabled, V_{RXA} = -16 dBV		6		dB
Nrx	Receive noise			-79		dBmp
Mrx	Mute	V_{RXA} = dBV		60		dB
Dtx	Receive distortion (SPK2 output)	__SPKGAIN=7FFF, AGC Disabled, V_{RXA} = -16dBV			2	%

AGC

The line current information is coming from the D.A.A. on DP_RING pin (frequencycoded information using by example a TS555 general purpose timer). The AGC has a 6dB depth . The attenuation table can be loaded to comply with each country regulation. The default table has the following values. The value of the AGC gain is applied to both Tx and Rx path (see Table 1).

The address of the table is given in the register @_TABLE.

The table length is 53. The AGC is enabled using CONF or MODC command (see paragraph "VI - COMMAND SET DESCRIPTION".

Once the AGC is running, it is possible to freeze the AGC gain with the register AGC_FRZ.

Softclipping

The softclipping introduces a 12dB gain and has a 18dB depth.

The softclipping value is half digital range (4000 Hex) (see Figure 5).

Figure 5 : Softclipping Static Gain Tx Softclipping and Distortion

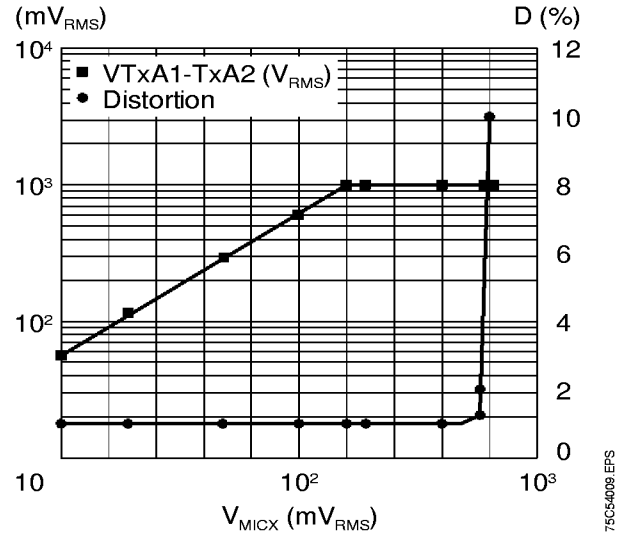


Table 1 : AGC Gain versus Period Information

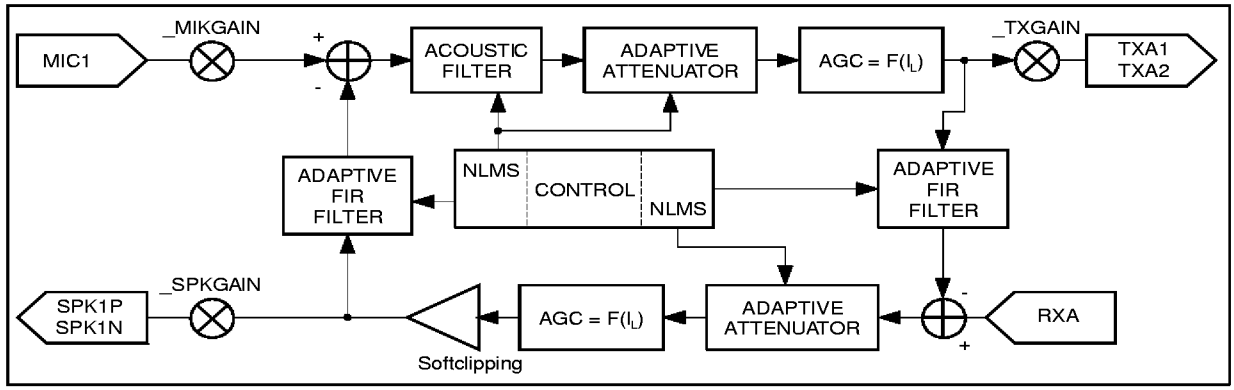
Period (ms)	<9	10	10.8	11.6	14.5	13.3	14.1	15.5	16.6	17.5	18.3	19.1	20	>20
Table Index	<13	13	14	15	16	17	18	19	20	21	22	23	24	>24
Gain (dB)	0	0.7	1.5	2.2	3	3.4	4	4.5	4.8	5.1	5.4	5.6	5.8	6

IV - FUNCTIONAL DESCRIPTION (continued)

IV.3.12.2 - Handsfree Mode

The handsfree uses a mic1 and a spk1 as microphone and loudspeaker interface (see Figure 6).

Figure 6 : Handsfree Mode : Full Duplex



Tx Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Gtx	Transmit Gain	_MIKGAIN=7FFF,_TXGAIN=7FFF ,AGC disabled, V_{MIC1} = -21dBV		24		dB
Ntx	Transmit noise	2kΩ between MIC1 and GND		-70		dBmp
Mmic	Microphone mute	V_{MIC1} = - dBV		60		dB
Dtx	Transmit distortion	_MIKGAIN=7FFF,_TXGAIN=7FFF ,AGC disabled, V_{MIC1} = -9dBV			2	%

Rx Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Grx	Receive Gain	_SPKGAIN=7FFF, AGC disabled, V_{RXA} = -33dBV		24		dB
Mrx	Mute			60		dB
Dtx	Receive distortion (SPK1 output)	__SPKGAIN=7FFF, AGC disabled, V_{RXA} = -33dBV			2	%

AGC

The AGC has the same behavior as in Handset mode. Furthermore, the maximum gain added by AGC can be fixed by using the RX_GAINMAX and TX_GAINMAX registers.

Softclipping

See Figure 7.

System Stability

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Loop attenuation in Rx Rxa to TXA1-TXA2	Speaker gain is 12dB, Mike gain is 14dB	20			dB
Loop attenuation in Tx MICx to SPK1P-SPK1N	Analogique sidetone not used (see DAA schematics)	20			dB

It is possible to add some gain switching in the Tx and Rx path (to reduce the gain of the loop) by using the GAIN_RCV and GAIN_XMT registers.

IV - FUNCTIONAL DESCRIPTION (continued)

Figure 7 : SPK1 Distortion versus RxA

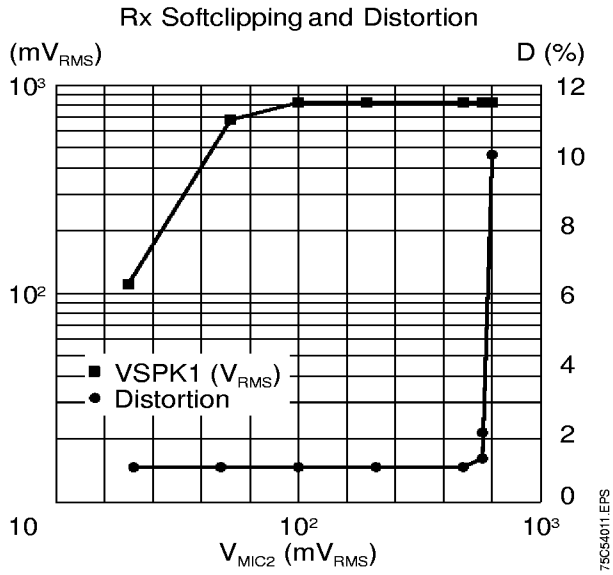
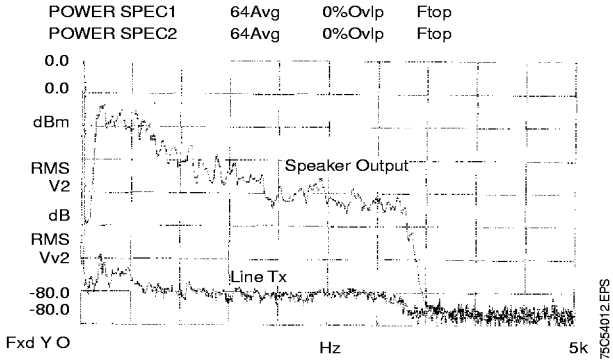


Figure 8 : Speaker and Line Tx Power Spectrums



Note : Acoustic echo from speaker to microphone input with no local speech. Receiving speech on line input.

IV.3.13 - Low Power Mode

Sleep state can be attained by a SLEEP command. When in sleep mode, the dual port RAM is unavailable and the clocks are disabled.

When entering the low power mode, the ST75C540 stops its oscillator, all the peripherals of the DSP core are stopped in order to reduce the power consumption. The dual port RAM is made inaccessible.

The ST75C540 can be awakened by a hardware reset, a RING signal or a dummy write at any location in the dual port RAM.

There is a maximum time of 20ms to restart the oscillator after waking up and an additional 5ms after the interrupt to be able to accept any command coming from the host.

IV.3.14 - Reset

After a hardware reset, or an INIT command, the ST75C540 clears all its internal memories, clears the whole dual port RAM and starts to initialize the delta sigma analog converters. As soon as these initializations are completed, the ST75C540 generates an interrupt IT6 (command acknoledge) and is programmed to send and receive tones, the sample clock are programmed to 9600Hz. The total duration of the reset sequence is about 5ms. After that time the ST75C540 is ready to execute commands sent by the host micro-controller. The duration of the reset signal should be greater than 700ns.

IV.4 - Modem Interface

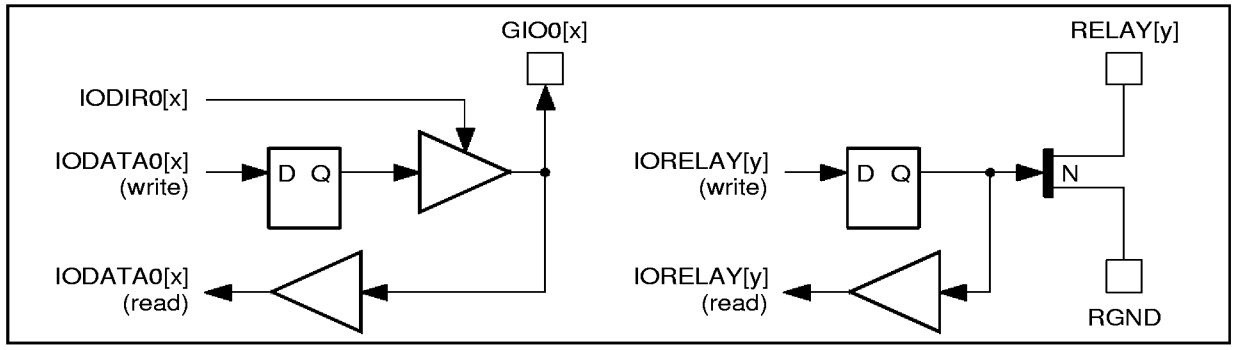
IV.4.1 - Analog Interface

Refer to Block Diagram on page 7.

IV.4.2 - General I/O and Relay Interface

16 pins are dedicated to the general I/O port. Two are dedicated to Relay driver. The equivalent schematic is as follows : see Figure 9.

Figure 9



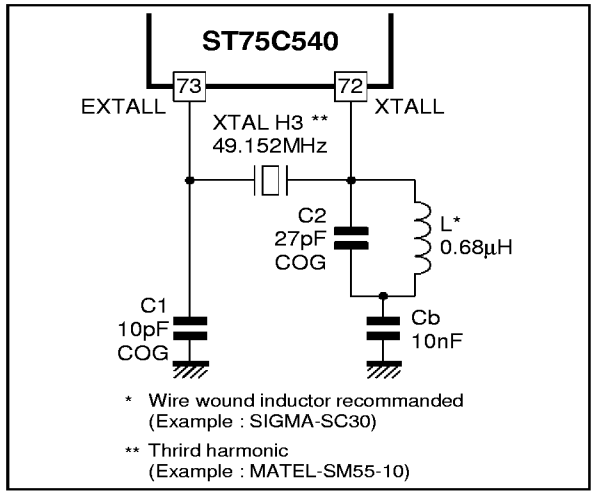
IV - FUNCTIONAL DESCRIPTION (continued)

IV.4.3 - Crystal

The crystal frequency must be 49.152MHz with an accuracy better that ±100 ppm. When using a third harmonic crystal the schematic must be as follow : see Figure 10.

The crystal features are :
- third harmonic (49.152MHz),
- parallel, load capacitance = 10pF,
- ± 100ppm from 0°C to 70°C,
- R_S < 50Ω,
- ATcut (example : SM55-10 MATEL).

Figure 10



IV.4.4 - Typical Application Schematic

The Figure 11 is a block diagram designed to allow transmission of fax signals up to +0dBm and sine wave up to +6dBm on the telephone line. It allows reception of fax signals up to 0dBm and sine waves up to +6dBm. Figure 12 is a block diagram designed to allow transmission of Modem signal up to -10dBm and reception up to -10dBm. The OPAmps are +12/0V powered. With this application schematic the out of band transmit spectrum (from 4kHz to 50kHz) is below -72dBm.

Figures 13 and 14 are examples of application schematics which respects gain value (respectively for fax and voice application and for Modem application) and the minimum differential load on TxA1 and TxA2.

IV.4.5 - Host Interface

The host interface is seen by the micro as a 128x8 RAM, with additional registers accessible through an 8-bit address space. A selection Pin (INT/$\overline{MOT}$) allows to configure the host bus for either INTEL or MOTOROLA type control signals.

Figure 11

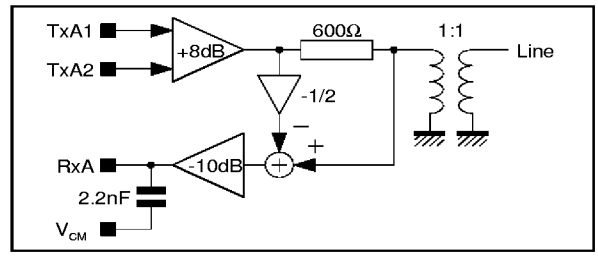
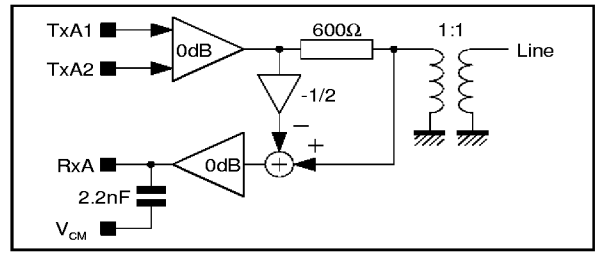


Figure 12



IV - FUNCTIONAL DESCRIPTION (continued)

Figure 13 : Fax Mode

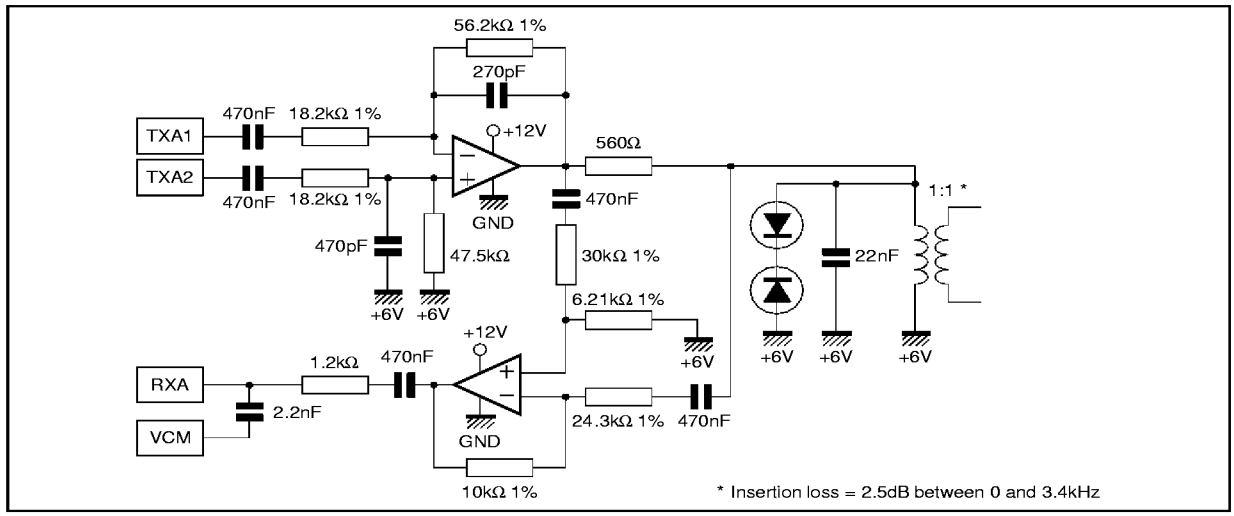
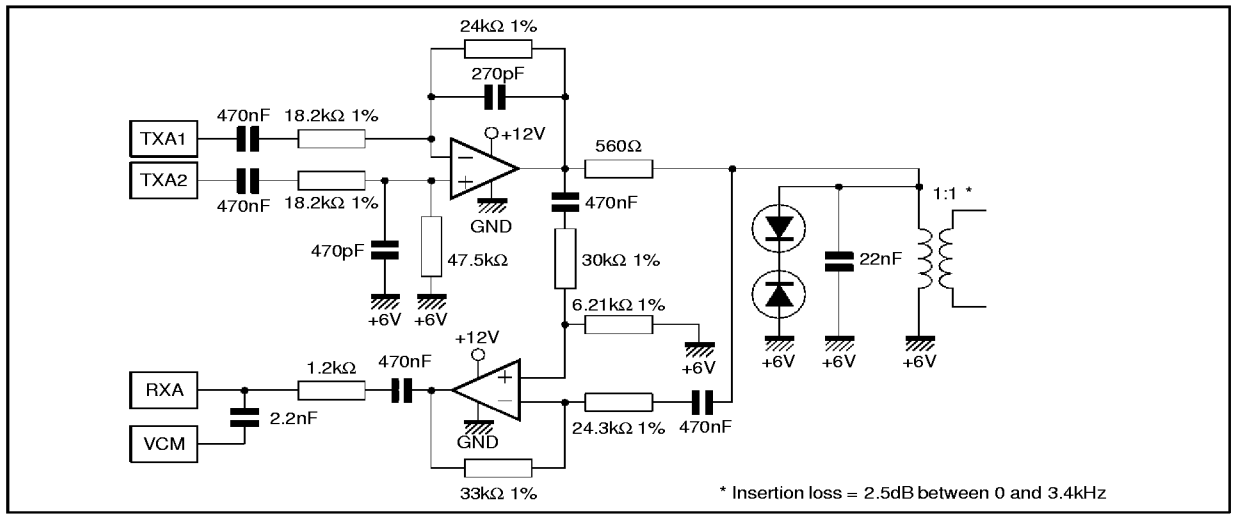


Figure 14 : Data Mode



V - USER INTERFACE

V.1 - Dual Port Ram Description

The dual port RAM is the standard interface between the host controller and the ST75C540, for either commands or data. This memory is addressed through a 7-bit address bus. The locations from $00 to $3F are RAM location, while locations from $40 to $60 are control registers dedicated to the interrupt handling and the general IO port and Relay output.

Several functional areas are defined in the dual port RAM mapping :
- the command area,
- the report area,
- the status area,
- the optional status area,
- the data buffer area,
- the interrupt control area,
- the general I/O and Relay Output area.

V.1.1 - Mapping

V.1.1.1 - Command Area

The command area is located from $00 to $04. Address $00 holds the command byte COMSYS, and the next four locations hold the parameters COMPAR[0..3]. The command parameters must be entered before the command word is issued. Once the command has been entered, the command byte is reset and an acknowledge report is issued. A new command should not be issued before the acknowledge counter COMACK is incremented.

V.1.1.2 - Report Area

The report area is located from address $05 to address $07. Location $05 holds the acknowledge counter COMACK. Each time a command is acknowledged, the report bytes COMREP[0..1] (if any) are written by the ST75C540 into locations $06 and $07, and the content of COMACK is incremented. This counter allows the ST75C540 to accurately monitor the command processing.

V.1.1.3 - Status Area

The status area is located from address $08 to $0B. The error status word SYSERR is located at address $08. This error status word is updated each time an error condition occurs. An optional interruption IT0 may additionally be triggered in the case of an error condition. Locations $09 and $0A hold the general status bytes STATUS[0..1]. The meaning of the bits depends on the mode of operation, and is described in Chapter VII. The third byte at address $0B holds the Quality Monitor byte STAQUA.

V.1.1.4 - Optional Status Area

The user can program (through the DOSR command) the four locations STAOPT[0..3] of the Optional Status Area ($0C to $0F) for the real time monitoring of four arbitrary memory locations.

V.1.1.5 - Data Buffer Area

The data area is made of four 8-byte buffers (see Paragraph V.1.3 “Host Interface Summary”). Two are dedicated to transmission and the two others to reception. Each of the four buffers is attached to a status byte. the meaning of the status byte depends on the selected format of transmission. Within each buffer, D0 represents the first bit in time.

V.1.1.6 - VOCODER Buffer Area (VOCODER Mode)

This area is made of a 18+2 byte buffer. This buffer contains the VOCODER frame. The first 18 bytes VOCDATA contain the coded frame and the other 2 bytes VOCCORR the Error corrections bit (only valid in low bit rate mode).
In the Receive Mode (CODER) the ST75C540 codes the received samples and writes the corresponding bytes in the buffer. If the low bit rate mode is selected, the ST75C540 computes the Error corrections 2 bytes and writes them in the buffer.
In the Transmit Mode (DECODER) the ST75C540 reads the 18 coded bytes decodes them and sends the signal to the analog output. In the low bit rate mode if the Error Correction is enabled, prior the decoding, the ST75C540 reads the 2 Error Correction Bytes and, if any, corrects the first 18 bytes.

A mechanism of flags to share the buffer access between the ST75C540 and the host controller is controlled by the VOCSTA byte :
- In CODER mode, when the ST75C540 has finished writing the VOCDATA and VOCCORR bytes, it writes $14 in VOCSTA and generate an Interrupt IT1. The host must read the Data buffer then clear the VOCSTA byte.
- In DECODER mode, the host must feed the VOCDATA and, optionaly, the VOCCORR bytes, then write $14 (if low bit rate) or $12 (if ADPCM) in VOCSTA. The ST75C540 will read the VOCDATA and VOCCORR bytes, clear the VOCSTA and generate an Interrupt IT1. A silence frame can be generated, in either low bit rate or ADPCM mode, by writing 00 in all the VOCDATA buffer, including the Error Correction Bytes VOCCORR.

V - USER INTERFACE (continued)

V.1.1.7 - Interrupt Control Area

The interrupt area, that start after the address $40 controls the behaviour of the Interrupts mechanism. Register ITSRCR defines the source of the interrupt, the register ITMASK allows independent enabling or disabling of any of the interrupt's source, registers ITREST0 to ITREST6 reset the corresponding interrupt source.
These registers are not affected by a INIT command, they are only reseted by a Hardware RESET signal.

V.1.1.8 - General IO and Relay Output Area

A set of 5 registers is directly accessible by the controller to program the General IO pins and Relay Outputs (see Paragraph V.1.3 "Host Interface Summary"). Two registers IODIR0 and IODIR1 define the type of the IO pin, either Input or Output (0 = input, 1 = output), and two registers IODATA0 and IODATA1 define the IO pin signals. The fifth register defines the Relay output signals. These registers are not affected by a INIT command, they are only reseted by a Hardware RESET signal. The general IO are setup as input after the power up or an hardware RESET. The relay output are open after power up or an hardware RESET.

V.1.2 - Interruptions

The ST75C540 can generate 7 interrupts for the controller. The interrupt handling is made with a set of registers located from $40 to $5F.
The interruptions generated by the ST75C540 come from several sources. Once the ST75C540 raises an interrupt, a signal ($\overline{SINTR}$) is sent to the controller. The controller has then to process the interrupt and clear it. The interrupt source can be examined in the interrupt source register ITSRCR located a $50. According to the ITSRCR bits, the interrupt source can be determined. Then writing a zero at one of the memory location $40 to $46 (Reset Interrupt Register ITRES[0..6]) will reset the corresponding interrupt (and thus acknowledge it). The source of the interrupt can be masked globally or individually using the Interrupt Mast register ITMASK located at $4F.

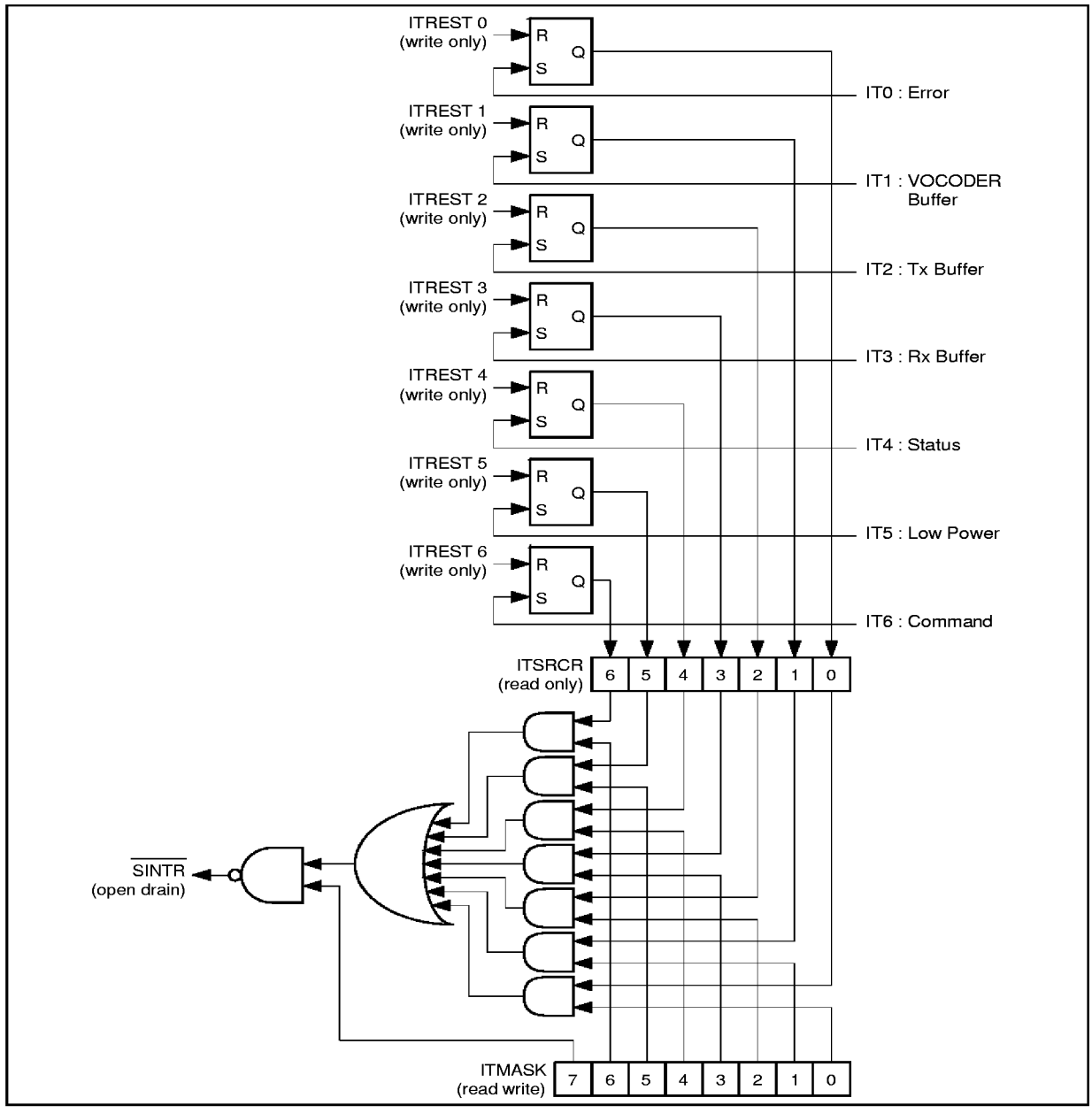
The interrupt sources are :

- **IT0 : Error**
  This signifies that an error has occurred and the error code is available in the error status byte SYSERR. This byte can be selectively cleared by the CSE command.
- **IT1 : VOCODER Buffer**
  Each time the ST75C540 have coded a frame (CODER Mode) or decoded a frame (DECODER Mode) this interrupt is generated.
- **IT2 : Tx Buffer**
  Each time the ST75C540 frees a data buffer, this interrupt is generated.
- **IT3 : Rx Buffer**
  Each time the ST75C540 has filled a data buffer, this interrupt is generated.
- **IT4 : Status Byte**
  This signifies that the status byte has changed and must be checked by the controller.
- **IT5 : Low Power Mode**
  The ST75C540 has been awakened from the low power mode by a low level on the RING pin or a dummy write issued by the host.
- **IT6 : Command Acknowledge**
  This signifies that the ST75C540 has read the last command entered by the host, incremented the command counter COMACK, and is ready for a new command.

Note : Interrupt registers are cleared after a Hardware RESET. These registers are not affected by a **INIT** Command.

V - USER INTERFACE (continued)

Figure 15 : Functional Schematic



V - USER INTERFACE (continued)

V.1.3 - Host Interface Summary

Address (hex)	Description	Size (Byte)	Mnemonic
COMMAND AREA			
$00	Command	1	COMSYS
$01-$04	Command Parameters	4	COMPAR[0..3]
REPORT AREA			
$05	Acknowledge Counter	1	COMACK
$06-$07	Report	2	COMREP[0..1]
STATUS AREA			
$08	Error Status	1	SYSERR
$09-$0A	General Status	2	STATUS[0..1]
$0B	Quality Monitor	1	STAQUA
$0C-$0F	Optional Report	3	STAOPT[0..3]
DATA BUFFER AREA (FAX Modes)			
$1C	Data Rx Buffer 0 Status	1	DTRBS0
$1D-$24	Data Rx Buffer 0	8	DTRBF0[0..7]
$25	Data Rx Buffer 1 Status	1	DTRBS1
$26-$2D	Data Rx Buffer 1	8	DTRBF1[0..7]
$2E	Data Tx Buffer 0 Status	1	DTTBS0
$2F-$36	Data Tx Buffer 0	8	DTTBF0[0..7]
$37	Data Tx Buffer 1 Status	1	DTTBS1
$38-$3F	Data Tx Buffer 1	8	DTTBF1[0..7]
VOCODER BUFFER AREA (Vocoder Mode)			
$1C	Vocoder Buffer Status	1	VOCSTA
$1D-$2E	Vocoder Buffer Data	18	VOCDATA
$2F-$30	Vocoder Buffer Corrector	2	VOCCORR
INTERRUPT AREA			
$40-$46	Reset Interrupt Register	7	ITREST[0..6]
$4F	Interrupt Mask Register	1	ITMASK
$50	Interrupt Source Register	1	ITSRCR
GENERAL IO AND RELAY			
$60	I/O Direction 0	1	IODIR0
$61	I/O Direction 1	1	IODIR1
$62	I/O Data 0	1	IODATA0
$63	I/O Data 1	1	IODATA1
$64	I/O Relay Register	1	IORELAY

Note : Registers which address is higher or equal to $40 are not affected by a INIT Command or a Low Power wake-up. They are reseted only by a Hardware RESET.

V - USER INTERFACE (continued)

V.2 - Command Set

The Command Set has the following attractive features :

- user friendly with easy to remember mnemonics,
- possibility of straightforward expansion with new commands to suit specific customer requirements,
- easy upgrade of existing software using previous modem based SGS-THOMSON products.

The command set has been designed to provide the necessary functional control on the ST75C540. Each command is classified according to its syntax and the presence/absence of parameters. In the case of a parametric command, parameters must first be written into the dual port RAM before the command is issued. Acknowledge and error report is issued for each command entered.

V.2.1 - Command Set Summary

V.2.1.1 - Operational Control Commands

INIT Initialize. Initialize the modem engine. Set all parameters to their default values and wait for commands of the control processor. Non parametric command.

IDT Identify. Return the product identification code. Non parametric command.

SLEEP Turn to low power mode, the ST75C540 enters the low power mode and stops its crystal oscillator to reduce power consumption. In this mode all the clocks are stopped and the dual RAM is unreachable.

HSHK Handshake. Begins the handshake sequence. The modem engine generates all the sequences defined in the ITU-T recommendations. A status report indicates to the control processor the state of the handshake. This command only applies to modes where a handshake sequence is defined. A CONF command must have been issued prior to the use of HSHK. Non parametric command.

STOP FAX Stop. Stop FAX Half-duplex transmitter. Non parametric command.

RTRA Retrain. Begin a retrain sequence in V.32bis/V.32 or V.22bis modes as described in the ITU-T recommendations.

SYNC FAX Synchronize. Start/Stop of FAX Half-duplex receiver. Parametric command.

CSE Clear Status Error. Selectively clears the Error status byte SYSERR. Parametric command.

SETGN Set Gain. This command sets the global gain factor, which is used for the transmit samples. Parametric command.

V.2.1.2 - Data Communication Commands

XMIT Transmit Data. Start/stop the transmission of data. After a XMIT command, the ST75C540 sends the data contained in its dual port RAM.

FORM Selects the Transmission Format. This command configures the data interface for both receiver and transmitter according to the selected data format. Parametric command (HDLC, UART or synchronous).

V.2.1.3 - Memory Handling Commands

MWI Memory Write Indirect

MWLO Memory Write Low Word

MW Memory Write. This command is used to write an arbitrary 16-bit value into the writable memory location currently specified by a parameter. Parametric command.

MRI Memory Read Indirect

MRLO Memory Read Low Word

MR Memory Read. This command allows the controller to read any of the ERAM or CROM (ST75C540 memory spaces) location without interrupting the processor. Parametric command.

CR Complex Read. This command allows the controller to read at the same time the real and imaginary part of a complex value stored in a double ERAM or CROM location. This feature is very interesting for eye pattern software control and for equalization monitoring. This command insures that the real and imaginary parts are sampled in the memory at the same time (integrity). Parametric command.

V - USER INTERFACE (continued)

V.2.1.4 - Configuration Control Commands

ASEL Select the Analog path option, like Microphone input, Speaker attenuation. Parametric command.

CONF Configure. This command configures the modem engine for data transmission and handshake procedures (if any) in any of the supported modes. The transmission parameters are set to their default values and can be modified with the MODC command. Parametric command.

MODC Modify Configuration. This command allows modification of some of the parameters which have been set up by the CONF command. It can also be used to alter the mode of operations (short train). Parametric command.

DOSR Define Optional Status Report. This command allows the modification of the optional status report located in the status area of the dual port RAM. One can thus select a particular parameter to be monitored during all modes of operation. Parametric command.

DSIT Define Status Interrupt. This command allows the programming of the status word bit that will generate an Interrupt to the controller. Parametric command.

V.2.1.5 - Tone Generation Commands

TONE Select Tone. Programs the tone generator(s) for the desired default tone(s). Additional mnemonics provide quick programming of DTMF tones or other currently used tones. Parametric command.

DEFT Define Tone. Programs the tone generator(s) for arbitrary tone synthesis. Parametric command.

TGEN Tone Generator Control. Enables or disables the tone generator(s). Parametric command.

IV.2.1.6 - Tone Detection Commands

TDRC Read Tone Detector Coefficient. Read one Tone Detector Coefficient. Parametric command.

TDWC Write Tone Detector Coefficient. Write one Tone Detector Coefficient. Parametric command.

TDRW Read Tone Detector Wiring. Read one Tone Detector Wiring connection. Parametric command.

TDWW Write Tone Detector Wiring. Write one Tone Detector Wiring connection. Parametric command.

TDZ Clear Tone Detector Cell. Clear internal variables of a Tone Detector Cell. Parametric command.

V.2.1.7 - Miscellaneous Commands

CALL Call a Subroutine. Call a subroutine with one Parameter. Parametric command.

JSR Call a Low Level Subroutine. Call an internal subroutine with one parameter. Parametric command.

V.3 - Command Set Short Form

CCI Command		
Mnemonic	**Value**	**Description**
XMIT	0x01	Transmit Data
SETGN	0x02	Set Transmit Gain
SLEEP	0x03	Power Down the ST75C540
HSHK	0x04	FAX Start Transmitter
RTRA	0x05	Retrain (V.32bis/V.32 and V.22bis)
INIT	0x06	Initialize (Software Reset)
CSE	0x08	Clear Error Status Word
FORM	0x09	Define Data Format
DOSR	0x0A	Define Optional Status Report
ASEL	0x0B	Select the Analog Path Options
TONE	0x0C	Generate Predefined Tones
TGEN	0x0D	Enable Tone Generator
DEFT	0x0E	Define Arbitrary Tone
MR	0x10	Memory Read
CR	0x11	Complex Read
MW	0x12	Memory Write
DSIT	0x13	Define Status Interrupt
IDT	0x14	Return Product Identification Code
JSR	0x18	Call a Low Level Routine
CALL	0x19	Call a Routine
TDRC	0x1A	Tone Detector Read Coefficient
TDRW	0x1B	Tone Detector Read Wiring
TDWC	0x1C	Tone Detector Write Coefficient
TDWW	0x1D	Tone Detector Write Wiring
TDZ	0x1E	Tone Detector Clear Cell
CONF	0x20	Configure
MODC	0x21	Modify Default Configuration
STOP	0x25	FAX Stop Transmitter
SYNC	0x26	FAX Synchronize Receiver
MRI	0x28	Memory Read Indirect
MRLO	0x29	Memory Read Low Word
MWI	0x2A	Memory Write Indirect
MWLO	0x2B	Memory Write Low Word

V - USER INTERFACE (continued)

V.4 - Status - Reports

V.4.1 - Status

The ST75C540 has a dedicated status reporting area located in its dual port RAM. This allow a continuous monitoring of the status variables without interrupting the ST75C540.

The first status byte gives the error status. Issuing of an error status can also be flagged by a maskable interrupt for the controller. The signification of the error codes are given in Chapter VII.

The second and third status bytes give the general status of the modem. These status include for example the ITU-T circuit status and other items described in Chapter VII "STATUS DESCRIPTION". These two status can generate, when a change occurs, an interrupt to the controller ; each bit of the two byte word can be masked independently.

The forth byte gives in real time a measure of the reception quality. This information may be used by the controller to monitor the quality of the received bits.

Four other locations are dedicated for custom status reporting. The controller can program the ST75C540 for a real time monitoring of any of its internal RAM location. High byte or low byte of any word can thus be monitored.

V.4.2 - Reports

The ST75C540 features an acknowledge and report facility. The acknowledge of a command is monitored by a counter COMACK located in the dual port RAM. Each time a command is read from the command area, the ST75C540 will increment this counter. For instance, when a MR (Memory Read) command is issued, the data is first written in the report area, and the counter is incremented afterwards. This way of processing insures data integrity and gives additional synchronization between the controller and the data pump.

V.5 - Data Exchanges

The ST75C540 accepts many kinds of data exchange : the default mode uses the synchronous parallel exchange. Other modes include HDLC framing support and UART. Detailed description of the Data Buffer Exchanges modes is available in the paragraph IX.

V.5.1 - Synchronous Parallel Mode

The data exchanges are made through the dual port RAM and are byte synchronous oriented. The double buffer facilities of the ST75C540 allow an efficient buffering of the data.

V.5.1.1 - Transmit

The controller must first fill at least the first buffer of data (Tx Buffer 0) with the bits to be transmitted. In order to perform this operation, the controller must first check the Tx Buffer 0 status word DTTBS0. If this buffer is empty, the controller fills the data buffer locations (up to 64 bits), and then writes in DTTBS0 the number of bytes contained in the buffer. The controller can then either proceed with the second buffer or initiate the transmission with a XMIT command.

The ST75C540 copies the contents of the data buffer and then clears the buffer status word in order to make it again available, then generates an IT2 interrupt. The number of bytes specified by the status word is then queued for transmission. The process goes on with the two buffers until an XMIT command stops the transmission. After the finishing XMIT command has been issued, the last buffers are emptied by the ST75C540.

Errors occur when both buffers are empty while the transmit bit queue is also empty. Error is signalled with an IT0 interruption to the controller.

V.5.1.2 - Receive

The controller should take care of releasing the Rx buffers before the Data Carrier Detect goes true. This is made by writing zero in the Rx Buffer Status 0 and 1. The ST75C540 then fills the first buffer, and once filled sets the status word with the number of bytes received and then generates an IT3 interrupt. It then takes control of the second buffer and operates the same way. The controller must check the status of the buffers and empty them. Once the data read, the controller must release the used buffer and wait for the next buffer to be filled.

Error occurs when both buffers are declared full, and incoming bits continue to arrive from the line. Error is signaled by an IT0 interrupt.

V.5.2 - HDLC Parallel Mode

This mode implements part of the High Level Data Link Control formats and procedures. It is well suited for error correcting protocols like ECM or FAX T4/T30 recommendations. It supports the flagging generation, 16-bit Frame Check Sequence, as well as the Zero insertion/deletion mechanism.

V.5.3 - UART Parallel Mode

This mode implement a 7 or 8 bit data format, it is well suited for Caller ID or Minitel applications.

VI - COMMAND SET DESCRIPTION

Commands are presented according to the following form :

COMMAND — Command Name Meaning — COMMAND

Opcode Hexadecimal digit

X	X	X	X	X	X	X	X

Synopsis Short description of the functions performed by the command.

Parameters

Field	Byte	Pos.	Value	Definition
Name	X	b..a	xx *	Explanation of the parameter Default value

Field — Name of the addressed bit field.
Byte — Index (or address in the dual port RAM) of the parameter byte (from 1 to 4).
Pos. — Bit field position inside the parameter byte. Can either be a single position (from 0 to 7, 0 being LSB) or a range.
Value — Possible values for the bit (resp. bit field). Range means all values are allowed. A star means a default value. Values are expressed either under the form of a bit string, or under hexadecimal format.

ASEL — ASEL

Opcode: 0B

0	0	0	0	1	0	1	1

Synopsis Select the analog path options. This command select the Attenuation/Mute of the outputs TXA1/TXA2 and SPK1/SPK2/SPK3. This command select also the source of the Mic signal MIC1/MIC2/MIC2 and the source of the Line Signal RXA/MIC3.

Parameters

Field	Byte	Pos.	Value	Definition
ASEL_ASPK1	1	7..4	0000* 0001 0010 ... 1010 1011 Other	Infinity attenuation 30dB attenuation 27dB attenuation ... 3dB attenuation 0dB attenuation Reserved
ASEL_MICSEL	2	1..0	00* 01 10 11	Select RX input as MIC1 Select RX input as MIC1 Select RX input as MIC2 Select RX input as MIC3
ASEL_LINESEL	2	2	0* 1	Select RxA as line input Select Mic3 as line input
ASEL_ESPK1	2	3	0* 1	SPK1 output muted SPK1 output normal
ASEL_ESPK2	2	4	0* 1	SPK2 output muted SPK2 output normal
ASEL_ESPK3	2	5	0* 1	SPK3 output muted SPK3 output normal
ASEL_MTXA	2	7	0* 1	TxA output normal TxA output muted

CALL — Call a Subroutine — CALL

Opcode: 19

0	0	0	1	1	0	0	1

Synopsis CALL allows to execute a part of the ST75C540 firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

This instruction can be used with SGS-THOMSON Microelectronics Application Laboratory Support for special applications development or debugging needs. Contact your local representative.

VI - COMMAND SET DESCRIPTION (continued)

CONF — Configure for Operations — CONF

Opcode : 20

0	0	1	0	0	0	0	0

Synopsis CONF allows the complete definition of the ST75C540 operation, including the mode of operation (Tone, FAX Transmit, Voice Transmit, Voice Receive, DTMF Receiver, ...) and the Modem or Vocoder Parameters (Standard, speed, ...). According with the 4 first bits of the CONF Parameter the ST75C540 is put into the following mode of operation.

CONF_ OPER	Mode	Detectors							
		Tone (2)	Tone (3)	DTMF	Ring	VAD	V.21 Flag	CPT (5)	Answ (6)
0000*	TONE	16	4	Yes	Yes	No	Yes	Yes	Yes
0001	TONECID(1)	6	4	Yes	Yes	No	Yes	Yes	No
0010	DECODER	0	4	Yes	Yes	No	No	No	No
1000	CODER	0	4	Yes	Yes	Yes	No	No	No
1001	ROOM-MONITOR	0	4	Yes	No	No	No	No	No
1100	HANDSET/HANDSFREE	0	2	No	No	No	No	No	No
1111	MODEM	0	4 (7)	Yes (4)	No	No	Yes	Yes (4)	No
Other	Reserved								

Notes :
1. This mode includes V.23/Bell202 FSK Demodulator and UART.
2. This primary Tone Detectors allows Detection of signal up to 3.3kHz. (Sampling Rate 7.2kHz).
3. This secondary Tone Detectors allows Detection of signal up to 1.8kHz (with Sampling Rate 4.8kHz) or up to 3.3kHz (with Sampling Rate 9.6kHz).
4. The DTMF detector and Call Progress Tone detector (CPT) are available only for V.21 Channel 2.
5. STA_CPT0, STA_CPT1 and STA_CPT10 in STATUS0.
6. STA_CCITT and STA_AT in STATUS1.
7. Not available in V.32bis/V.32.

Parameters When the CONF_OPER is set to F, selecting the Modem Mode of operation, the parameters have the following meaning :

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	1111	Select Modem Mode
CONF_ANAL	1	4	0 1	Normal mode Analog loop back (test mode only)
CONF_PSTN	1	5	0 1	PSTN (carrier detect set to -43/-48dBm) Leased line (carrier detect -33/-38dBm)
CONF_AO	1	6	0 1	Answer mode Originate mode
CONF_DTINIT (only in tone mode)	1	7	0 1	Global init of secondary tone detector Partial init of secondary tone detector (8)
CONF_MODE	2	5..0	0 1 2 3 4 5 6 7 8 9 A B C D Other	Automode (V.32bis/V.32/V.22bis/V.22) Bell 103 (full duplex) Bell 212A (full duplex) V.21 (full duplex) V.23 (full duplex) V.22 (full duplex) V.22bis (full duplex) V.27ter V.29 V.17 V.32 (full duplex) V.32bis (full duplex) V.33 (half duplex) V.21 channel 2 Reserved
CONF_TXEQ	2	7..6	0 1 2 3	No transmit equalizer Transmit equalizer #1 Transmit equalizer #2 Transmit equalizer #3 (V.17/V.33/V.29/V.27ter)
CONF_CAR	3	0	0 1	1800Hz carrier (V.17/V.33 only) 1700Hz carrier (V.17/V.33 only)
CONF_TCM	3	1	0 1	Treillis coding not allowed (V.32 only) Treillis coding allowed (V.32bis, V.32)
CONF_SP0	3	7..4	xxx1 xx1x x1xx 1xxx	1200bps allowed (V.22, V.22bis) 2400bps allowed (V.22bis, V.27) 4800bps allowed (V.32bis, V.32, V.27, V.29) 7200bps allowed (V.32bis, V.29, V.17)
CONF_SP1	4	2..0	xx1 x1x 1xx	9600bps allowed (V.32bis, V.32, V.29, V.17) 12000bps allowed (V.32bis, V.17, V.33) 14400bps allowed (V.32bis, V.17, V.33)

Note :
8. With conf 80 00 00 00 the coefficients of secondary tone detectors are not initialized.

VI - COMMAND SET DESCRIPTION (continued)

Parameters **CODER and DECODER Modes**

In the VOCODER Modes, either CODER or DECODER, (CONF_OPER equals 2 or 8) the parameters have the following meaning :

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	-	Define mode : see table above
CONF_CODE	3	0	0 1	Low bit rate coded ADPCM coded
CONF_VPF	3	1	0 1	Decoder post filter off Decoder post filter on (not in ADPCM)
CONF_VASP	3	3..2	00 01 10 11	ADPCM 32000 bps ADPCM 24000 bps ADPCM 16000 bps Reserved
CONF_EC	3	4	0 1	Line echo canceller disabled Line echo canceller enabled
CONF_SRC	3	5	0 1	Coder source is line input Coder source is audio input
CONF_SUPSIL	3	6	0 1	Coder silence supressor disabled Coder silence supressor enabled
CONF_ERCOR	3	7	0 1	Low bit rate decoder disable error correction Low bit rate decoder enable error correction

Parameters **ROOM-MONITOR Mode**

In the ROOM MONITOR Mode (CONF_OPER equals 9) the parameters have the following meaning :

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	1001	Define ROOM-MONITOR mode
CONF_EC	3	4	0 1	Line echo canceller disabled Line echo canceller enabled

Parameters **HANDSET/HANDSFREE Mode**

In the HANDSET/HANDSFREE mode (CONF_OPER equals C), the parameters have the following meaning :

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	1100	Define HANDSET/HANDSFREE mode
CONF_HFREE	3	7	0 1	Handset mode Handsfree mode
CONF_LEC	4	0	0 1	Line echo canceller enabled Line echo canceller disabled
CONF_AEC	4	1	0 1	Audio echo canceller enabled Audio echo canceller disabled
CONF_FULLD	4	2	0 1	Full duplex mode enabled Half duplex mode enabled
CONF_SOFT	4	3	0 1	Softclipping enabled Softclipping disabled
CONF_AGC	4	4	0 1	AGC enabled AGC disabled

CR — Complex Read — CR

Opcode: 11

0	0	0	1	0	0	0	1

Synopsis CR allows the reading of a complex parameter. The parameter specifies the parameter address (for the real part : the imaginary part is next location). CR returns the high byte value of both real and imaginary part of the addressed complex parameter (see Chapter VII “STATUS DESCRIPTION”).

Parameters

Field	Byte	Pos.	Value	Definition
CR_ADDR_L	1	7..0		Low byte of the 16-bit address
CR_ADDR_H	2	7..0		High byte of the 16-bit address

VI - COMMAND SET DESCRIPTION (continued)

CSE — Clear Error Status — CSE

Opcode: 08

0	0	0	0	1	0	0	0

Synopsis CSE is used to clear the ST75C540 error status SYSERR byte. It is also used as an acknowledge to the error condition handler.

Parameters

Field	Byte	Pos.	Value	Definition
ERR_MASK	1	7..0		Error mask. See report appendix for detailed meaning

DEFT — Define Arbitrary Tone — DEFT

Opcode: 0E

0	0	0	0	1	1	1	0

Synopsis DEFT programs one of the four tone generator for arbitrary tone generation. The parameter is the frequency of the generated tone expressed in Hertz between 0 and 3600Hz.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_GEN_SL	1	1..0		Index of the tone generator (3..0)
TONE_FREQ_L	2	7..0		Low byte of the frequency
TONE_FREQ_H	3	7..0		High byte of the frequency (internally masked with 0F)
TONE_SCALE	4	7..0		Amplitude scaling factor (high byte) 3F gives the nominal amplitude

DOSR — Define Optional Status Report — DOSR

Opcode: 0A

0	0	0	0	1	0	1	0

Synopsis DOSR specifies the address of the RAM variables to be monitored in the 4 locations STAOPT[0..3] of the dual port RAM. It also specifies the assignment within the 4 locations.

Parameters

Field	Byte	Pos.	Value	Definition
STA_OPT_ASS	1	1..0	0..3	Index of the STAOPT destination
STA_OPT_ADL	2	7..0		Low byte of source address
STA_OPT_ADH	3	3..0		High byte of source address
STA_OPT_HL	3	7	0 1	Select low byte of source Select high byte of source

DSIT — Define Status Interrupt — DSIT

Opcode: 13

0	0	0	1	0	0	1	1

Synopsis DSIT specifies the bit mask used with the STATUS[0] and STATUS[1] byte to generate an interrupt IT4 to controller. Each time a bit change happens in the status words, assuming the corresponding bit mask will be set, an interrupt will be generated.

Parameters

Field	Byte	Pos.	Value	Definition
STA_IT_MSK0	1	7..0		Status[0] bit mask pattern
STA_IT_MSK1	2	7..0		Status[1] bit mask pattern

Note : The default IT Status is 0x3F for STATUS[0] and 0xFF for STATUS[1].

VI - COMMAND SET DESCRIPTION (continued)

FORM — Select Transmission Format — FORM

Opcode: 09

0	0	0	0	1	0	0	1

Synopsis FORM defines the type of transmission used on the line.

Parameters

Field	Byte	Pos.	Value	Definition
X_SYNC	1	2..0	000* 001 010 011 100	Synchronous format Transmit continous "1" (1) HDLC framing Transmit continous "0" (1) UART
X_ANBIT	2	1..0	00 01	7 Bit per character 8 Bit per character
X_APAR	2	3..2	00 01 10	No parity Even parity Odd parity
X_ASTOP	2	5	0 1	1 stop bit(1) 2 stop bit(1)

Note : 1. Valid only when transmitting.

HSHK — Handshake — HSHK

Opcode: 04

0	0	0	0	0	1	0	0

Synopsis HSHK is used to command the ST75C540 to begin the transmit handshake sequence processing. The progress of the handshake is reported to the control processor.

Parameter Non parametric command.

IDT — Identify — IDT

Opcode: 14

0	0	0	1	0	1	0	0

Synopsis IDT Return the ST75C540 Hardware and Software release number. See paragraph VII.1.4.

Parameter Non parametric command.

INIT — Initialization — INIT

Opcode: 06

0	0	0	0	0	1	1	0

Synopsis INIT forces the ST75C540 to reset all parameters to their default conditions and restart operations.

Parameter Non parametric command.

Note : This command makes a software reset of the ST75C540 and so cannot have the regular handshake protocol. It does not increment the COMACK, neither generate an Interrupt.

JSR — Call a Low Level Subroutine — JSR

Opcode: 18

0	0	0	1	1	0	0	0

Synopsis JSR allows to execute a part of the ST75C540 firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

This instruction can be used with SGS-THOMSON Microelectronics Application Laboratory Support for special applications development or debugging needs. Contact your local representative.

VI - COMMAND SET DESCRIPTION (continued)

MODC — Modify Configuration — MODC

Opcode: 21

0	0	1	0	0	0	0	1

Synopsis MODC allows the modification of the parameters defined by the CONF command.

Parameters

Field	Byte	Pos.	Value	Definition
MODC_SDM	1	0	0 1	Normal data mode Short data mode (e.g. TVR) (5)
MODC_DV21F	1	1	0 1	Normal V.21ch2 (1) Disable V.21ch2 flag detector
MODC_DDTMF	1	2	0 1	Normal DTMF detector (1) Disable DTMF detector
MODC_DTDT4	1	3	0 1	Normal secondary tone detector (1) Disable secondary tone detector
MODC_DTDT16	1	4	0 1	Normal primary tone detector (1) Disable primary tone detector
MODC_SH	1	6	0* 1	Normal training sequence Short training sequence (2)
MODC_FS	1	7	0* 1	Secondary tone detector sampling frequency is 4.8kHz Secondary tone detector sampling frequency is 9.6kHz
MODC_V22G	2	1..0	00* 01 10	No guard tone 1800Hz guard tone (V.22bis/V.22) 550Hz guard tone (V.22bis/V.22)
MODC_FPT	2	3..2	00* 01 10	No echo protection tone Long echo protection tone (180ms) (4) Short echo protection tone (30ms) (4)
MODC_NOTA	2	4	0* 1	Answer mode : generate answer tone for handshake Originate mode : wait answer tone for handshake Answer mode : do not generate answer Originate mode : do not wait answer tone
MODC_NOSA	2	6	0* 1	Cut answer tone when receiving AA (V.32bis, V.32) Continue answer tone when receiving AA.
MODC_NOQA	2	7	0* 1	Enable V.32bis/V.32 autoretrain on quality. Disable V.32bis/V.32 autoretrain on quality.
MODC_ADCFD	3	0..3	0000* 0001 0010 0011 1111 1110 1101 0111 Other	Low bit rate decoder voice frame duration 30ms (nominal) Low bit rate decoder voice frame duration 35ms (+16%) Low bit rate decoder voice frame duration 40ms (+33%) Low bit rate decoder voice frame duration 45ms (+50%) Low bit rate decoder voice frame duration 25ms (-16%) Low bit rate decoder voice frame duration 20ms (-33%) Low bit rate decoder voice frame duration 15ms (-50%) Low bit rate decoder pause Reserved
MODC_COD	3	5	0 1	Low bit rate coder disabled Low bit rate coder enabled(3)
MODC_LEC	4	0	0 1	Line echo canceller enabled Line echo canceller disabled
MODC_AEC	4	1	0 1	Audio echo canceller enabled Audio echo canceller disabled(3)
MODC_FULLD	4	2	0 1	Full duplex mode enabled Half duplex mode enabled
MODC_SOFT	4	3	0 1	Softclipping enabled Softclipping disabled
MODC_AGC	4	4	0 1	AGC enabled AGC disabled

Notes :

1. In the modes where they are active.
2. Short train sequence must be preceded by at least one successful long train sequence at the same data rate. For V.17 a successful long train at any data rate must preceded the short train.
3. Only coder or decoder can be enabled at the same time.
4. Only when sending V.17, V.33, V.29 or V.27ter.
5. French Minitel Application (TVR : Teletel Vitesse Rapide).

VI - COMMAND SET DESCRIPTION (continued)

MR — Memory Read — MR

Opcode: 10

0	0	0	1	0	0	0	0

Synopsis MR allows the reading of a 16-bit parameter. The parameter specifies the parameter address.

Parameters

Field	Byte	Pos.	Value	Definition
MR_ADDR_L	1	7..0		Low byte of the 16-bit address
MR_ADDR_H	2	7..0		High byte of the 16-bit address

MRI — Memory Read Indirect — MRI

Opcode: 28

0	0	1	0	1	0	0	0

Synopsis MRI allows the reading of a 16-bit parameter. The parameter specifies an indirect address. Refer to the "RAM Mapping Application Note" (delivered on request according to revision number). The advantage to use MRI instead of MR is that the Indirect Address is constant over the different release of the product.

Parameters

Field	Byte	Pos.	Value	Definition
MRI_IADDR	1	7..0		Indirect Address

MRLO — Memory Read Low Word — MRLO

Opcode: 29

0	0	1	0	1	0	0	1

Synopsis MRLO allows the reading of the memory location which address coresponds to the previous MR or MRI Absolute Adress minus 1. This command must be preceded by a MR or MRI command. This command does not have any parameter. The double word reading is executed by the MR or MRI previous command.

MW — Memory Write — MW

Opcode: 12

0	0	0	1	0	0	1	0

Synopsis MW allows the writing of a 16-bit parameter. The parameter specifies the address as well as the value to be transferred.

Parameters

Field	Byte	Pos.	Value	Definition
MW_ADDR_L	1	7..0		Low byte of the 16-bit address
MW_ADDR_H	2	7..0		High byte of the 16-bit address
MW_VALUE_L	3	7..0		Low byte of the 16-bit value
MW_VALUE_H	4	7..0		High byte of the 16-bit value

VI - COMMAND SET DESCRIPTION (continued)

MWI — Memory Write Indirect — MWI

Opcode: 2A

0	0	1	0	1	0	1	0

Synopsis MWI allows the writing of a 16-bit parameter. The parameters specifies an indirect address as well as the value to be transferred. Refer to the "RAM Mapping Application Note" (delivered on request according to revision number). The advantage to use MWI instead of MW is that the Indirect Address is constant over the different release of the product.

Parameters

Field	Byte	Pos.	Value	Definition
MWI_IADDR	1	7..0		Indirect address
MWI_IVALUE_L	2	7..0		Low byte of the 16-bit value
MWI_IVALUE_H	3	7..0		High byte of the 16-bit value

MWLO — Memory Write Low Word — MWLO

Opcode: 2B

0	0	1	0	1	0	1	1

Synopsis MWLO allows the writing of a 16-bit parameter at the address defined by the following MW or MW Absolute Address minus 1. This command must be followed by a MW or MWI command. The double word writing is executed by the MW or MWI following command.

Parameters

Field	Byte	Pos.	Value	Definition
MWLO_VALUE_L	1	7..0		Low byte of the 16-bit value
MWLO_VALUE_H	2	7..0		High byte of the 16-bit value

RTRA — Retrain — RTRA

Opcode: 02A

0	0	0	0	0	1	0	1

Synopsis RTRA is used to force the ST75C540 to initiate a retrain sequence or a rate negotiation. If MODC_NOQUA bit is set, the ST75C540 will initiate a transmission at the maximum speed defined by the RTRA parameter, otherwise it will found the best reliable speed based on the quality of the line (within the RTRA allowed speed).

Parameters

Field	Byte	Pos.	Value	Definition
RTRA_NEG0	1	0	0 1	Retrain (V.22bis, V.32, V.32bis) Ratr negotiation (V.32bis, V.22bis)
RTRA_SP0	1	7..4	xxx1 xx1x x1xx 1xxx	1200bps allowed (V.22bis) 2400bps allowed (V.22bis) 4800bps allowed (V.32bis, V.32) 7200bps allowed (V.32bis)
RTRA_SP1	2	2..0	xx1 x1x 1xx	9600bps allowed (V.32bis, V.32) 12000bps allowed (V.32bis) 14400bps allowed (V.32bis)

VI - COMMAND SET DESCRIPTION (continued)

SETGN — Set Output Gain — SETGN

Opcode: 02

0	0	0	0	0	0	1	0

Synopsis SETGN is a command which sets the scaling factor of the transmit samples. It is used for setting the output level or for setting the level of the tone generators. The gain value is given in the form of a 2's complement 16-bit value.

Parameter

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-bit gain value
GAIN_H	2	7..0	range 7F*	High byte of the 16-bit gain value

Example

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	-5	47FA	-10	287A
-1	7214	-6	4026	-11	2413
-2	65AC	-7	392C	-12	2026
-3	5A9D	-8	32F5	-13	1CA7
-4	50C3	-9	2D6A	-14	198A

The multiplication factor is : $10^{(-1/20)} = 0.89125$ for 1dB step.

SLEEP — Turn to Sleep Mode — SLEEP

Opcode: 03

0	0	0	0	0	0	1	1

Synopsis SLEEP is used to force the ST75C540 to turn to low power mode.

Parameter Non parametric command.

Note : When receiving this command the ST75C540 will stop processing and so cannot have the regular handshake protocol. It does not increment the COMACK, neither generate an Interrupt.

STOP — FAX Stop Transmitter — STOP

Opcode: 25

0	0	1	0	0	1	0	1

Synopsis STOP is used, in FAX Modes, to force the ST75C540 to turn off the transmitter in accordance with the corresponding ITU-T V.33/V.17/V.29/V.27 recommendation.

Parameter Non parametric command.

Note : When receiving this command the ST75C540 will stop sending regular Data. This command must be preceded by a **XMIT** Stop command. The ST75C540 will wait until all the transmit buffers are sent before starting the Stop sequence.

SYNC — FAX Synchronize the Receiver — SYNC

Opcode: 26

0	0	1	0	0	1	1	0

Synopsis SYNC is used, in FAX Modes, to force the ST75C540 to Start/Stop the receiver in accordance with the corresponding ITU-T V.33/V.17/V.29/V.27 recommendation. As soon as the ST75C54 receives the **SYNC** Start command it sets its receiver to detect the FAX synchronization signal. This command is the equivalent **HSHK** command for the receiver.

Parameters

Field	Byte	Pos.	Value	Definition
RX_SYNC	1	0	0* 1	Stop receiver Start receiver synchronization

VI - COMMAND SET DESCRIPTION (continued)

TDRC — Tone Detector Read Coefficient — TDRC

Opcode: 1A

0	0	0	1	1	0	1	0

Synopsis TDRC Read one Coefficient of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	4..0	0..13	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 30 (1) 40 (1)	Biquad coefficient Energy coefficient Static level Energy coefficient for relative comparison Gain for relative comparison

The command answer is : Low Byte of Coefficient followed by High Byte of Coefficient.

Note 1 : Value 30 and 40 of byte 2 are available only for secondary tone detector.

TDRW — Tone Detector Read Wiring — TDRW

Opcode: 1B

0	0	0	1	1	0	1	1

Synopsis TDRW Read Wiring of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	4..0	0..13	Tone detector cell number

For primary tone detector

TD_W_ADDR	2	0	0 1 Other	Biquad and energy input Comparator inputs Reserved

The command answer is :

a) If TD_W_ADDR = 0 :

- First Byte is the Node Number of the Signal connected to Biquadratic Filter input.
- Second Byte is the Node Number of the Signal connected to the Energy estimator input.

b) if TD_W_ADDR = 1 :

- First Byte is the Node Number of the Signal connected to Comparator Negative input.
- Second Byte is the Node Number of the Signal connected to the Comparator Positive input.

For secondary tone detector TD_W_ADDR is not defined.

- First byte is 00 if relative comparison is not mandatory,
  First byte is 01 if relative comparison is mandatory.
- Second byte is for the configuration of the secondary tone detector :
  C0 configuration 1+1 of secondary tone detectors,
  E0 configuration 1+1+2,
  F0 configuration 1+1+1.

VI - COMMAND SET DESCRIPTION (continued)

TDWC — Tone Detector Write Coefficient — TDWC

Opcode: 1C

0	0	0	1	1	1	0	0

Synopsis TDWC Write one Coefficient of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	4..0	0..13	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 30 (1) 40 (1)	Biquad coefficient Energy coefficient Static level Energy coefficient for relative comparison Gain for relative comparison
TD_COEFL	3	7..0		Low byte of coefficient
TD_COEFH	4	7..0		High byte of coefficient

Note 1 : Value 30 and 40 of byte 2 are available only for secondary tone detector.

TDWW — Tone Detector Write Wiring — TDWW

Opcode: 1D

0	0	0	1	1	1	0	1

Synopsis TDWW Write Wiring of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	4..0	0..13	Tone detector cell number

For Primary Tone Detector

Field	Byte	Pos.	Value	Definition
TD_W_ADDR	2	0	0 1 Other	Biquad and energy input Comparator inputs Reserved

If TD_W_ADDR = 0 (Select Biquad and Energy Inputs)

Field	Byte	Pos.	Value	Definition
TD_W_ERN	3		0..3F	Energy estimator signal input
TD_W_BIQ	4		0..3F	Biquad filter signal input

If TD_W_ADDR = 1 (Select Comparator Inputs)

Field	Byte	Pos.	Value	Definition
TD_W_CN	3		0..3F	Negative comparator signal input
TD_W_CP	4		0..3F	Positive comparator signal input

For Secondary Tone Detector

Field	Byte	Pos.	Value	Definition
TD_4DIFF	2	7..0	00 01 other	Relative comparison not enable Relative comparison enable Reserved
TD_4_CONF	3	7..0	0	Mandatory
TD_4_CONF2	4	7..0	C0 E0 F0 other	1+1 configuration 1+1+2 configuration 1+1+1+1 configuration Reserved

VI - COMMAND SET DESCRIPTION (continued)

TDZ — Tone Detector Clear Cell — TDZ

Opcode: 1E

0	0	0	1	1	1	1	0

Synopsis TDZ Clears all internal variables of one Tone detector cell including Filter local variables and energy estimator. This command must be sent after changing coefficients of a cell to avoid instability.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	4..0	0..13	Tone detector cell number

TGEN — Enable/Disable Tone Generators — TGEN

Opcode: 0D

0	0	0	0	1	1	0	1

Synopsis Enable or disable one of the four tone generator, define the output of the tone generator either Line or Audio.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_0_ENA	1	0	0* 1	Generator #0 disabled Generator #0 enabled
TONE_1_ENA	1	1	0* 1	Generator #1 disabled Generator #1 enabled
TONE_2_ENA	1	2	0* 1	Generator #2 disabled Generator #2 enabled
TONE_3_ENA	1	3	0* 1	Generator #3 disabled Generator #3 enabled
TONE_0_OUT	1	4	0* 1	Generator #0 output to line Generator #0 output to audio
TONE_1_OUT	1	5	0* 1	Generator #1 output to line Generator #1 output to audio
TONE_2_OUT	1	6	0* 1	Generator #2 output to line Generator #2 output to audio
TONE_3_OUT	1	7	0* 1	Generator #3 output to line Generator #3 output to audio

VI - COMMAND SET DESCRIPTION (continued)

TONE — Predefined Tones — TONE

Opcode: 0C

0	0	0	0	1	1	0	0

Synopsis TONE programs the tone generator for the predifined tones. The tone generator #0 and eventualy #1 are reprogrammed with this command. The tone generator #0 and eventualy the #1 are enabled. Using a value not in the following table will disable tone generator #0 and #1.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_SELECT	1	5..0	0	DTMF digit 0
			1	DTMF digit 1
			2	DTMF digit 2
			3	DTMF digit 3
			4	DTMF digit 4
			5	DTMF digit 5
			6	DTMF digit 6
			7	DTMF digit 7
			8	DTMF digit 8
			9	DTMF digit 9
			A	DTMF digit A
			B	DTMF digit B
			C	DTMF digit C
			D	DTMF digit D
			E	DTMF digit *
			F	DTMF digit #
			10	Answer tone 2100Hz
			11	Tone 1650Hz
			12	Tone 2225Hz
			13	Tone 1300Hz
			14	Tone 1100Hz
TONE_OUT	1	7	0	Output on line
			1	Output on audio

XMIT — Start/stop Transmission — XMIT

Opcode: 01

0	0	0	0	0	0	0	1

Synopsis XMIT start or stop the transmission of the Transmit Data.

Parameters

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0*	Stop transmission
			1	Start transmission

VII - STATUS DESCRIPTION

This appendix is dedicated to the ST75C540 reporting features. In the following sections the command acknowledge process and the report and status definitions are explained.

VII.1 - Command Acknowledge and Report
VII.1.1 - Command Acknowledge Process

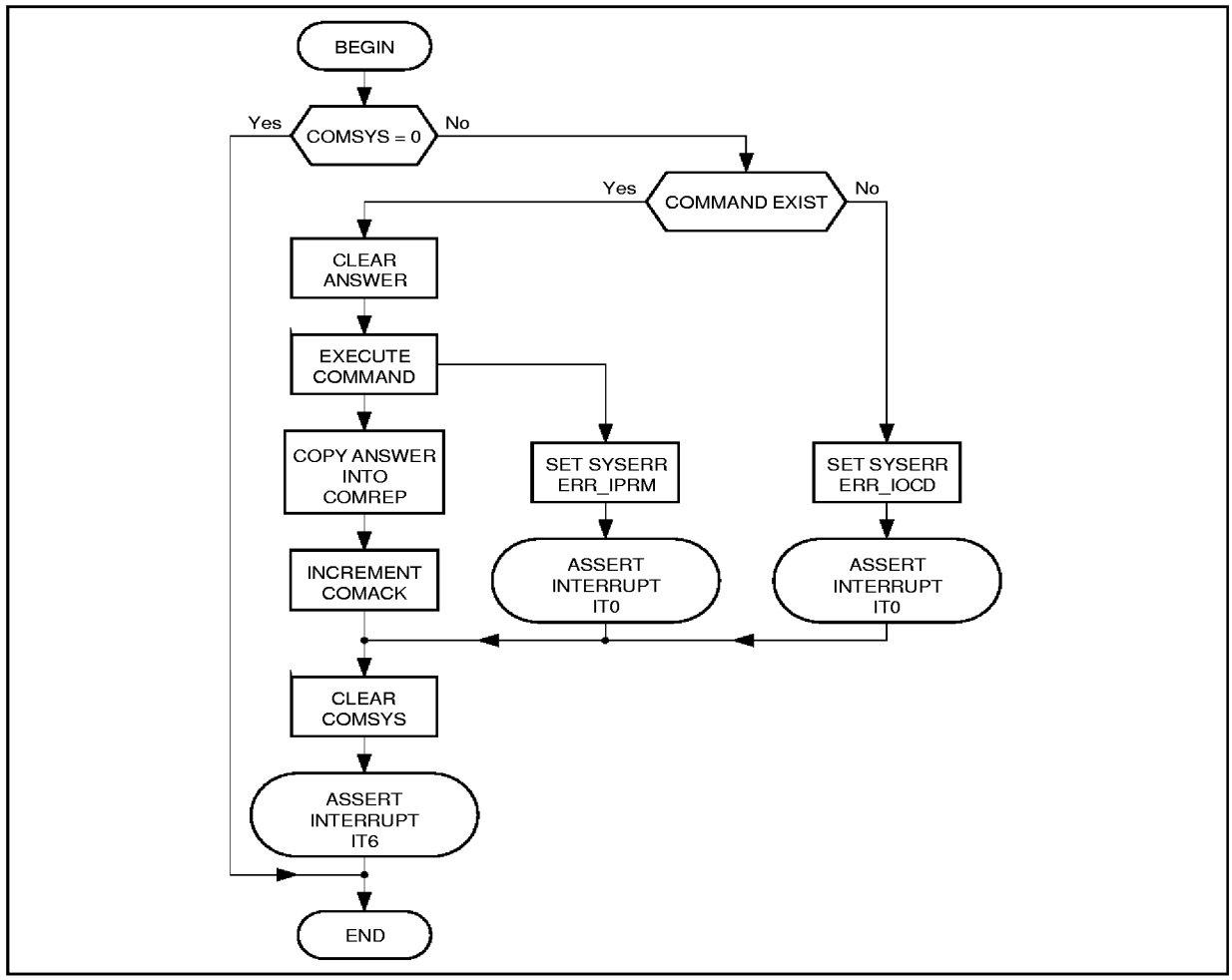
The ST75C540 features an acknowledge process based on a counter COMACK. On power-on reset (or INIT command), this counter's value is set to 0. Each time a command is successfully executed by the ST75C540, the acknowledge counter COMACK is incremented. This allows a precise monitoring of the command entered and avoids command collision.

In the case of a memory reading command (CR, TDRC, TDRW, IDT or MR) once the command entered is executed, the report area is filled and the acknowledge counter is incremented afterwards. This insures that the controller will read the value corresponding to its request.
Furthermore, the ST75C540 resets the value of the COMSYS register and the interruption IT6 is raised.

VII.1.2 - Reports Specification

The report section of the Dual Port RAM is dedicated to memory reading. In response to a CR, MR, MRI, MRLO, TDRC, TDRW, IDT commands, the value read is transferred to the report registers COMREP[0..1].

Figure 16 : Command Acknowledge Process



VII - STATUS DESCRIPTION (continued)

VII.1.3 - CR Command

Issuing a CR command causes the ST75C540 to dump a specific memory location in complex mode. This instruction is particularly useful for equalizer state analysis or for software eye-pattern display. The report area has this meaning :

RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0	COMREP[0]
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	COMREP[1]

RP0..RP7 is the MSB part of the 16-bit value of the real part and IP0..IP7 is the MSB part of the imaginary part. The CR command insures that the real and imaginary part of the desired complex value are sampled internally at the same time. The address given in the parameter field of CR is the address of the real part.

VII.1.4 - MR/TDRC/TDRW/IDT/MRI/MRLO Commands

The report issued by the MR/TDRC/TDRW/IDT/MRI/MRLO commands follow the same rules as for CR. The report meaning is :

D7	D6	D5	D4	D3	D2	D1	D0	COMREP[0]
D15	D14	D13	D12	D11	D10	D9	D8	COMREP[1]

D0..D15 is the 16-bit value requested by the command.

In the case of IDT, D15..D12 contains the product identification (4 for ST75C540), D11..D8 contains the hardware revision identification and D7..D0 contains the software revision identification.

VII.2 - Modem Status

VII.2.1 - Modem Status Description

The Status of ST75C540 is divided into 4 fields :

- The error status byte SYSERR that provides information about error. This status can trigger an IT0 interrupt,
- The general status byte STATUS[0] and STATUS[1] that contains all the modem signals. These status bytes can trigger an IT4 interrupt,
- The quality status STAQUA, that contains the quality of the received transmission,
- The optional status bytes STAOP[0], STAOP[1], STAOP[2] and STAOP[3], that contains additional information regarding the ST75C540 operating mode. This default information can be changed to monitor any internal variables using the DOSR command.

All these informations are updated on a Baud basis :

Mode	Baud Rate (2) (Hz)
V.32bis/V.32	2400
V.22bis/V.22/Bell 212A	2400
Tone	2400
Bell 103 (full duplex)	2400
V.21 (full duplex)	2400
V.23 (full duplex)	2400
V.27ter 2400bps	1200
V.27ter 4800bps	1600 (1)
V.29	2400
V.17/V.33	2400
V.21 channel 2	2400
HANDSET, CODER or DECODER Modes	1200

Notes : 1. In this mode the tone detectors outputs are update 800 times by second.
2. This baud rate defines also, the maximum command rate. Each baud time the ST75C540 looks at the COMSYS location (Address $00) to see if a command have been sent by the host processor. If the content of this location is different from zero the ST75C540 execute the command.

VII - STATUS DESCRIPTION (continued)

Starting at the adddress $08 the status area have the following format :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$08	SYSERR	ERR_RTK	-	-	ERR_IPRM	ERR_IOCD	ERR_VOCO	ERR_RX	ERR_TX
$09	STATUS0	STA_109F	STA_CPT10	STA_CPT1	STA_CPT0	STA_RING	STA_106	STA_107	STA_109 STA_VAD
$0A	STATUS1	STA_DTMF	STA_FLAG STA_CLR	STA_RNEG	STA_HR STA_RTRN	STA_AT	STA_CCITT	STA-TIM	STA_H
$0B	STAQUA	-	Quality						
$0C	STAOP0	Depend on operating mode (see below)							
$0D	STAOP1								
$0E	STAOP2								
$0F	STAOP3								

VII.2.2 - Error Status

The error status changes each time an error occurs. When the ST75C540 signals an error by setting one of the SYSERR bit, it generates an interrupt IT0. These bits can only be cleared by the host controler using the CSE command.

The meaning of the different bits of the SYSERR byte is discribed below :

SYSERR		
Field	**Pos.**	**Meaning when set**
ERR_TX	0	Transmit buffer underflow. Loss of synchronisation between the host and ST75C540 transmit data buffer managment.
ERR_RX	1	Receive buffer overflow. Loss of synchronisation between the host and ST75C540 receive data buffer managment.
ERR_VOCO	2	Vocoder buffer underflow (Decoder) or overflow (Coder). Lost of synchronisation between the Host and ST75C540 VOCODER Buffer management.
ERR_IOCD	3	Incorrect command
ERR_IPRM	4	Incorrect parameter for the command
ERR_RTK	7	Real time kernel error. ST75C540 not able to perform all its tasks within the baud period (transmit or receive samples lost).

VII - STATUS DESCRIPTION (continued)

VII.2.3 - Modem General Status

The modem general status word is composed of two bytes STATUS[0] and STATUS[1]. Any bit change can generate an IT4 interrupt. Using the DSIT command allows the selection of the corresponding bit that will generate an interrupt each time they will change. The default pattern is $3F for STATUS[0] and $FF for STATUS[1].

The different bits have the following meaning :

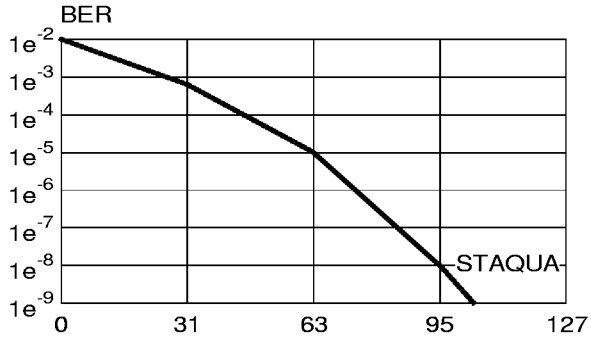
STATUS[0]		
Field	**Pos.**	**Meaning when set**
STA_109 STA_VAD	0	In FAX MODEM and TONECID modes STA_109 : CCITT Circuit 109 (Carrier Detect). Indicates that valid data are received. In CODER and DECODER modes : VAD: Voice Activity Detected
STA_107	1	CCITT Circuit 107 (Data Set Ready). Valid only inFAX & DATA MODEM modes.
STA_106	2	CCITT Circuit 106 (Clear To Send). Indicates that the training sequence has been completed and that any data in the Transmit Buffer will be transmitted. Valid only in FAX & DATA MODEM modes.
STA_RING	3	Ring Detected. A valid ring signal is present at the Ring pin. Valid only in Tones modes. The precise frequency can be read in the optional status byte STAOP2.
STA_CPT0	4	In TONE and TONECID modes STA_CPT0: Call progress tone detector #0. Low pass filter 650Hz.
STA_CPT1	5	In TONE and TONECID modes STA_CPT1: Call progress tone detector #1. High pass filter 600Hz.
STA_CPT10	6	In TONE and TONECID modes STA_CPT10: Signal in Filter #0 is higher than #1.
STA_109F	7	In FAX MODEM mode, V.22bis mode and TONECID mode STA_109F: Fast Carrier Detect.

STATUS[1]		
Field	**Pos.**	**Meaning**
STA_H	0	Transmit synchronisation in progress. Valid only in FAX & DATA MODEM modes.
STA_TIM	1	Handshake timeout. Valid only in Data Modem mode.
STA_CCITT	2	CCITT 2100Hz versus 2225Hz answer tone detect. Valid if STA_AT is set. Valid only in Tone mode.
STA_AT	3	Answer tone (either 2100Hz or 2225Hz) detected. Valid only in Tone mode.
STA_HR STA_RTRN	4	STA_HR : Receive synchronisation in progress. Valid only in Fax Modem mode. STA_RTRN : Remote retrain detec, valid only in V.32bis/V.32/V.22bis Data Modem modes.
STA_RENEG	5	Remote rate negotiation detected, valid only in V.32bis/V.32/V.22bis Data Modem modes.
STA_FLAG STA_CLR	6	STA_FLAG : V.21 channel 2 flag detect. Valid only in FAX Modem mode and Tone mode. STA_CLR : Remote clear down detected V.32bis/V.32 Data Modem modes.
STA_DTMF	7	DTMF digit detect. The digit itself is available in the optional status byte STAOP3.

VII - STATUS DESCRIPTION (continued)

VII.2.4 - Quality Status

The quality bytes STAQUA and STAQUAS monitor an evaluation of the line quality. They are updated once per baud and their value ranges from 127 (perfect quality) to 0 (terrible quality). This value is automaticaly adjusted according to the current receiving mode. Refer to the following chart to convert the value of STAQUA into its Bit Error Rate equivalence. The time constant for STAQUA is 100ms. The slow quality byte (available on STAOP1 in Fax and Data mode except FSK) STAQUAS gives the equivalent quality with a 1 seconde time constant.



75C54021.EPS

VII.2.5 - Optional Status

According to the operating mode of the ST75C540 the optional status is displaying different informations.

The optional status are automatically reprogrammed after each CONF command with the address of the variables to monitor according with the operating mode selected (CONF_OPER). After the CONF command the user must overwrite this default programming by using the DOSR command. In order to change the default set-up please refer to the "RAM Mapping application note" (delivered on request according to revision number) to obtain the addresses of the DSP Internal variables.

VII.2.5.1 - Default Optional Status in All modes Except MODEM

While in Tone mode the format of the STAOP word is as follows :

Optional Status Words									
Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7	TDT6	TDT5	TDT4	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15	TDT14	TDT13	TDT12	TDT11	TDT10	TDT9	TDT8
$0E	STAOP2	RING_PERIOD (1)							
$0F	STAOP3	TDT19	TDT18	TDT17	TDT16	DTMF_DIGIT(4)			

Notes : 1. RING_PERIOD is valid when the Bit 3 of the STATUS0 (STA_RING goes high. This value is updated at each falling edge of the RING Signal. The RING_PERIOD value must be multiplied by 2400 to obtain the Period in second.

2. TDTx (x in [0..15]) is the Output of the 16 Tone detectors x (sampling rate 7200Hz).
3. TDTy (y in [16..19] is the Output of the secondary Tone detectors (sampling rate 4800Hz or 9600Hz) with absolute comparison or relative comparison.
4. DTMF_DIGIT is valid when the Bit 7 of STATUS1 (STA_DTMF) goes high. This value remains unchanged until a new DTMF Digit is detected.

VII - STATUS DESCRIPTION (continued)

VII.2.5.2 - Default Optional Status in Fax Mode

While in Fax Modem mode the format of the STAOP word is as follows :

Optional Status Words in MODEM Mode									
Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	x	x	x	SPEED (2)(5)				SPVAL (1)(5)
$0D	STAOP1	STAQUAS							
$0E	STAOP2	PNSUCs	PRDETs	PNDETs	SCR1s	PRs	PNs	P2s	P1s
$0F	STAOP3	TDT19	TDT18	TDT17	TDT16	DTMF_DIGIT(4)			

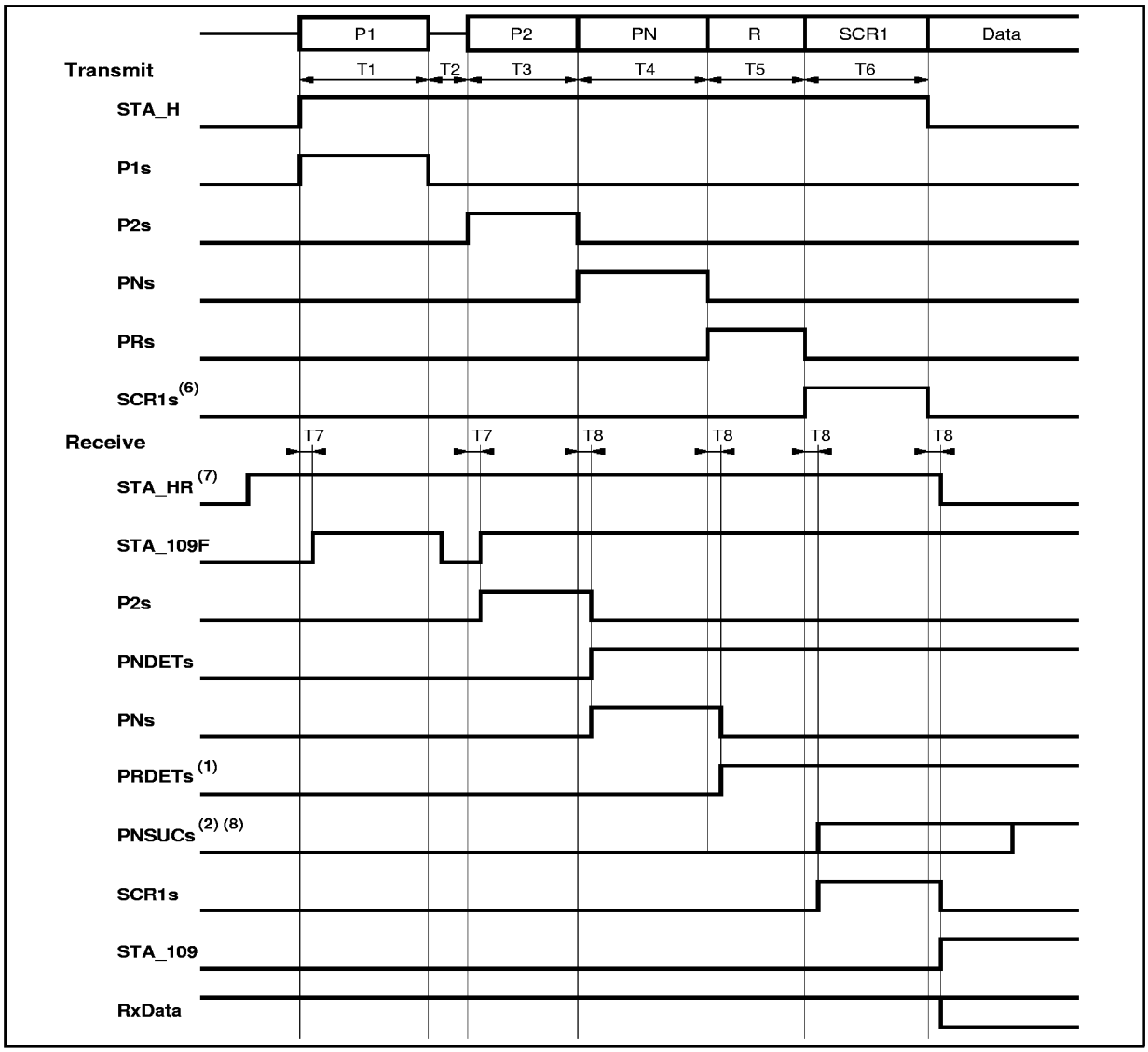
Notes : 1. SPVAL is active in V.33 receiver only at the same time as the rising transition of the SCR1s signal. When SPVAL is set, it indicates that the SPEED bits contain the Data speed information.
2. SPEED is valid in V.33 receiver only it can have 2 values, after the SCR1s signal goes high : 1000 for 14400bps and 0111 for 12000bps.
3. The STAOP2 Bit reflects the progression of the Synchronisation.
4. Only valid in V.21 Channel 2 Receive mode.

The STAOP2 Bits have the following meanings :

STAOP2 in Fax Modem Mode		
Name	Position	Description
P1s	0	Unmodulated carrier sequence. Optional, used for echo protection.
P2s	1	Continuous 180° phase reversal sequence
PNs	2	Equalizer trainning sequence
PRs	3	V.33 and V.17 rate sequence
SCR1s	4	Continuous scrambled 1 sequence
PNDETs	5	Turned on after PN sequence detection
PRDETs	6	Turned on after PR sequence detection (V.33 and V.17 only)
PNSUCs	7	Turned on after succesfull training of the receive equalizer. When on at the end of the synchronization, the transmition BER is statisticaly bellow 10ppm.

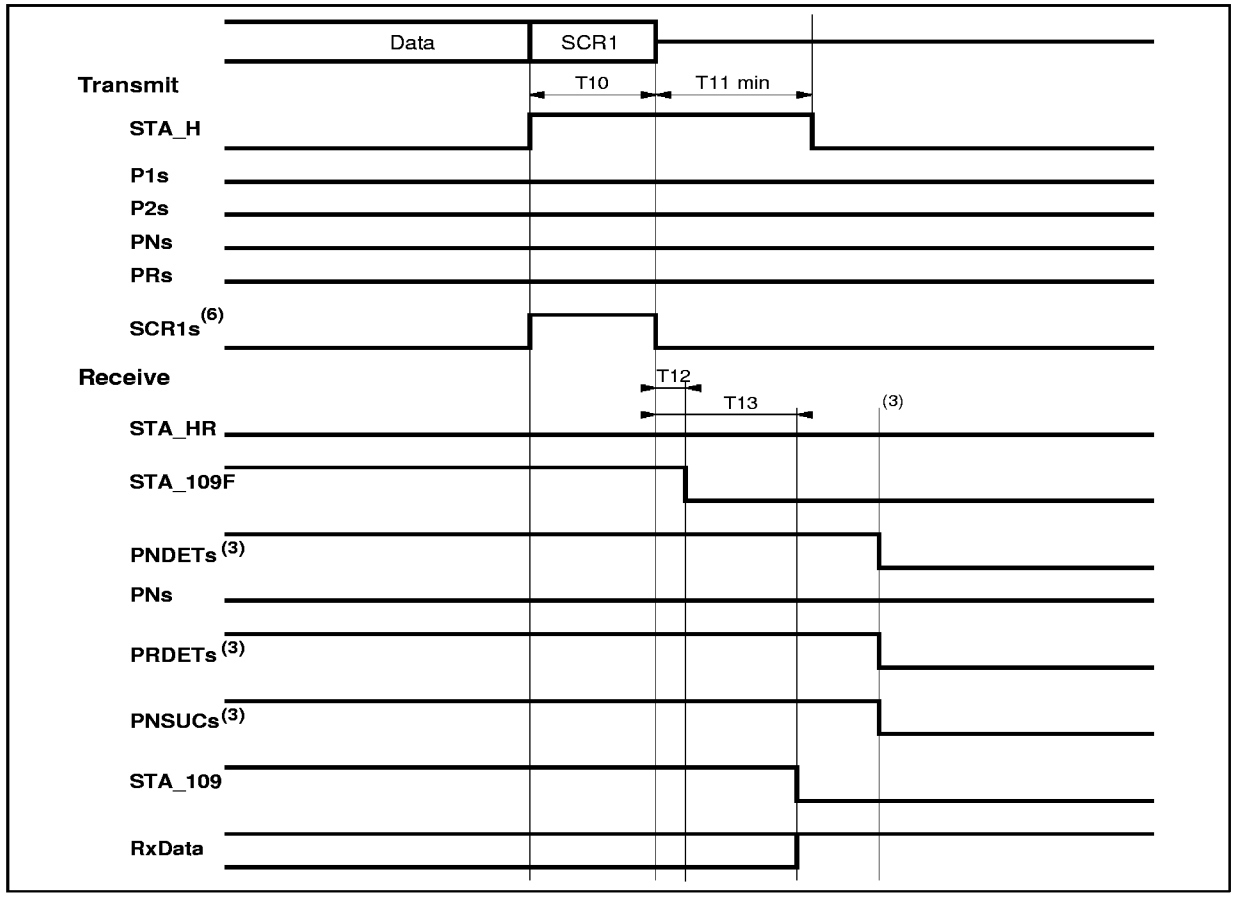
VII - STATUS DESCRIPTION (continued)

With the following timing :



Mode	T1 (4)	T1p (5)	T2	T3	T4	T5	T6	T7	T8	Unit
V.17	192	30	22	107	1240	27	20	5	7	ms
V.17 short	192	30	22	107	16	0	20	5	7	ms
V.29	192	30	22	53	160	0	20	5	7	ms
V.29 short	192	30	22	41	26	0	8	5	7	ms
V.27 4800	192	30	22	31	670	0	5	5	7	ms
V.27 4800 short	192	30	22	9	36	0	5	5	7	ms
V.27 2400	192	30	22	42	895	0	7	6	7	ms
V.27 2400 short	192	30	22	12	48	0	7	6	7	ms

VII - STATUS DESCRIPTION (continued)



Mode	T10	T11	T12	T13	Unit
V.17	13	20	8	25	ms
V.17 short	13	20	8	25	ms
V.29	13	20	8	25	ms
V.29 short	13	20	8	25	ms
V.27 4800	20	30	8	25	ms
V.27 4800 short	20	30	8	25	ms
V.27 2400	27	40	8	25	ms
V.27 2400 short	27	40	8	25	ms

Notes : 1. In the case of V.29 or V.27, PRs and PRDETs bits are not active.
2. PNSUCs indicates the quality of the Rx signal that will give a ber of approximation of $1e^{-5}$.
3. After sending the command SYNC0, all bits are reset.
4. When using long echo protection tone, otherwise 0.
5. When using short echo protection tone, otherwise 0.
6. STA-106 is set at the end of T6 and reset at the beginning of T10.
7. After sending the command SYNC1, this bit is set.
8. PNSUC is evaluated twice, first at SCR1 detection and further 256 baud (V.29, V.17, V.33 : 106ms ; V.27 4800bps : 160ms ; V.27 2400bps : 212ms) after STA_109.
9. For V.21 channel 2, timing for loss of STA_109 is 25ms and timing for detection of STA_109 is 7ms.
10. For V.21 channel 2 after a STOP command, STA_H is set to "1" during 13ms when the last HDLC flag is transmitted.

VII - STATUS DESCRIPTION (continued)

VII.2.5.3 - Default Optional Status in DATA MODEM Mode

While in Data Modem mode the format of the STAOP word is as follows :

Optional Status Words in MODEM Mode									
Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	x	x	x	SPEED (2)(5)				SPVAL (1)(5)
$0D	STAOP1	STAQUAS							
$0E	STAOP2	**HSHK_PHA**							
$0F	STAOP3	TDT19	TDT18	TDT17	TDT16	Not Used			

Notes : 1. SPVAL is active in V.33 receiver only at the same time as the rising transition of the SCR1s signal. When SPVAL is set, it indicates that the SPEED bits contain the Data speed information.

2. SPEED is valid in V.32bis, V.32, V.22bis, V.22, Bell 212A and V.33 receiver only with the following meaning :

Bit 4	Bit 3	Bit 2	Bit 1	Data Speed
0	0	1	0	1200bps
0	0	1	1	2400bps
0	1	0	0	4800bps
0	1	0	1	7200bps
0	1	1	0	9600bps
0	1	1	1	12000bps
1	0	0	0	14400bps
Other				Reserved

3. The STAOP2 Bit reflects the progression of the Synchronisation.
4. Only valid in V.21 Channel 2 Receive mode.
5. SPVAL is active in V.32bis/V.32/V.22bis/V.22 at the end of the training sequence and at least 8 baud before entering Data mode. SPVAL and SPEED are also updated with each retrain and rate negotiation.
6. The SPAOP1 bits reflect the progression of the synchronization in Data modes.

VII - STATUS DESCRIPTION (continued)

The STAOP2 Bits have the following meanings in Data Modem mode :

HSHK_PHA(R) Handshake progression counter contains information about the progress of the hadshake in V.32 and V.22bis modes. This 8-bit value is available in STAOP2 in modem mode. It can be read to examine the progressio of the handshake and it contains normal values and error values as below :

AUTOBAUD ORIG MODE

Event	HSHK_PHA Value
Wait Answer Tone	$01
Wait End Answer Tone	$02
Not Autobaud and Waiting	$03
USC1	$04
Autobaud Waiting AC or USC1	

AUTOBAUD ANSW MODE

Event	HSHK_PHA Value
Waiting HSK Command	$10
Generating Answer Tone	$11
Generating Silence	$12

V.32 ORIG MODE

EVENT	HSHK_PHA Normal Value	HSHK_PHA Error Value
AC_DET	$20	
AC/CA DET	$21	$1
CA/AC DET	$22	$2
NO AC DET	$23	$B for RTN, $C for RTN
S_DET	$24	$4
SB_DET	$25	$5
R1_DET	$26	$6
S_DET	$27	$7
SB_DET	$28	$8
R3_DET	$29	$9, $D no R5 det after RRN
E_DET	$2A	$A
DATA_MODE	$30	

V.32 ANSW MODE

EVENT	HSHK_PHA Normal Value	HSHK_PHA Error Value
AA_DET	$40	$8 for RTN, $9 for RRN
AA/CC DET	$41	$1
NO CC DET	$42	$2
S_DET	$43	$3
SB_DET2	$44	$4
SB_DET	$45	$5
R2_DET	$46	$6, $A if no R det after RRN
E_DET	$47	$7
DATA_MODE	$50	

V.22bis ORIG MODE

EVENT	HSHK_PHA Normal Value
HSHK	$60
USC1_DET	$61
SCR1_DET	$62
S1_DET	$63
DATA_MODE	$70

V.22bis ANSW MODE

EVENT	HSHK_PHA Normal Value
HSHK	$80
SCR1_DET	$82
S1_DET	$83
DATA_MODE	$90

VIII - TONE DETECTORS

VIII.1 - Overview

The general purpose ST75C540 tone detectors block is a powerful module that covers a lot of applications :

- call progress tone detection, fully programmable for all countries,
- FAX, voice, data automatic detection,
- call waiting detection, while in vocoder or data mode.

VIII.2 - Description

The primary tone detector block is a set of 16 identical Cells. Each cell is composed of a Double Biquadratic Filter, a Power estimator section, a Static level and a Level comparator.

Each Biquadratic Filter, Power Estimator and Static Level can be programmed using a complete set of commands (**TDRC**, **TDRW**, **TDWC**, **TDWW**, **TDZ**).

The wiring between the different Cells can be defined by the user, using the associated command allowing a wide range of applications.

The sampling frequency is 7200Hz, allowing detection of signals less than 3300Hz. The level of detection is programmable from -6dBm down to -51dBm.

The 16 Comparator Outputs give, on a baud basis, the information into two 8 bits words **TONEDET0** (for cells number 0 to 7) and **TONEDET1** (for cells number 8 to F). These TONEDET variables can be accessed using a **MRI** command or, more easily, monitored on a baud basis using the **DOSR** command.

The 16 primary tone detectors are initialized each time entering the tone mode. However the previous coefficient values could be kept using a **MW** command.

The secondary tone detector have been added to the ST75C540. The filter structure is the same as the primary tone detector.

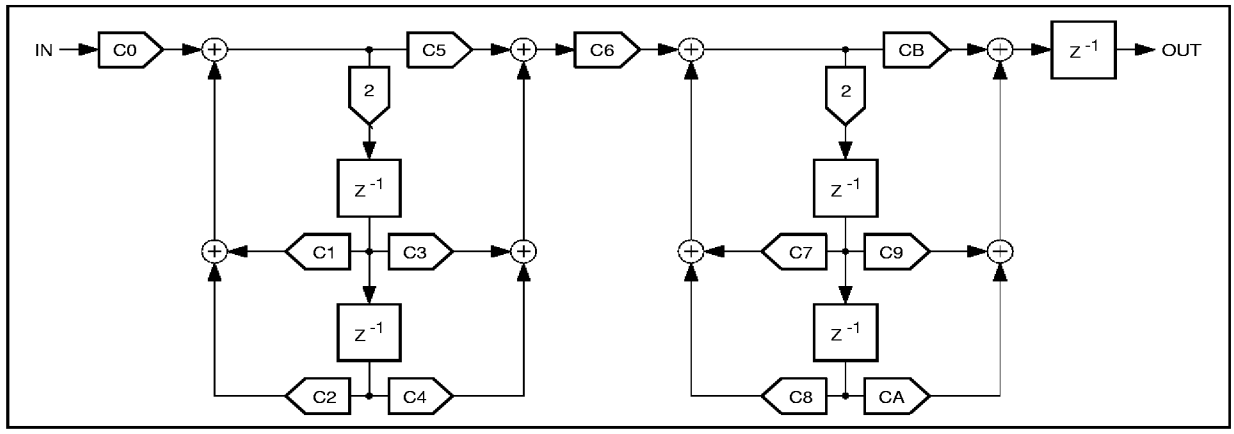
The sampling rate is 4800Hz allowing detection of signal less than 1800Hz by default programming or with a **MODC** command, the sampling rate is 9600Hz allowing detection of signal less than 3300Hz. The level of detection is programmable from -6dBm down to -51dBm. In order to increase the reliability of the detection, using a **TDWW** command, 2 comparisons are provided, one with a fixed level (absolute) or with the receive signal (relative). The 4 secondary tone detectors are initialiazed each time entering the tone mode. However the previous coefficient values could be kept using a **CONF** command.

The command TDRC, TDWC, TDWW, TDRW, TDZ with the TD_CELL parameter of 0x10, 0x11, 0x12 or 0x13 can be used to program these filters.

VIII.2.1 - Biquadratic Filters

Each Biquadratic Filter is a double regular section that can perform any Transfer function with 4 Poles and 4 Zeros.
This routine is run on a sample basis.

Figure 17 : Biquadratic IIR Filter



The corresponding transfer function is :

$$\frac{Out}{Input} = C0 \cdot \frac{C5 + 2 \cdot C3 \cdot z^{-1} + 2 \cdot C4 \cdot z^{-2}}{1 - 2 \cdot C1 \cdot z^{-1} - 2 \cdot C2 \cdot z^{-2}} \cdot C6 \cdot \frac{CB + 2 \cdot C9 \cdot z^{-1} + 2 \cdot CA \cdot z^{-2}}{1 - 2 \cdot C7 \cdot z^{-1} - 2 \cdot C8 \cdot z^{-2}} \cdot z^{-1}$$

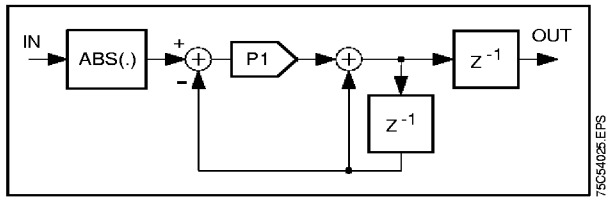
Note : All coefficients are coded on 16 bits 2's complement in the range +1, -1 (Q15). To avoid the possibility of overflow the user must check that the internal node must not be higher that 0.5 (in Q15 representation).

VIII - TONE DETECTORS (continued)

VIII.2.2 - Power Estimation

The Power estimation Cell is needed to measure the amplitude of the different tones. It is run on a sample basis.

Figure 18 : Power Estimator



The corresponding transfer function is :

$$Out = \left| Input \right| \cdot z^{-1} \cdot \frac{P1}{1 - (1 - P1) \cdot z^{-1}}$$

VIII.2.3 - Static Level

A single Threshold level is associated with each Cell. It can be use to compare the output of a Power Estimation with an Absolute Value.

VIII.2.4 - Comparator

The Comparator computes, on a baud basis, the difference of the signal on its Positive and Negative Inputs. If the result is Higher that zero it sets the corresponding bit into the TONEDET[0..1] word; if not it clear this bit.

VIII.2.5 - Wiring

The user must specify the connection (wiring) between the input/output of the Filter, the input/output of the Power estimator, the output of the static levels and the two inputs of the Comparators.

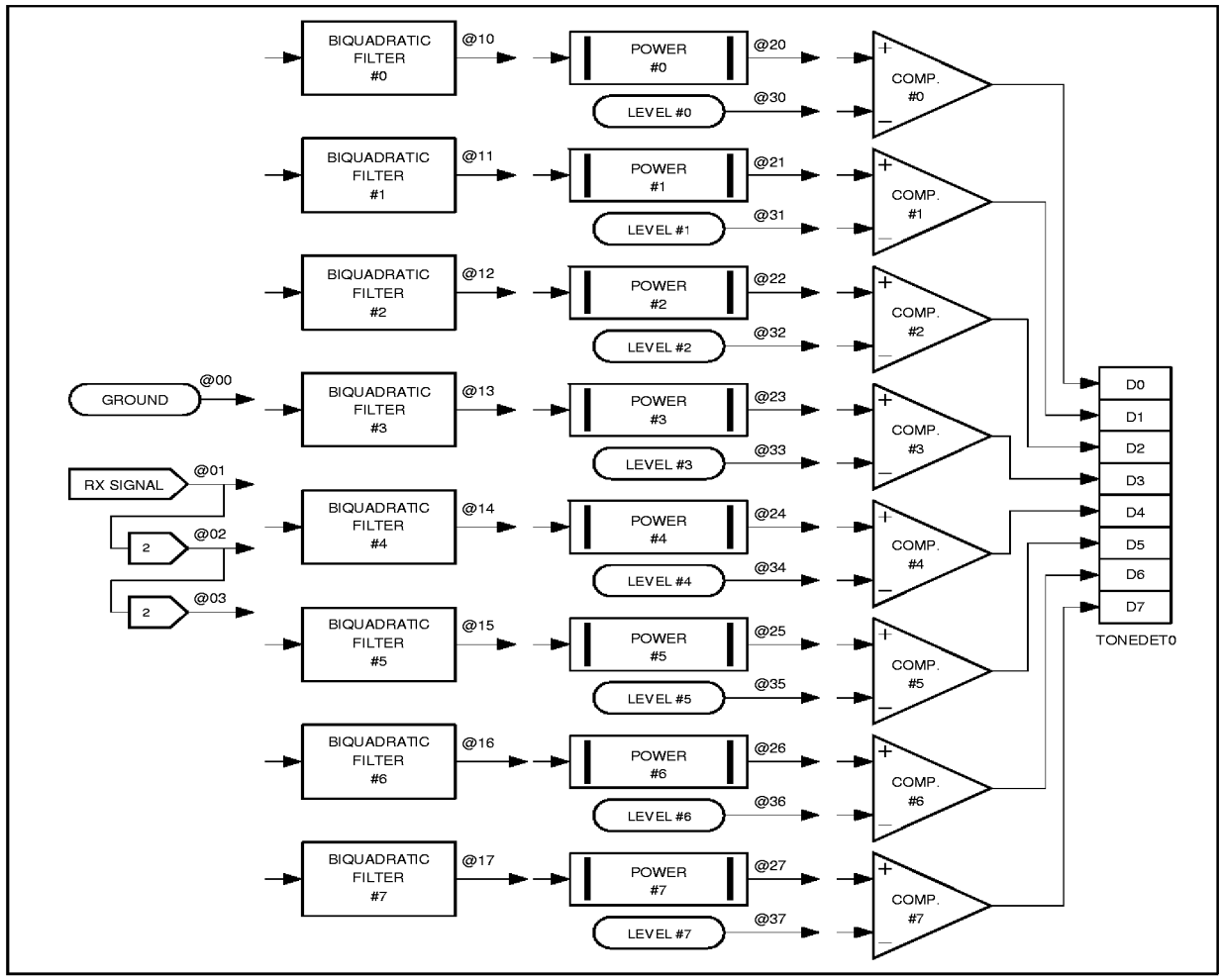
The output signals have an absolute address:

Node Address		
Signal Name	**Address**	**Description**
Ground	00	Signal always equal to 0000
RxSig	01	Receive signal from the Analog front end
RxSig2	02	Receive signal multiplied by 2
RxSig4	03	Receive signal multiplied by 4
	04..0F	Reserved
Filter[0..F]	10..1F	Biquadratic Filter Outputs
Power[0..F]	20..2F	Power Estimator Outputs
Level[0..F]	30..3F	Static Levels

The user will specify the inputs of the filters, Power and Comparator. At least one input must come from the RxSig (node 01, 02 or 03). It is mandatory to connect all unused cell inputs to the Ground signal (node 00).

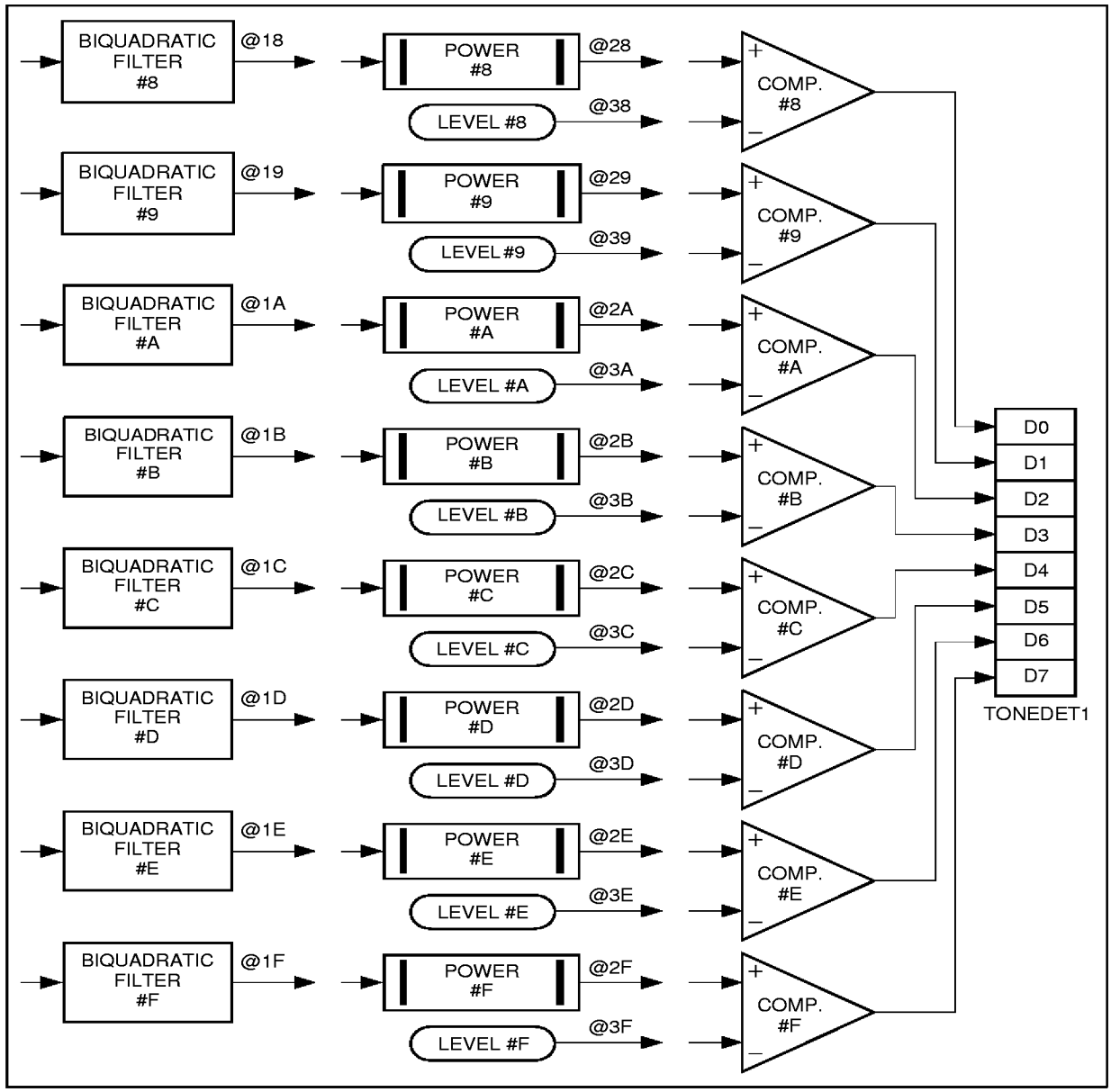
VIII - TONE DETECTORS (continued)

Figure 19 : Tone Detector Wiring Address (first half)



VIII - TONE DETECTORS (continued)

Figure 20 : Tone Detector Wiring Address (second half)



VIII - TONE DETECTORS (continued)

Figure 21a : Secondary Tone Detector Configuration (2 tone detectors 1 + 1)

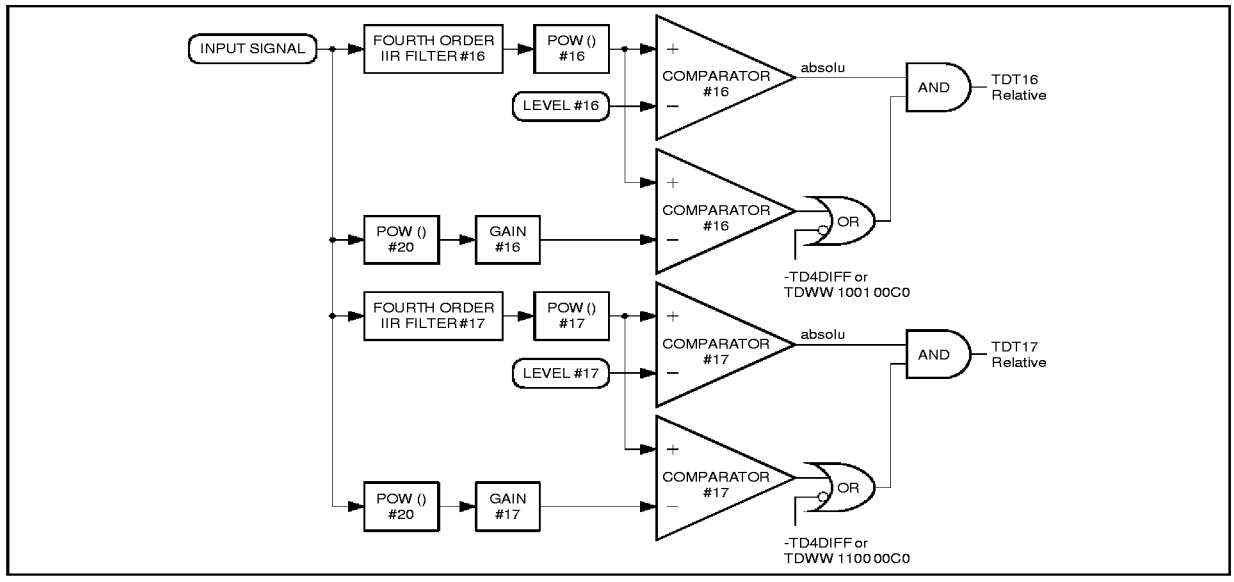
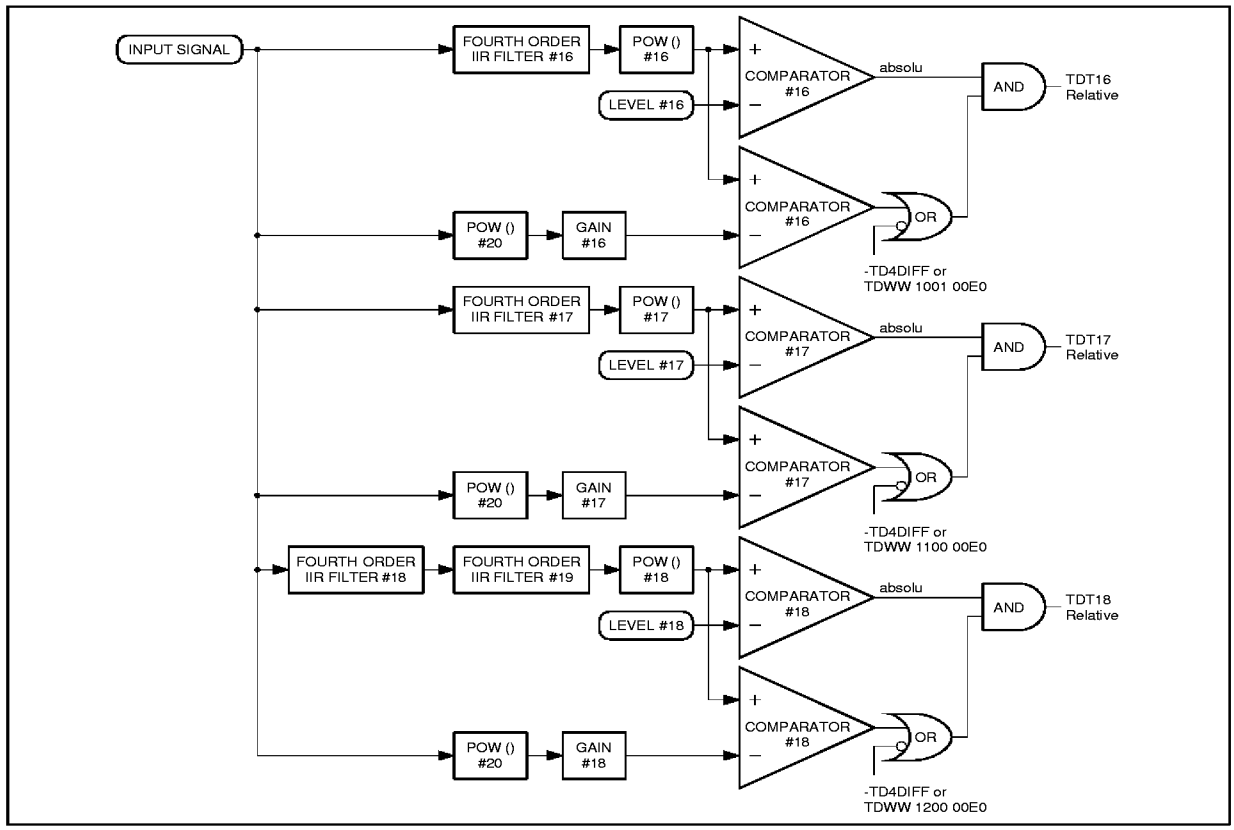
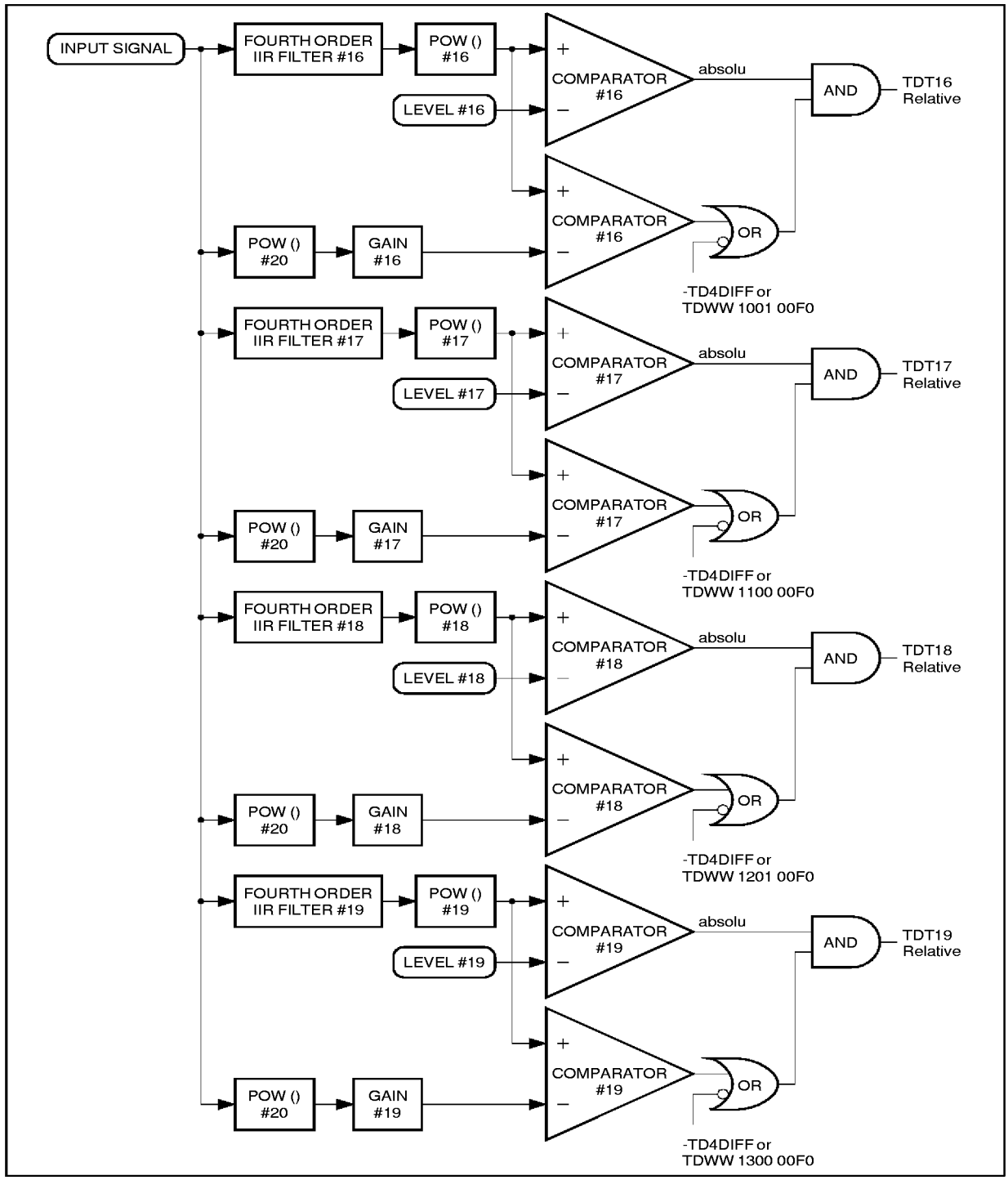


Figure 21b : Secondary Tone Detector Configuration (3 tone detectors 1 + 1 + 2)



VIII - TONE DETECTORS (continued)

Figure 21c : Secondary Tone Detector Configuration (4 tone detectors 1 + 1 + 1 + 1)



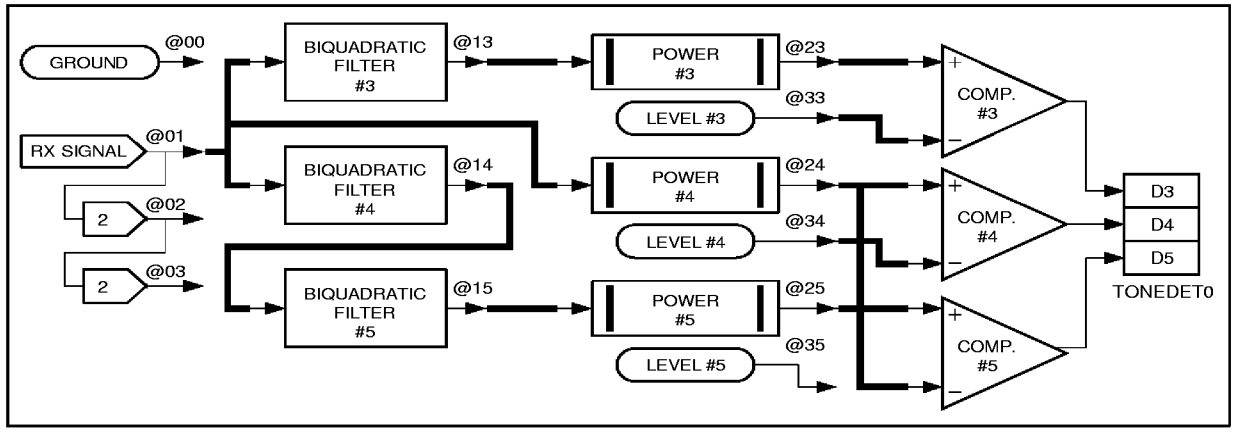
VIII - TONE DETECTORS (continued)

VIII.3 - Example

Hereunder is an example of programming a single Tone detection (using Cell #3) and a complex differential tone detection (using Cell #4 and #5).
Bit 3 of the TONEDET variable will be triggered each time the energy of that filtered signal is higher than Static Level number 3.

Bit 4 of the TONEDET variable will be on each time a receive signal has an energy higher than the Static Level number 4. Bit 5 will be on only when the Filtered (Filter section 4 and 5) received signal higher than the energy of the wide-band signal number 4 ; this prevents triggering on noise.

Figure 22 : Wiring Example



Program Cell #3 :

TDWW	**03**	**00**	**13**	**01**

Connect Received signal to Filter and Filter to Energy.

TDWW	**03**	**01**	**33**	**23**

Connect Level to Comparator Neg Input and Energy to Pos Input.

Program Cell #4 and #5 :

TDWW	**04**	**00**	**01**	**01**

Connect Received Signal to Filter and Energy.

TDWW	**04**	**01**	**34**	**24**

Connect Level to Comparator Neg Input and Energy to Pos Input.

TDWW	**05**	**00**	**15**	**14**

Connect Filter#4 Output to Filter and Filter to Energy.

TDWW	**05**	**01**	**24**	**25**

Connect Wide-band Energy to Neg Input and Energy to Pos Input.

IX - PARALLEL DATA EXCHANGE

IX.1 - Overview

While transmiting (respectively receiving) data to (from) the telephone line data are exchanged between the host and the ST75C540.

Two totaly independent channels are provived for transmit and receive data. Even while using half duplex modes of operation, the transmitted data comes from the transmit buffers and the receive data arrives in the receive buffers.

Two independent interrupts, ***IT2*** (for transmit) and ***IT3*** (for receive) are available for synchronizing the ST75C540 and the host. An additional ***IT0*** interrupt will signal the errors in the synchronization mechanism.

The equivalent data flow is as follows (see Figure 20).

The ST75C540 has a buit-in HDLC capability. This feature automatically performs HDLC framing/deframing, CRC generation/detection and "0" insertion/deletion. The ST75C540 have also UART capability, the format of data is selected by the ***FORM*** command described bellow.

IX.2 - Transmit Buffers

Two identical buffers are provided to exchange the data between the host interface and the ST75C540. When the host is writing data into a buffer, the ST75C540 is transmitting the other one. After that, both the host and the ST75C540 switch to use the other buffer. This mechanism, called "Double-Buffering", ensures that the host has the maximum time to fill one buffer.

The DUAL Ram area associated with the transmit buffers is as following table.

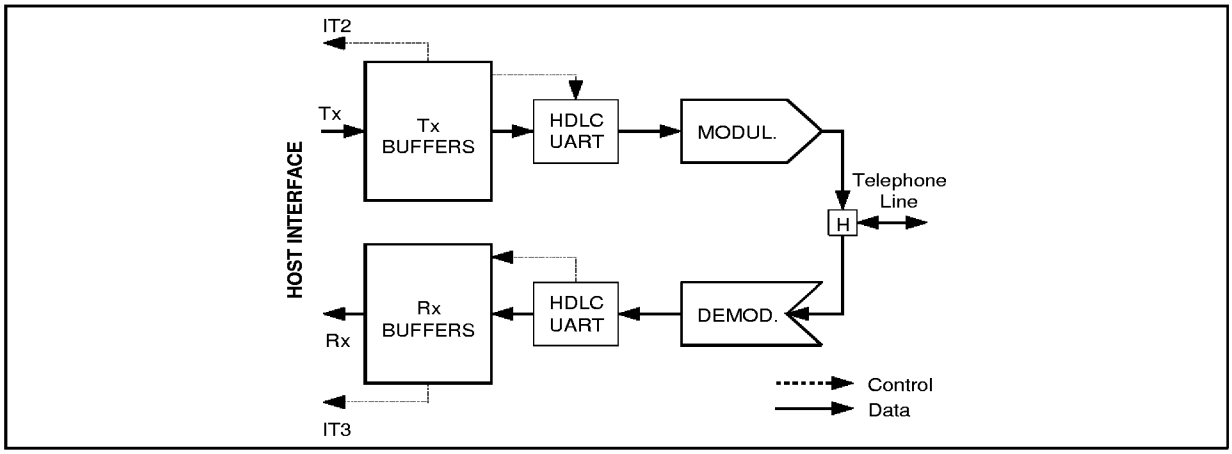
Name	Address	Description
DTTBS0	$2E	Buffer 0 Status Byte
DTTBS0 [0]	$2F	Buffer 0 Data Byte 0
DTTBS0 [1]	$30	Buffer 0 Data Byte 1
DTTBS0 [2]	$31	Buffer 0 Data Byte 2
DTTBS0 [3]	$32	Buffer 0 Data Byte 3
DTTBS0 [4]	$33	Buffer 0 Data Byte 4
DTTBS0 [5]	$34	Buffer 0 Data Byte 5
DTTBS0 [6]	$35	Buffer 0 Data Byte 6
DTTBS0 [7]	$36	Buffer 0 Data Byte 7
DTTBS1	$37	Buffer 1 Status Byte
DTTBS1 [0]	$38	Buffer 1 Data Byte 0
DTTBS1 [1]	$39	Buffer 1 Data Byte 1
DTTBS1 [2]	$3A	Buffer 1 Data Byte 2
DTTBS1 [3]	$3B	Buffer 1 Data Byte 3
DTTBS1 [4]	$3C	Buffer 1 Data Byte 4
DTTBS1 [5]	$3D	Buffer 1 Data Byte 5
DTTBS1 [6]	$3E	Buffer 1 Data Byte 6
DTTBS1 [7]	$3F	Buffer 1 Data Byte 7

Bit 0 (LSB) of the Buffer 0 Data Byte 0 is the first in time to be transmited.

According to the Data Format, the Status byte of a buffer has different meanings. However a value of 0 signals to the host that a buffer is empty. This value is set by the ST75C540 each time it has emptied the buffer. After having used one buffer, the host must select the other buffer for the next operation. The host must start with the Buffer 0 as soon as the ***ST_106*** signal goes on and BEFORE the ***XMIT 1*** command is sent.

A mechanism of interruption (***IT2*** for Transmit) is associated with the data buffer managment. Each time a buffer is emptied by the ST75C540 it generates an interrupt.

Figure 23



IX - PARALLEL DATA EXCHANGE (continued)

IX.3 - Receive Buffers

Symetrically two identical buffers are provided to exchange receive data between the ST75C540 and the host processor. While the ST75C540 is filling one of the buffers with the receive bits, the host processor is reading the other buffer. As soon as the host has emptied a buffer it frees it by writing 0 in the buffer status byte.

The DUAL Ram area associated with the receive buffers is as following table.

Name	Address	Description
DTRBS0	$1C	Buffer 0 Status Byte
DTRBS0 [0]	$1D	Buffer 0 Data Byte 0
DTRBS0 [1]	$1E	Buffer 0 Data Byte 1
DTRBS0 [2]	$1F	Buffer 0 Data Byte 2
DTRBS0 [3]	$20	Buffer 0 Data Byte 3
DTRBS0 [4]	$21	Buffer 0 Data Byte 4
DTRBS0 [5]	$22	Buffer 0 Data Byte 5
DTRBS0 [6]	$23	Buffer 0 Data Byte 6
DTRBS0 [7]	$24	Buffer 0 Data Byte 7
DTRBS1	$25	Buffer 1 Status Byte
DTRBS1 [0]	$26	Buffer 1 Data Byte 0
DTRBS1 [1]	$27	Buffer 1 Data Byte 1
DTRBS1 [2]	$28	Buffer 1 Data Byte 2
DTRBS1 [3]	$29	Buffer 1 Data Byte 3
DTRBS1 [4]	$2A	Buffer 1 Data Byte 4
DTRBS1 [5]	$2B	Buffer 1 Data Byte 5
DTRBS1 [6]	$2C	Buffer 1 Data Byte 6
DTRBS1 [7]	$2D	Buffer 1 Data Byte 7

The Bit 0 (LSB) of the Buffer 0 Data Byte 0 is the first received bit in time (the oldest).

According to the Data Format, the Status byte of a buffer has different meaning. However a value of 0 signals to the ST75C540 that a buffer is empty. This value is set by the Host each time it has emptied the buffer. After having used one buffer, the host must select the other buffer for the next operation. The Host must start with the Buffer 0 as soon as the ***STA_109*** signal goes.

A mechanism of interruption (***IT3*** for Receive) is associated with the Data Buffer managment. Each time a buffer is filled by the ST75C540 it generates an interrupt.

IX.4 - Interruption

Two Interrupt signals are provided in order to synchronize the Data Buffer Exchanges. ***IT2*** is associated with the Transmit Buffer mechanism and ***IT3*** with the Receive Buffer mechanism.

In order to enable these interrupts, the Host processor must set the bit 2 (for ***IT2***) and the bit 3 (for ***IT3***) of the ***ITMASK*** Register to 1. It must also set the Bit 7 of the ***ITMASK*** register to 1 in order to globally enable all the selected sources of interruption.

When an Interrupt occurs (low level on ***SINTR*** pin) the user must read the ***ITSRCR*** Register to determine the source of the interrupt, either ***IT2*** for Tx (if the bit 2 is 1) or ***IT3*** for Rx (if the bit 3 is 1).

Once the Interrupt has been serviced, the host must acknowledge it by writing a $00 value into the register ***ITRES2*** for ***IT2***, or ***ITRES3*** for ***IT3***.

These registers have the following address :

Name	Address	Type	Description
ITRES2	$42	Write only	Clear IT2
ITRES3	$43	Write only	Clear IT3
ITMASK	$4F	Read/Write	Interrupt Mask
ITSRCR	$50	Read Only	Interrupt Source

Notes : 1. The ST75C540 does not check that the interrupt has been acknowledged.
2. Even if the Host does not use the interruption, the ST75C540 will set the bit 2 (for ***IT2***) and/or bit 3 (for ***IT3***) of the ***ITSRCR***.
3. The ST75C540 uses only the Data Buffer Status Bytes to detect Overrun or Underrun Error. These errors are reported into the ***SYSERR*** byte, and could generate an interrupt ***IT0***.

The equivalent schematic is : see Figure 21.

The interrupt mechanism assumes that the Host processor uses a Level sensitive interrupt (active low). The Flow chart of the Host interrupt service routine looks generaly like Figure 22.

IX.5 - Data Format

Different Formats of Data can be Transmitted/Received to/from the Telephone Line.
These Formats can be selected when entering the Data Mode by using the ***FORM*** command.
The Format of the Data can be changed, on the fly in the Data Mode during the same communication, by sending a different ***FORM*** command at any time.
Note that for Full Duplex operation the Data Format is the same for the transmitter and the receiver.

IX - PARALLEL DATA EXCHANGE (continued)

Figure 24

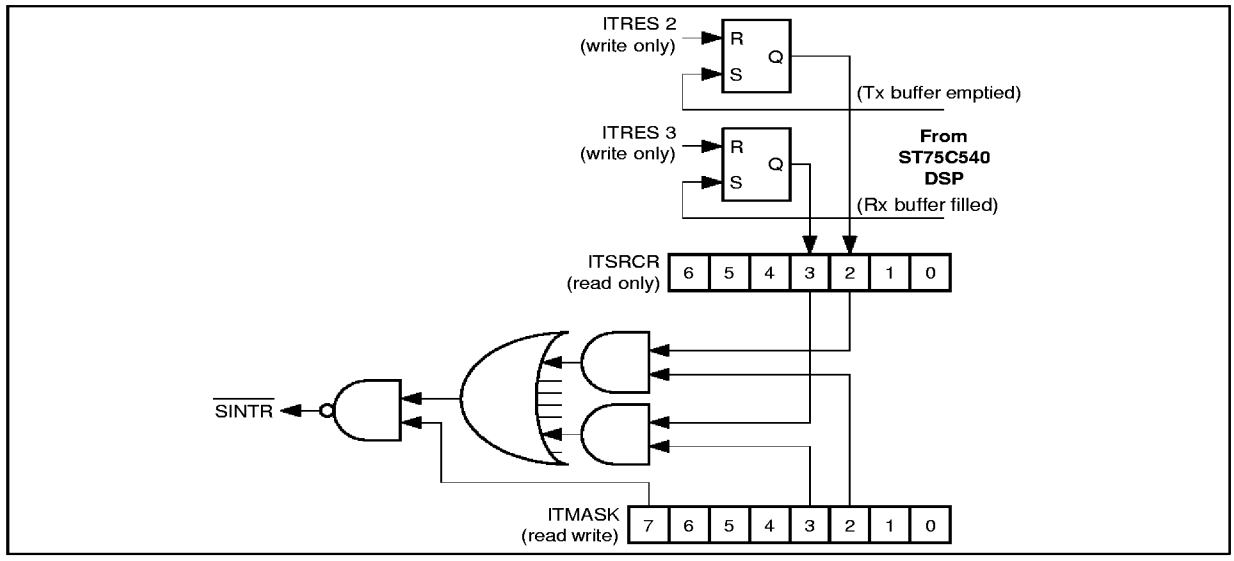
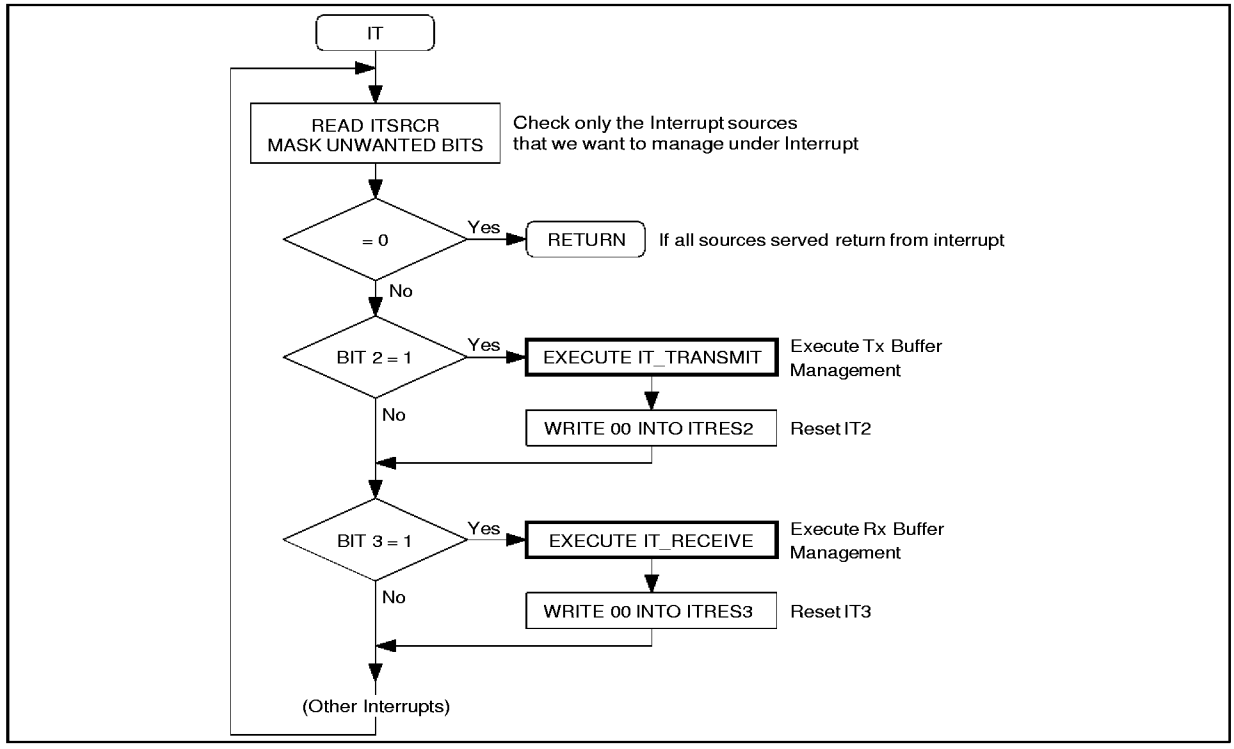


Figure 25



IX - PARALLEL DATA EXCHANGE (continued)

IX.6 - FORM Command

The ***FORM*** command allows the selection of the Data Format. The Parameter syntax is as follows :

Field	Byte	Pos.	Value	Definition
X_SYNC	1	2..0	000* 001 010 011 100	Synchronous format Transmit continuous "1"(1) HDLC framming Transmit continuous "0"(1) UART
X_ANBIT	2	1..0	00 01	7 Bit per character 8 Bit per character
X_APAR	2	3..2	00 01 10	No parity Even parity Odd parity
X_ASTOP	2	5	0 1	1 stop bit(1) 2 stop bit(1)

Note : 1. Transmit only

IX.6.1 - Synchronous Mode

The synchronous mode is the default mode, if no ***FORM*** command is used.
The transmitter reads the bits in the DUAL Ram Buffer ***DTTBFx*** (starting with the Bit 0 of Byte 0 of Buffer 0) and send them over the Telephone line. The Buffer Status Byte ***DTTBSx*** contains the number of Data Bytes to transmit.
The Receiver write the received bits coming from the Telephone line and write them into the DUAL Ram Buffer ***DTRBFx*** (starting with the Bit 0 of the Byte 0 of the Buffer 0). The Buffer Status Byte ***DTRBSx*** contains the number of Data Bytes received (generaly 8).

The time between each ***IT2*** interrupts (or ***IT3***) is equal to 64bit if the number of Data Bytes is set to 8. The Host has the full 64 bits time to serve the interrupt :

Bit Rate (bps)	Interrupt Time (ms)
14400	4.4
12000	5.3
9600	6.6
7200	8.8
4800	13.3
2400	26.6
1200	53.3
300	213.3
75	853.3

IX.6.2 - HDLC Mode

The HDLC Format can be used for T.30 or ECM implementations

IX.6.2.1 - HDLC Transmit

The HDLC Transmitter performs the following tasks :
- Flag generation (7E) while in inter-frame.
- Flag generation (7E) at the begining of a frame.
- Zero insertion (after 5 consecutive "1").
- CRC16 computation.
- CRC16 transmission at the end of a frame.
- Flag generation (7E) at the end of a frame.
- Abort frame.
- Programmable number of Starting flags.
- Programmable number of Inter frame flags.
- Programmable number of Ending flags.

The Buffer Status Byte ***DTTBSx*** defines the frame type, and the number of Data Bytes to transmit.

IX.6.2.2 - HDLC Receive

The HDLC Receiver performs the following tasks :
- Flag recognition.
- Opening flag recognition.
- Zero deletion.
- CRC16 computation.
- CRC16 check ; error CRC16 detection.
- Closing flag recognition.
- Abort frame detection.
- Received CRC.

The Buffer Status Byte ***DTRBSx*** contains the frame type, the number of Data Bytes and the error report if any. The errors detected are :
- CRC16 Error : Wrong CRC received.
- Non byte-alligned frame : The number of Data bits between the begining of the frame and the end of the frame (after "zero" deletion) is not a byte- multiple.
- Aborted frame : More that 6 consecutive "1" received.

IX.6.3 - UART Mode

In the UART mode the buffers contains only one Character to transmit or received. The worse case of interrupt rate is obtained with the lower character bit length (7bit of data, no parity and 1 stop bit) and is provided in the following table.

Bit Rate (bps)	Interrupt Time (ms)
14400	0.41
12000	0.41
9600	0.82
7200	1.25
4800	1.64
2400	3.75
1200	7.5
300	30
75	120

IX.6.3.1 - UART Transmit

The UART Transmitter performs the following tasks :
- Start bit generation.
- Parity Computation.
- Stop Bit generation.
- Break generation.

IX.6.3.2 - UART Receive

The UART Receiver performs the following tasks :
- Start bit recognition.
- Parity Checking.
- Stop bit Checking.
- Break detection.

X - TRANSMITTING DATA IN PARALLEL MODE

X.1 - Description

X.1.1 - XMIT Command

The ***XMIT*** Command works like a CTS signal for the Parallel Data process.
When ***XMIT*** is off, the ST75C540 transmits continuous "1". When on the ST75C540 transmits Data in accordance with the ***FORM*** command and starts to manage the Data Buffer.
This command can be sent at any time, while in Data Mode (see Table below).

X.1.2 - FORM Command

The ***FORM*** Command can be sent at any time to redefine the current format. The effect will take place only when ***XMIT*** is on.
Here is a formal example showing the relationship between ***XMIT***, and ***FORM*** Commands (see Figure 26).

X.1.3 - STOP Command

The ***STOP*** command is used, at the end of the transmission, to stop sending the carrier on the telephone line.
Prior to the ***STOP*** command the user must have stop the parallel transmition with a ***XMIT off*** command.
When the current data buffer will be totaly transmitted, and that no more buffers will be available, that is to said both ***DTTBF0*** and ***DTTBF1*** will be $00 (equivalent to an Underrun condition).

X.1.4 - Timing

Here are regular sequences to stop properly the transmition (see Figure 27).

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0 * 1	(Off) Send continuous "1" (**). (On) Send Data according with the Format defined in the ***FORM*** command.

** The ***XMITOff*** command takes effect only when the two Transmit buffers are empty : ***DTTBF0*** and ***DTTBF1*** equal to $00.

Figure 26

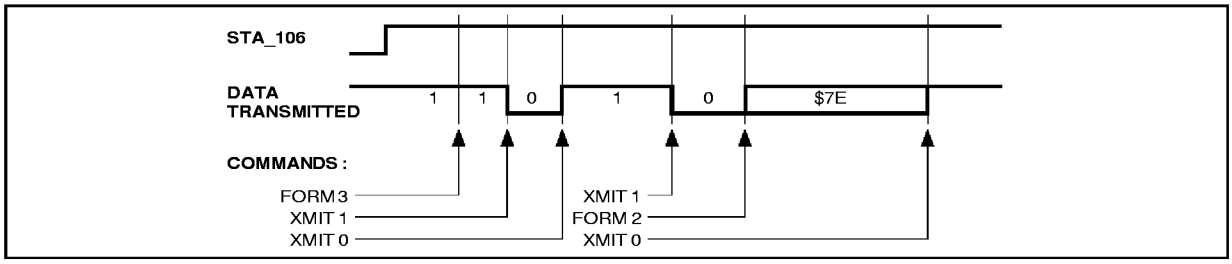
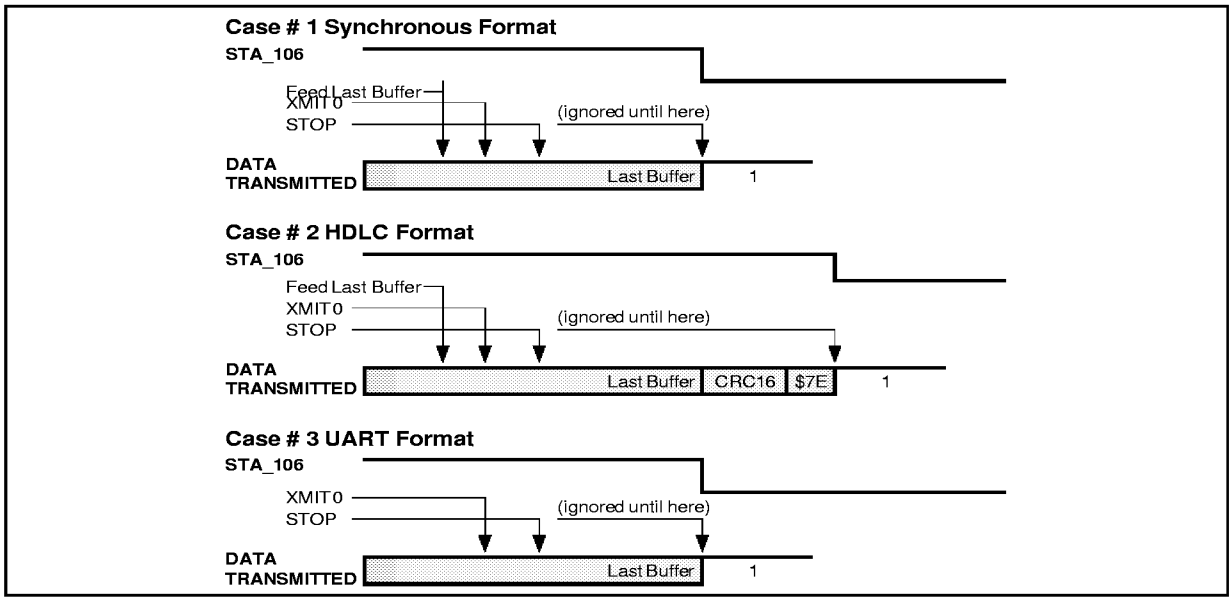


Figure 27



X - TRANSMITTING DATA IN PARALLEL MODE (continued)

X.1.5 - FSK Full Duplex Mode

In FSK Full duplex Mode the parallel mode assumes that the Bit time duration is the nominal Bit rate.

Each bit element from the Transmit buffer is maintained during the full bit time.

The Nominal bit clock is defined as follows :

FSK Standard	Nominal Transmit Bit Rate (Hz) (1)
V.21	300
Bell 103	300
V.23 Originate	75
V.23 Answer	1200

Note 1 : The accuracy of the Bit clock is given by the ST75C540 oscillator, and must better than 100ppm.

X.2 - Modem Flow Chart

When Data Mode, each time the ST75C540 need a bit to transmit it executes the following routine (see Figure 28). Where x starts with the value 0 and toggle thereafter between 1 and 0.

X.3 - Host Flow Chart

Here after are Flowcharts to :
- Establish a V.29 transmission
- Send Synchronous continuous "$AA, $55, $AA, $55, ..." sequence. The managment of the Buffers are done under Interrupt.
- Stop properly the transmition.

Establish a V.29 transmition and send the very first Buffer (see Figure 29).

Figure 28

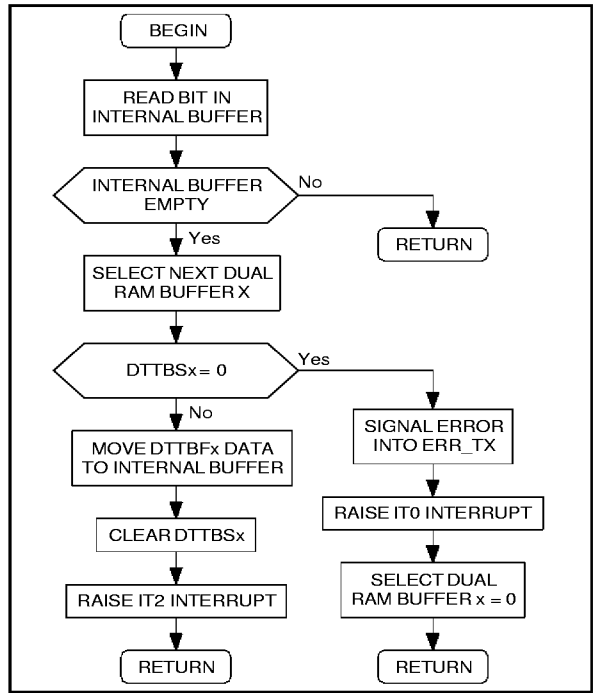
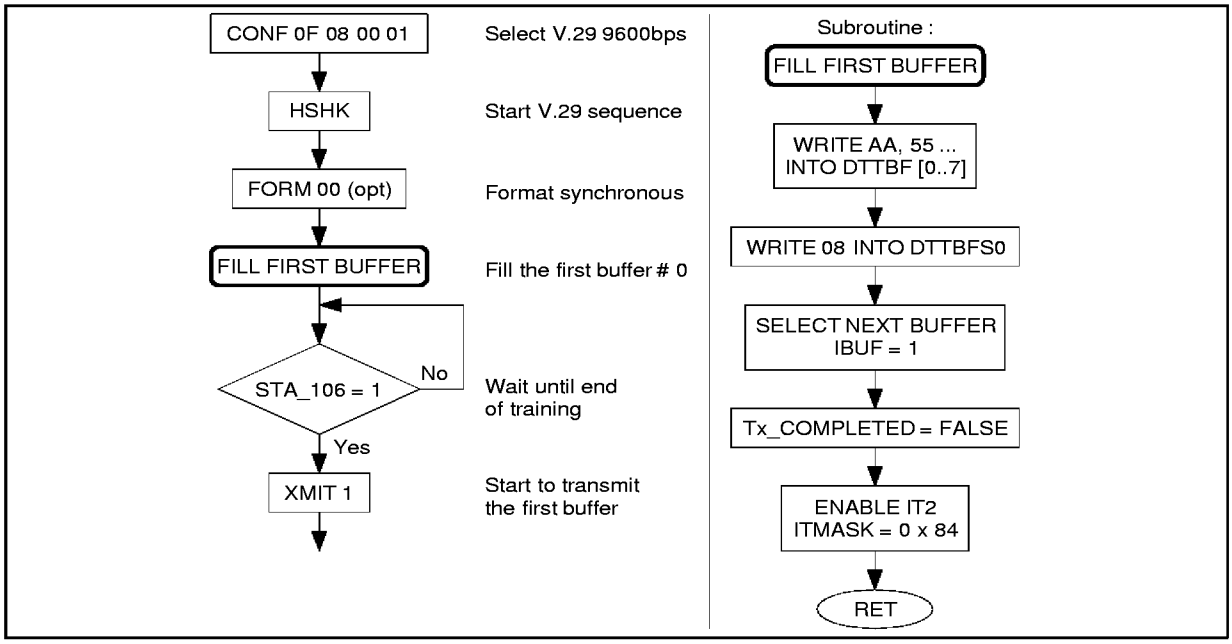


Figure 29



X - TRANSMITTING DATA IN PARALLEL MODE (continued)

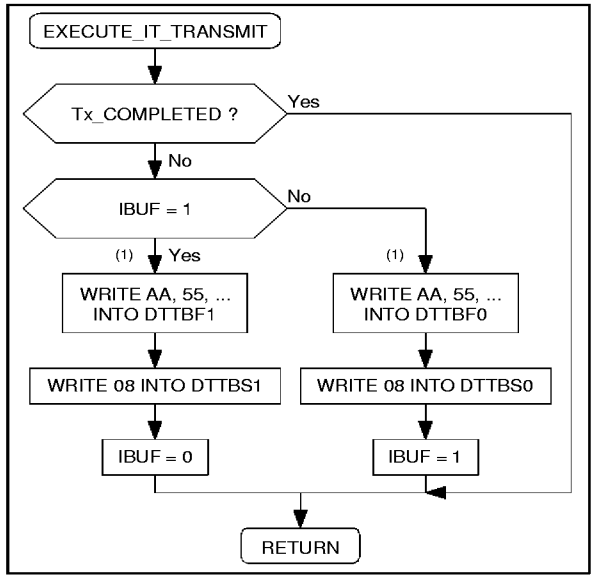
These flowcharts show two CPU variables labeled IBUF and Tx_Completed, they are necessary for the understanding of the mechanism, but there is different manners to implement it. These two variables have the following meanning :

- IBUF : This is the number of the DUAL RAM Buffer currently in use by the Host processor. It starts with 0 and then alternate 1, 0, 1, 0, ...
- Tx_Completed : This is a Flag to dialog with the interrupt process in order to stop properly the transmition.

The other Buffers are sent under interrupt control (refer to the interrupt flow chart, Figure 30).

To stop properly the transmition, without loss of Data (see Figure 31).

Figure 30



X.4 - Error Detection

Error occurs when the ST75C540 need some bits from the transmit buffer ***DTTBSx*** and this buffer is empty. This condition is called "Underflow".

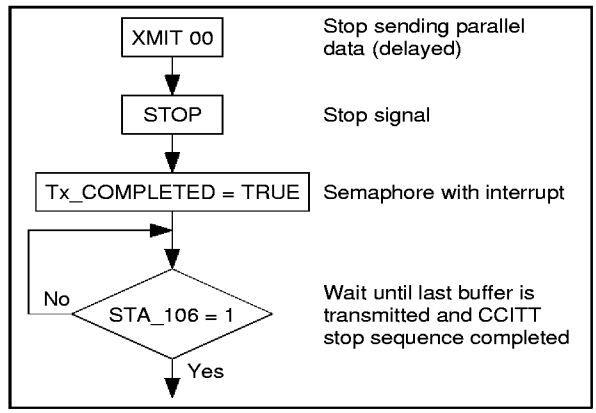
This error is signaled in the bit ***ERR_TX*** of the ***SYSERR*** byte, and generates an interrupt ***IT0***. To clear the error a ***CSE01*** command must be issued.

An Underflow contition occurs when :

- In synchronous mode: the host processor "forgets" to feed the current ***DTTBSx*** buffer.
- In HDLC mode: when, while inside a frame, the host processor "forgets" to feed the current ***DTTBSx*** buffer. An abort frame is transmitted in place of the regular Buffer.
- This condition cannot append in UART mode.

When an underflow condition occur the host must restart the whole parallel initialization, as explained above.

Figure 31



X.5 - Synchronous Mode

X.5.1 - Description

In synchronous mode the ST75C540 transmits the bits contained in the DUAL RAM Buffer without any modification. It starts with the Bit 0 of the ***DTTBF0[0]*** byte.

X.5.2 - Status Word Format

The Transmit Status Bytes ***DTTBS0*** or ***DTTBS1*** have the same following meaning (see table below).

DTTBSx in Synchronous Mode			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0	Buffer empty.
		1	1 Byte to transmit (***DTTBFx[0]***).
		2	2 Bytes to transmit (***DTTBFx[0]*** and ***DTTBFx[1]***).
		..	..
		8	8 Bytes to transmit (***DTTBFx[0 .. 7]***).
		Other	Not allowed.
Other	7 .. 4	0	Reserved, must be 0.

This status byte must be written by the Host, after filing the corresponding data buffer ***DTTBFx[0..7]*** with the right number of data bytes to transmit.

This status byte is cleared by the ST75C540, just before generating the ***IT2*** interrupt.

X - TRANSMITTING DATA IN PARALLEL MODE (continued)

X.6 - HDLC Mode

X.6.1 - Description

In HDLC mode the ST75C540 transmits the data bytes contained into the DUAL Ram buffer packed inside an HDLC frame. The mechanism is as follows :

- While the Host has no frame to transmit, that is: as long as ***DTTBSx*** equals $00, the ST75C540 transmits the HDLC Flag $7E.
- When the Host wants to send some data, it feeds the buffer with some data bytes to transmit (between 1 and 8) and set the ***BUFF_SFRM*** bit in the ***DTTBSx*** status buffer. At that time the ST75C540 start sending data contained in the Buffer, computin the CRC and performing "zero intertion" if needed.
- When the host wants to send additional data (within the same frame) it feeds the buffers just like in synchronous mode. If an Underflow condition occurs, the ST75C540 will abort the frame by sending 8 consecutive "1", and the Host must restart the whole parallel initialization.
- When the host wants to close a frame, it set the ***BUFF_EFRM*** bit in the ***DTTBSx*** status buffer. At that time the ST75C540 will send the contents of the buffer, then send the CRC and an HDLC closing flag $7E.
- If the Host, wants to abort a frame (while sending a frame) it set the ***BUFF_FRAB*** bit in the ***DTTBSx*** status buffer. At that time, as soon as the last buffer will be transmitted, the ST75C540 will send 8 consecutive "1" and wait for the next buffer.

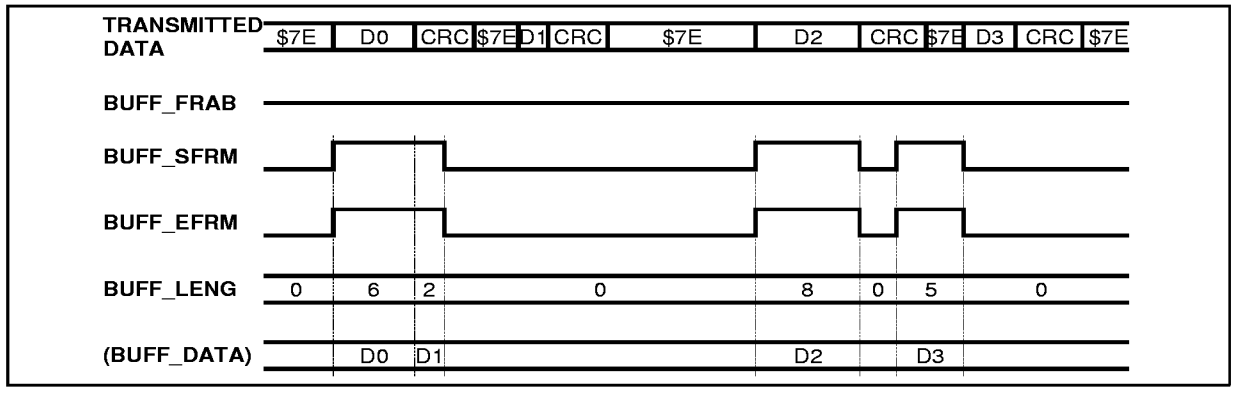
X.6.2 - Status Word Format

DTTBSx in HDLC Mode			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 other	Buffer empty. 1 Byte to transmit (***DTTBFx[0]***). 2 Bytes to transmit (***DTTBFx[0]*** and ***DTTBFx[1]***). .. 8 Bytes to transmit (***DTTBFx[0 .. 7]***). Not allowed.
BUFF_SFRM	4	0 1	Data stream. Start of frame : the buffer is a beginning of frame.
BUFF_EFRM	5	0 1	Data stream. End of frame : the buffer will be followed by the transmission of the CRC and closing flag.
BUFF_FRAB	6	0 1	Data stream. Abort frame : 8 consecutive "1" will be transmitted (whatever ***BUFF_LENG*** is).
Other	7	0	Reserved, must be 0.

Notes : 1. A buffer can have ***BUFF_SFRM*** and ***BUFF_EFRM*** set in the same ***DTTBSx*** byte, this means that the frame transmitted is short (between 1 and 8 Bytes long).
2. An ending frame (with ***BUFF_EFRM*** set) must have at least ONE byte of data to transmit.

X.6.3 - Single Short Frame (see Figure 32)

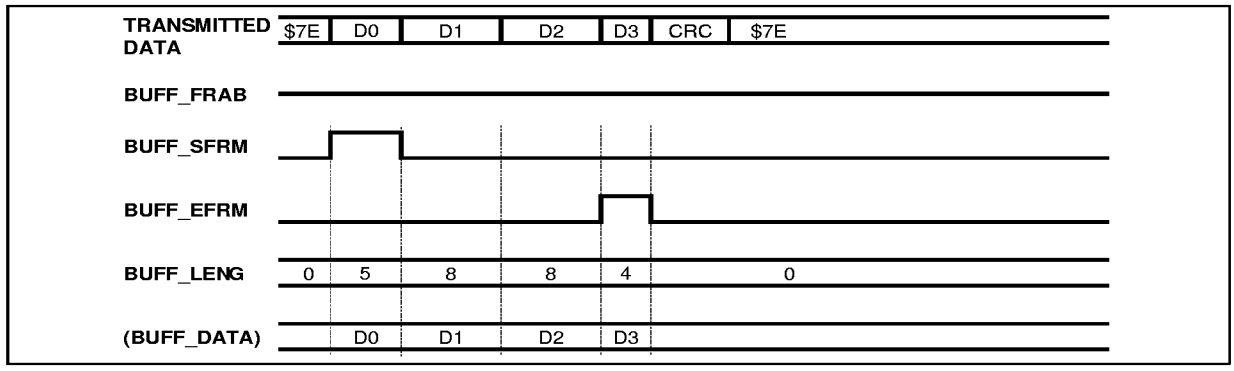
Figure 32



X - TRANSMITTING DATA IN PARALLEL MODE (continued)

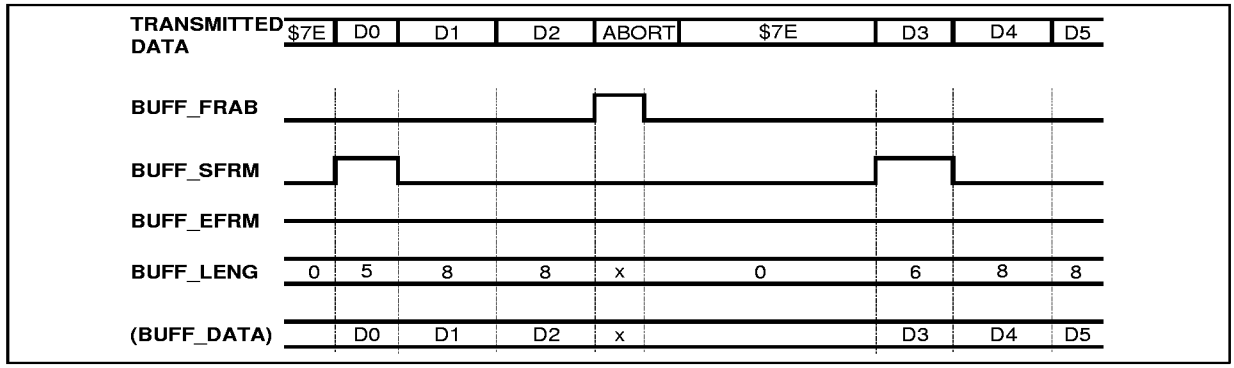
X.6.4 - Long Frame

Figure 33



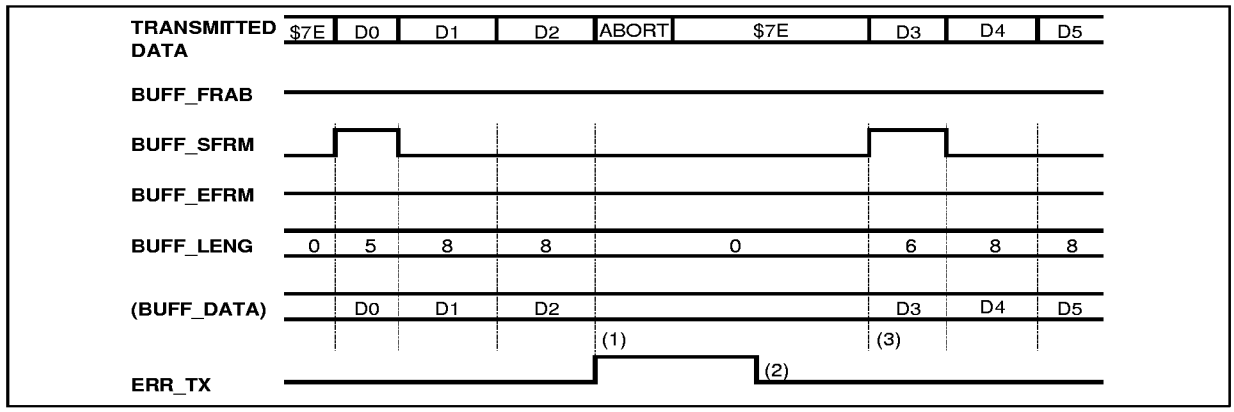
X.6.5 - Abort Frame

Figure 34



X.6.6 - Abort Due to Underflow

Figure 35

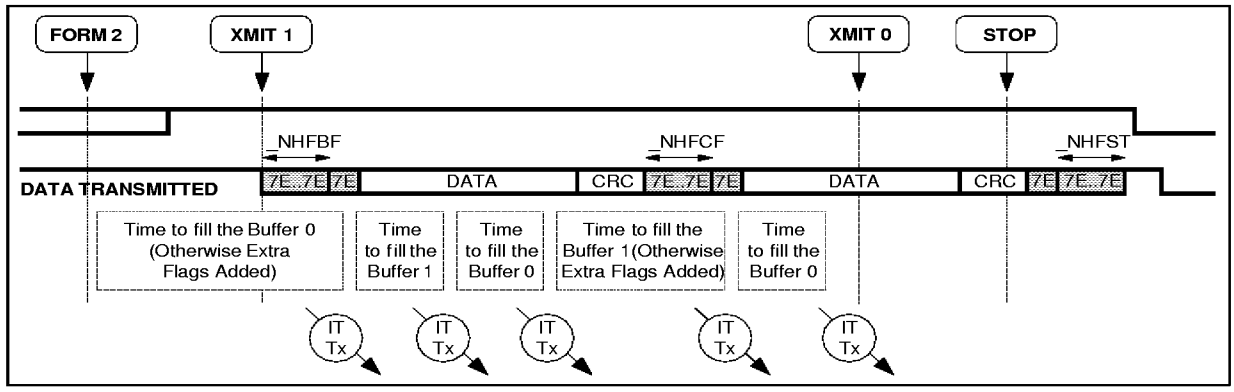


Where : 1. The Underflow condition appears when the ST75C540 needs, inside a frame, some bytes to transmit and that the corresponding buffer is empty.
2. The ***ERR_TX*** bit is cleared with a ***CSE 01*** Command.
3. After an Underflow condition restart the initialization of the parallel mode and use the buffer number 0.

X - TRANSMITTING DATA IN PARALLEL MODE (continued)

X.6.7 - HDLC Special Timming

Figure 36



A set of global variables allows the programmation of the number of flags (7E) generated by the ST75C540 :

- _NHFBF : Number of flags before the first frame.
- _NHFCF : Number of flags between frames.
- _NHFST : Number of flags after the last frame.

The default value for all these variables is 0, the programming range is from 0 to 7FFF (32767). These varaibales must be modified with a MW or MWI command (see Figure 36).

X.7 - UART Mode Description

In UART mode the ST75C540 transmits the data Character contained into the DUAL Ram buffe. The mechanism is as follows :

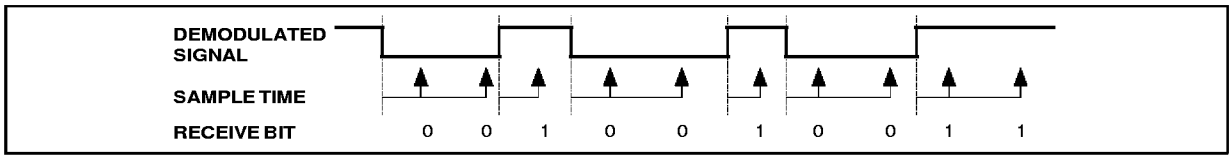
- While the Host has no character to transmit, that is: as long as ***DTTBSx*** equals $00, the ST75C540 transmits continuous "1".
- When the Host wants to send a chacarter, it feeds the buffer with the character to transmit.
- The ST75C540 start to send a stop bit ("0") then the character contained in the Buffer, computing the parity. It send the parity bit, if needed, and the stop bits (1 or 2 according with the ***FORM*** command).
- If the user wants to send a break signal, he has to set the ***BUFF_UBRK*** bit within the corresponding Status Word (***DTTBSx***). A break signal is defined as a totaly null character with all stop bits duration maintained to "0" (e.g: if format is 7 bit, even parity and 2 stop bit, break is a "0" durring 10 bit). Multiple continuous breaks ("0" continuous signal) can be send by using consecutive buffers with ***BUFF_UBRK*** set to 1.

X.7.1 - Status Word Format

DTTBSx **in UART Mode**			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 other	Buffer empty. 1 character to transmit (***DTTBFx[0]***). Not allowed.
BUFF_UBRK	6	0 1	Normal character. Break signal : a complete "0" character with all stop bits equal to "0".
Other	7	0	Reserved, must be 0.

XI - RECEIVING IN PARALLEL MODE

Figure 37



XI.1 - Description

When the STA_109 (CD) signal goes on, the ST75C540 will write received data into the DUAL RAM buffer DTRBS0 at first.

XI.1.1 - Initialization

The host processor must enable the IT3 receive interrupt first.

Then it must empty the two DTRBS0 and DTRBS1 registers by writting $00 at these locations.

As soon as the first IT3 interrupt appears, the host must proceed with the DTRBS0 buffer.

XI.1.2 - Loss of Carrier

Each time a loss of carrier appears the ST75C540 stops updating the Data buffer. If the carrier reappers the host must proceed again with the initialisation sequence.

XI.1.3 - FSK Synchronization

The FSK Full Duplex demodulator uses an algorithm based on the transitions of the received signal. The synchronization mechanism is adjusted with each signal transiton in order to sample the demodulated signal at the middle of the bit (see Figure 37).

XI.2 - Modem Flow Chart

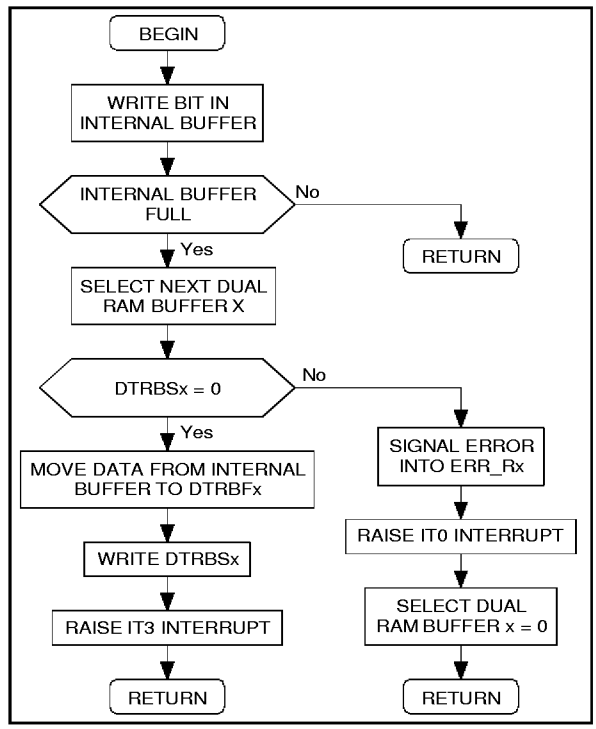
When in parallel data mode, each time the ST75C540 has receive some bit of data it executes the following routine (see Figure 38).

Where x start with the value 0 and toggle between 1 and 0.

XI.3 - Host Flow Chart

Hereafter are flowcharts to :
- Establish a V.29 reception.
- Receive synchronous data. This task is performed under interrupt.
- Handle properly some temporary loss of carrier.

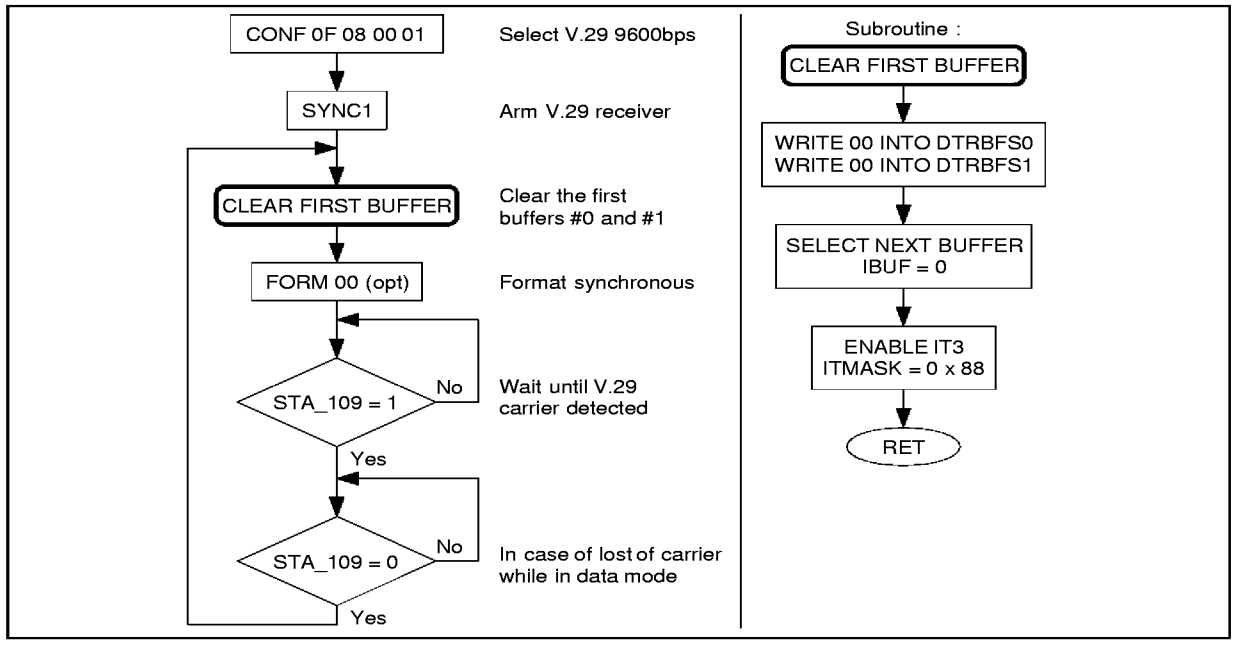
Figure 38



XI - RECEIVING IN PARALLEL MODE (continued)

Establish the reception (see Figure 39).

Figure 39

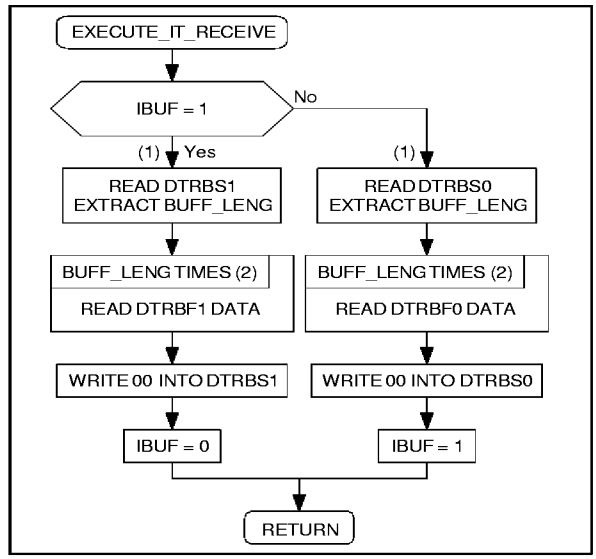


These flowcharts show one CPU variable labeled IBUF which is necessary for the understanding of the mechanism, but there are different manners to implement it.

- IBUF : this is the number of the DUAL RAM buffer currently in use by the Host processor. It starts wit 0 an then alternates 1, 0, 1, 0, ...

The received bits are read by an interrupt routine (See Figure 40).

Figure 40



Notes : 1. At that step the host can check that the corresponding ***DTRBSx*** buffer is full (different from $00), otherwise it is an error.

2. This means read ***BUFF_LENG*** bytes, inside the Receive buffer ***DTRBFx*** starting from location ***DTRBFx[0]*** to ***DTRBFx[BUFF_LENG - 1]***. In synchronous mode, the ***BUFF_LENG*** is always 8 bytes, except when a ***STA_109*** lost appears in the middle of the buffer.

XI.4 - Error Detection

Error occurs when the ST75C540 has received some bits and that the buffer ***DTRBSx*** is not empty, this condition is called “Overflow”.

This error is signaled in the bit ***ERR_RX*** of the ***SYSERR*** byte, and generates an interrupt ***IT0***. To clear the error a ***CSE 02*** command must be issued.

An Overflow condition occurs when :

- In synchronous mode: the host processor “forgets” to empty the current ***DTRBSx*** buffer.
- In HDLC mode: when, while inside a frame, the host processors “forgets” to empty the current ***DTRBSx*** buffer.
- In UART mode, this cannot happen.

When an Overflow condition occurs the host must restart the whole parallel initialisation.

XI - RECEIVING IN PARALLEL MODE (continued)

XI.5 - Synchronous Mode

XI.5.1 - Description

In synchronous mode the ST75C540 writes the received bit into the DUAL RAM Buffer without any modification. It starts with the Bit 0 of the ***DTRBF0[0]*** byte.

XI.5.2 - Status Word Format

The receive Status Byte ***DTRBS0*** or ***DTRBS1*** have the same following meaning (See Table below).

The BUFF_LENG is always 8 except when a lost of carrier (***STA_109*** going to 0) happens.

This status byte is set by the ST75C540, just before generating the ***IT3*** interrupt.

XI.6 - HDLC Mode

XI.6.1 - Description

In HDLC mode the ST75C540 extracts from the received HDLC frame the Data information only. It reports, trough the DUAL Ram buffer, only data information and frame validity. The mechanism is as follows :

- As long as the ST75C540 receives continuous HDLC Flag $7E, nothing happens. Note that the ST75C540 allows zero sharing between adjacent flags.
- When the ST75C540 receives some data, it removes inserted "zero" if needed, and starts to compute the CRC. As soon as its internal buffer is full, the ST75C540 writes the received data into the ***DTRBFx*** buffer and sets the ***BUFF_SFRM*** inside the ***DTRBSx*** status byte.
- When receiving additional data, the ST75C540 feeds the buffer just like in synchronous mode.
- When the ST75C540 receives a closing flag (which can be shared with the following opening flag) it compares the received CRC with its internal computation. It writes the contents of the received last data into the ***DTRBFx*** buffer, sets the ***BUFF_EFRM*** bit and reports any frame error in the ***DTRBSx*** register via the ***BUFF_ERRS*** bits. Reported errors are :
  - CRC error (lowest priority): the received CRC is not equal to the computed CRC. Some bits, inside the frame, are erroneous.
  - Non Byte-Aligned frame (middle priority): the received data bit count (after deletion of the "zero inserted"), between the opening and the closing flag, is not a multiple of 8.
  - Aborted frame (highest priority): the frame was aborted with at least 7 consecutive "1"
- An abort frame can be also detected, while in the inter frame mode, if instead of receiving $7E flag, the ST75C540 receive more than 7 consecutive "1". In this case only one Aborted frame is signaled, event if the "1" condition is maintained.

DTRBSx in Synchronous Mode			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 Other	Buffer empty. 1 Byte received (***DTRBFx[0]***). 2 Bytes received (***DTRBFx[0]*** and ***DTRBFx[1]***). .. 8 Bytes received (***DTRBFx[0 .. 7]***). Not used.
Other	7 .. 4	0	Not used.

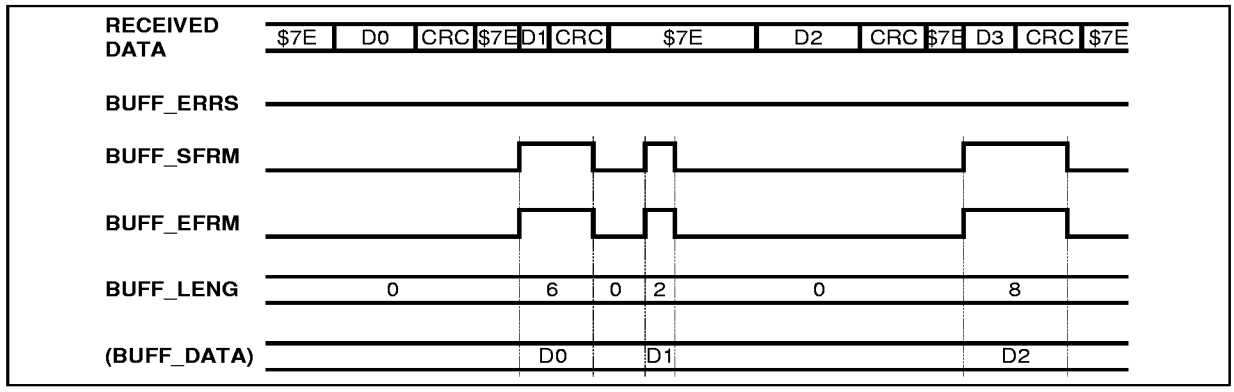
XI.6.2 - Status Word Format

DTRBSx in HDLC Mode			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 other	Buffer empty. 1 Byte received (***DTRBFx[0]***). 2 Bytes received (***DTRBFx[0]*** and ***DTRBFx[1]***). .. 8 Bytes received (***DTRBFx[0 .. 7]***). Not allowed.
BUFF_ERRS	5 .. 4	0 0 0 1 1 0 1 1	No error. CRC error. Non Byte-Aligned frame. Aborted frame.
BUFF_SFRM	6	0 1	Data stream. Start of frame : the buffer is a beginning of frame.
BUFF_EFRM	7	0 1	Data stream. End of frame : the buffer is a closing frame.

XI - RECEIVING IN PARALLEL MODE (continued)

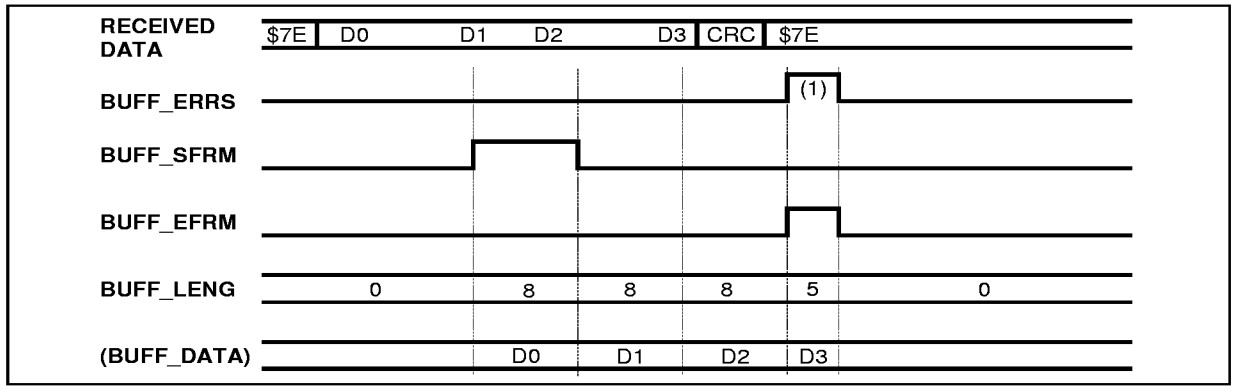
XI.6.3 - Single Short frame

Figure 41



XI.6.4 - Long Frame

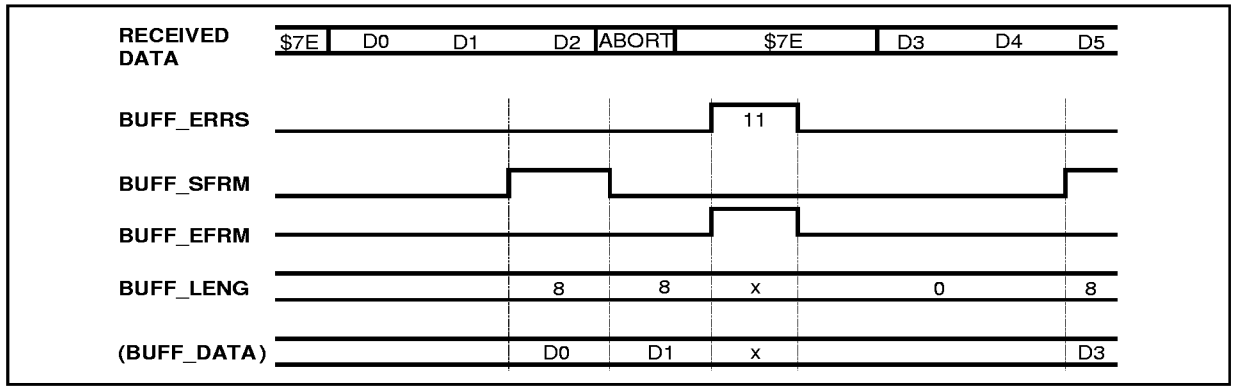
Figure 42



Note : 1. If error occurs during the reception, it is signaled in this last buffer.

XI.6.5 - Aborted Frame

Figure 43



XI - RECEIVING IN PARALLEL MODE (continued)

XI.7 - UART Mode

XI.7.1 - Description

In UART mode the ST75C540 extracts from the received Characters the Data information only. It reports, trough the DUAL Ram buffer, only data information character validity. The mechanism is as follows :

- As long as the ST75C540 receives continuous "1" nothing happens.
- When the ST75C540 receives the start bit ("0") it starts to compute the parity. As soon as the number of data bit (defined by the FORM command) is received, the ST75C540 writes the received character into the DTRBFx buffer and update the receive Status word DTRBSx.
- The Reported errors are :
  - Parity error (lowest priority): the received parity is not equal to the computed parity. Some bits, inside the character, are erroneous.
  - Stop bit error (middle priority): the bit after the parity was not a stop bit ("1"). Note that if the two stop bit format was selected, only the first stop bit will be checked.
  - Break Detection (highest priority): the character is a break signal as defined in the transmit section. If the duration of the break is longer than one character, only one break buffer will be reported.

XI.7.2 - Status Word Format

DTRBSx in UART Mode			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 Other	Buffer empty. 1 character received (DTRBFx[0]). Not allowed.
BUFF_ERRS	5..4	00 01 10 11	No error. Parity error Stop bit error Break signal detected

XII - VOCODER DATA EXCHANGE

XII.1 - Overview

The ST75C540 can receive (or transmit) coded voice from (to) the telephone line or the audio interface. The receiving mode is the CODER mode while the transmit is the DECODER mode.
Two formats of Voice compression are provided: Low bit rate and ADPCM. In all the formats and speed the management of the Coded Voice is exactly the same. In any format a frame of all data equal to zero will be synthesised (DECODER) as a frame of silence.

XII.2 - Vocoder Buffer

A buffer area is reserved in the DUAL ram to exchange Voice between the ST75C540 and the Host processor. This area is used either for recording (CODER) or playing back (DECODER) the voice signal.

The DUAL Ram area associated with the VOCODER is as follows :

Name	Address	Description
VOCSTA	$1C	Vocoder Buffer Status
VOCDATA	$1D..$2E	Vocoder Buffer Data
VOCCORR	$2F..$30	Vocoder Buffer Corrector

The IT1 interrupt signal is dedicated to the Vocoder Buffer Management.

XII.3 - Transmit (DECODER)

This mode is entered with the CONF DECODER command.

If the ADPCM or Low bit rate without error correction mode (CONF_ERCOR = 0) are selected, the user needs to feed the vocoder buffer with 18 bytes of voice data, then set the VOCSTA byte with a value different from zero.

In the low bit rate with error mode (CONF_ERCOR = 1), the user needs to feed the vocoder buffer with 20 bytes of voice data, then set the VOCSTA byte with a value different from zero.

Once the ST75C540 have read the buffer, it clears the VOCSTA byte and raise the IT1 interrupt. The IT1 interrupt rate is as follows :

Mode	Interrupt Time (ms)	Number of Voice Samples in the Buffer (8kHz sampling)
ADPCM 32Kpbs	4.5	36
ADPCM 24Kpbs	6	48
ADPCM 16Kpbs	9	72
Low Bit Rate Nominal (with and without error correction)	30	240
Low Bit Rate Fast/Slow Playback	Depends on speed 15 to 45	Depends on speed 120 to 360
Low Bit Rate Pause	0	-

A silence can be generated by writing zero to all the VOCDATA bytes (and VOCCORR bytes if CONF_ERCOR = 1). The duration of the silence will be the same as the other frames of signal.

As the buffer contains always a complete number of samples representing the same duration, it is easy to randomly advance forward/backward in a message.

If the user does not feed the Buffer within the Interrupt time, the ST75C540 will signal this error by rising the ERR_VOCO in the SYSERR byte and rising the IT0 Interrupt. In this case the previous frame will be re-transmited.

XII - VOCODER DATA EXCHANGE (continued)

XII.4 - Receive (CODER)

This function can be entered either by :

- The CONF CODER Command. This corresponds to the "Normal Answering Machine" function.
- The MODC Command with MODC_COD = 1, in the HANDSET Mode. This corresponds, in the HANDSET mode to the "Conversation Recording" function. This reduced sub-mode does not allow ADPCM format and does not perform VAD (Voice Activity Detector).

Once this function is selected, the ST75C540 starts to code the voice signal, writes one frame of compressed voice into the VOCDATA bytes (if the low bit rate mode is selected, computes always the Corrector bytes and writes them in the VOCCORR bytes) then writes the VOCSTA byte and generates the IT1 interrupt. The IT1 interrupt rate is as follows :

Mode	Interrupt Time (ms)	Number of Voice Samples in the Buffer (8kHz sampling)
ADPCM 32Kpbs	4.5	36
ADPCM 24Kpbs	6	48
ADPCM 16Kpbs	9	72
Low Bit Rate (with and without error correction)	30	240

Note that the VOCCORR are always computed, whatever the value of CONF_ERCOR.

The format of the VOCSTA byte is as follows :

VOCSTAT				
Format	**Field**	**Pos.**	**Value**	**Definition**
Low Bit Rate	VOC_VAD	7	0 1	VAD Unvoiced Signal. VAD Voice Signal.
	VOC_NUM	4..0	10100	(20 decimal) Number of VOCDATA Bytes
ADPCM	VOC_VAD	7	0 1	VAD Unvoiced Signal. VAD Voice Signal.
	VOC_NUM	4..0	10010	(18 decimal) Number of VOCDATA Bytes

Note that in "Conversation recording" the VOCSTA byte is always $14.

The user must read the VOCDATA (and optionally the VOCCORR) bytes and clear the VOCSTA byte (writing $00).

If the user does not clear the VOCSTA byte within the interrupt time, the ST75C540 will signal this error by rising the ERR_VOCO in the SYSERR byte and rising the IT0 Interrupt. In this case the current frame is lost.

If the CONF_SUPSIL bit is 1 in the CONF CODER command, the interrupts IT1 appears only when

the VAD has detected a voiced signal.

Figure 44 : Call Progress Tone Detector Band 1

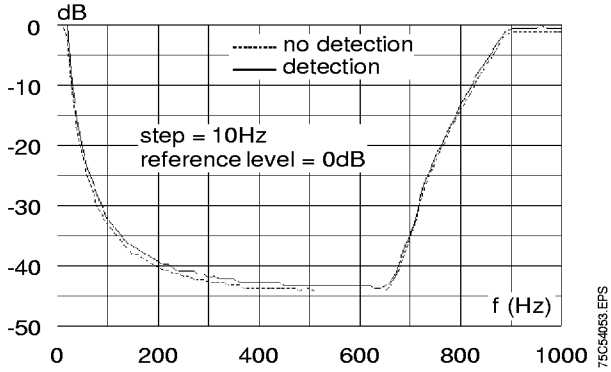
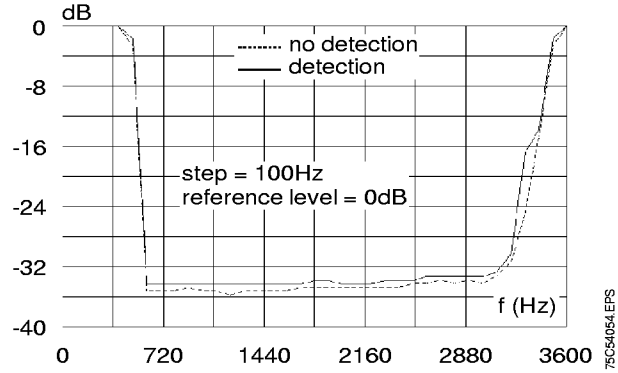


Figure 45 : Call Progress Tone Detector Band 2



XIII - DEFAULT CALL PROGRESS TONE DETECTORS

Figure 46 : 2100Hz Answer Tone Detector

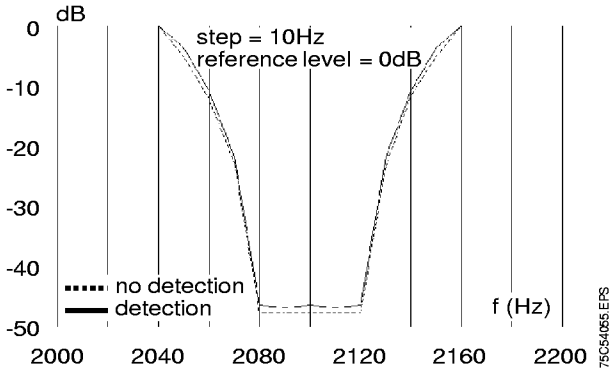
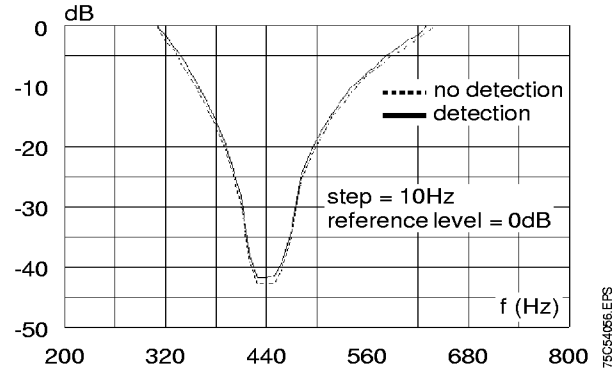
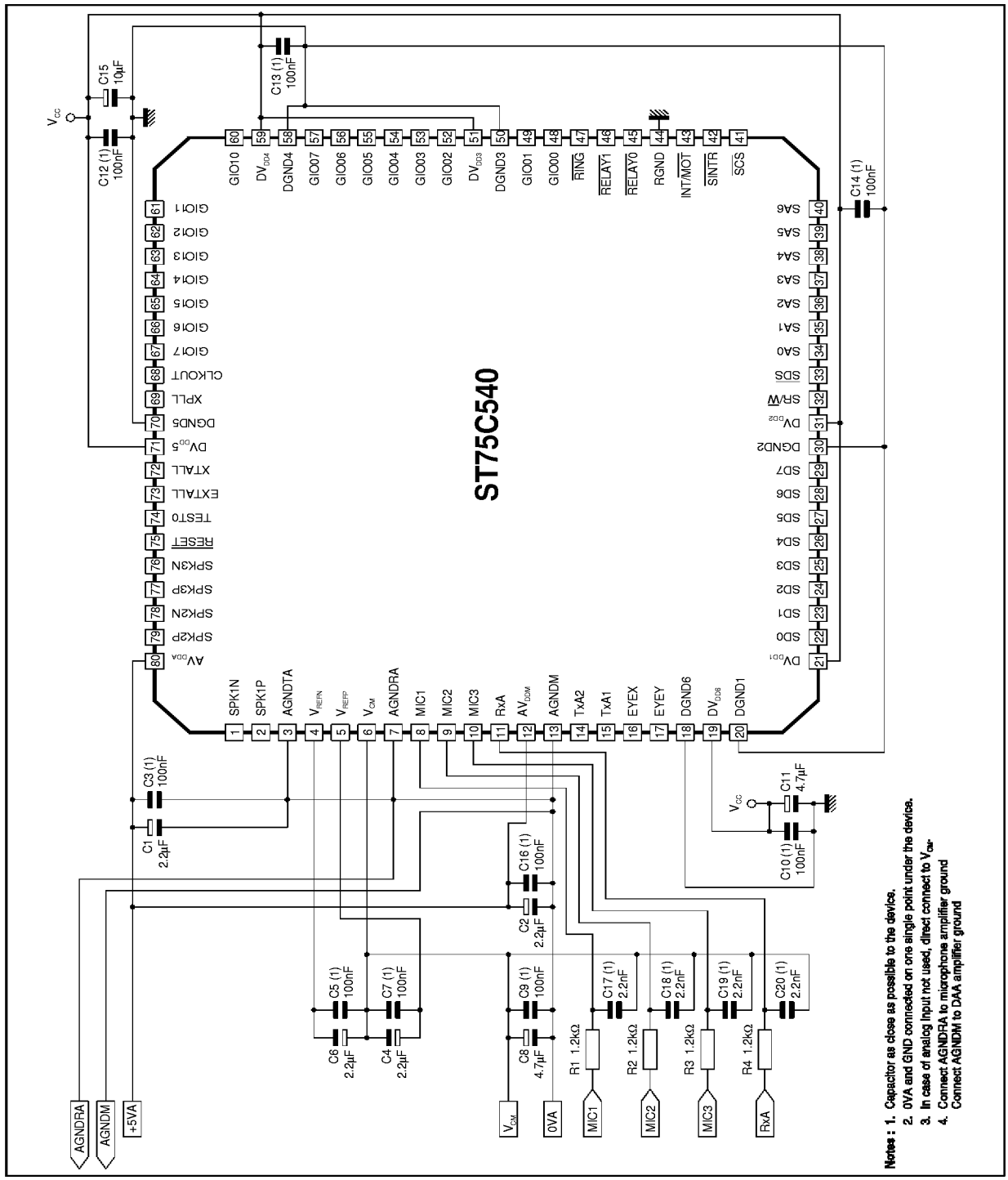


Figure 47 : 440Hz Tone Detector



XIV - DEFAULT ANSWER TONE DETECTORS

Figure 48



XV - ELECTRICAL SCHEMATICS

XVI - PCB DESIGN GUIDELINES

Performances of the FAX modem depends on the ST75C540 intrinsic performances and on the proper PC board layout. All aspects of the proper engineering practices, for PC board design, are beyond the scope of this paragraph.

We recommend the following points :

- in a 4-layer PC board : Separated digital ground and analog ground, connected together at one point, as close as possible to the ST75C540,
- in a 2-layer PC board : Provide a ground grid in all space around and under components on both sides of the band and connect to avoid small islands,
- both AGNDR and AGNDT must be connected with very low impedance to a single point, (see Chapter I.7, Power Supply),
- the four 2.2nF capacitors connected to the RXA and MIC1, MIC2, MIC3 Pins must be as close as possible to them,
- the two 100nF capacitors connected to the V_{REFP} and V_{REFN} pins must be as close as possible to them,
- analog and digital supplies must be connected together, at a single point, as close as possible to the chip.

Figure 49 : Tone Mode (TONE)

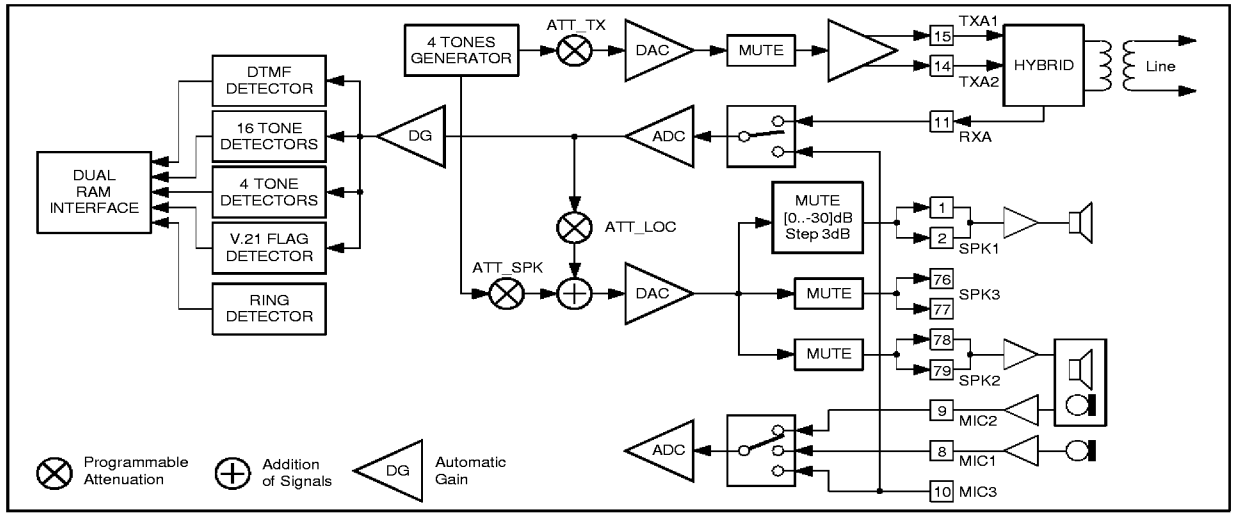
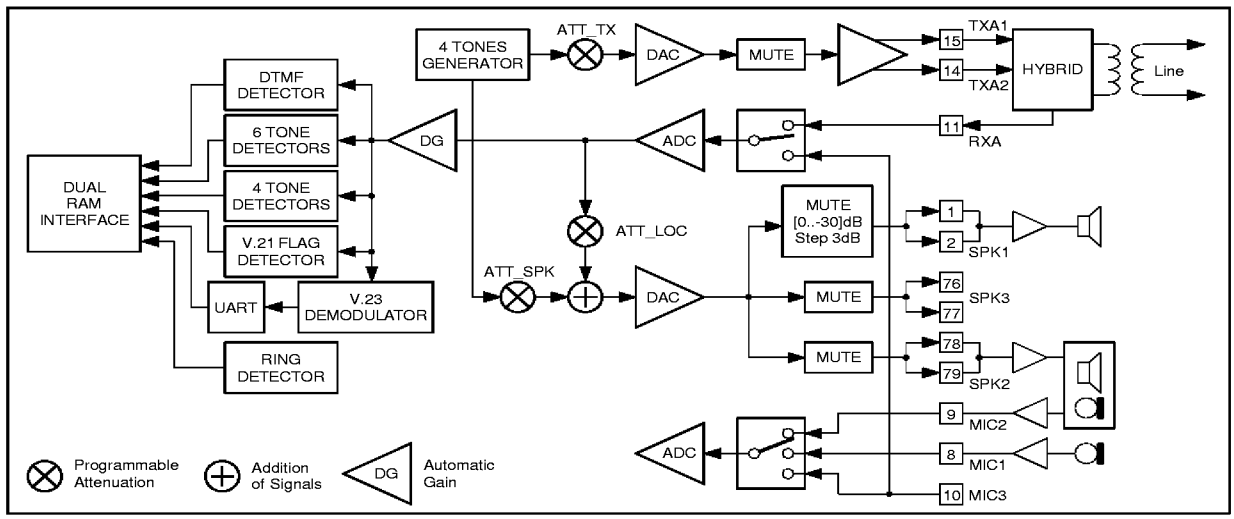


Figure 50 : Tone Mode with Caller ID (TONECID)



XVII - APPENDIX A : MODES OF OPERATION

Figure 51 : Fax Modem Mode (MODEM)

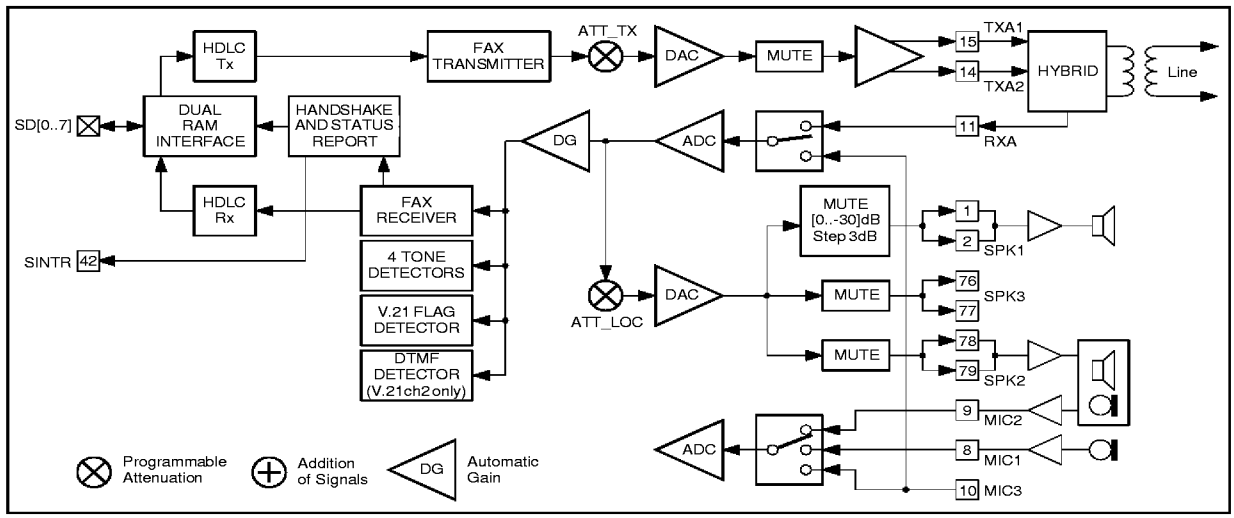
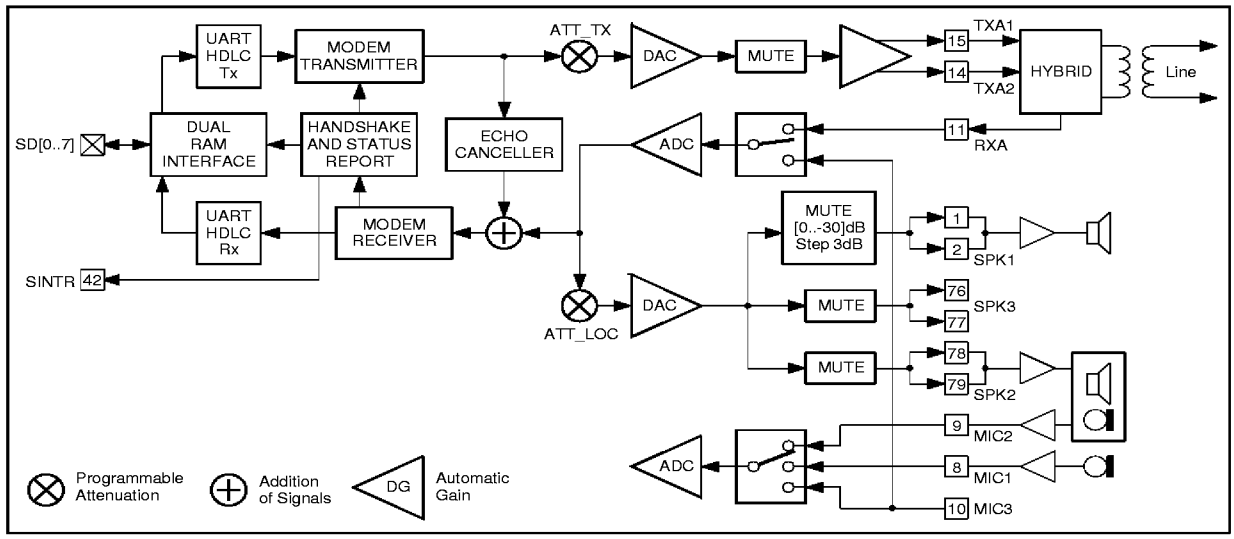


Figure 52 : Data Modem Mode (Full Duplex Modem)



XVII - APPENDIX A : MODES OF OPERATION (continued)

Figure 53 : Decoder Mode (DECODER)

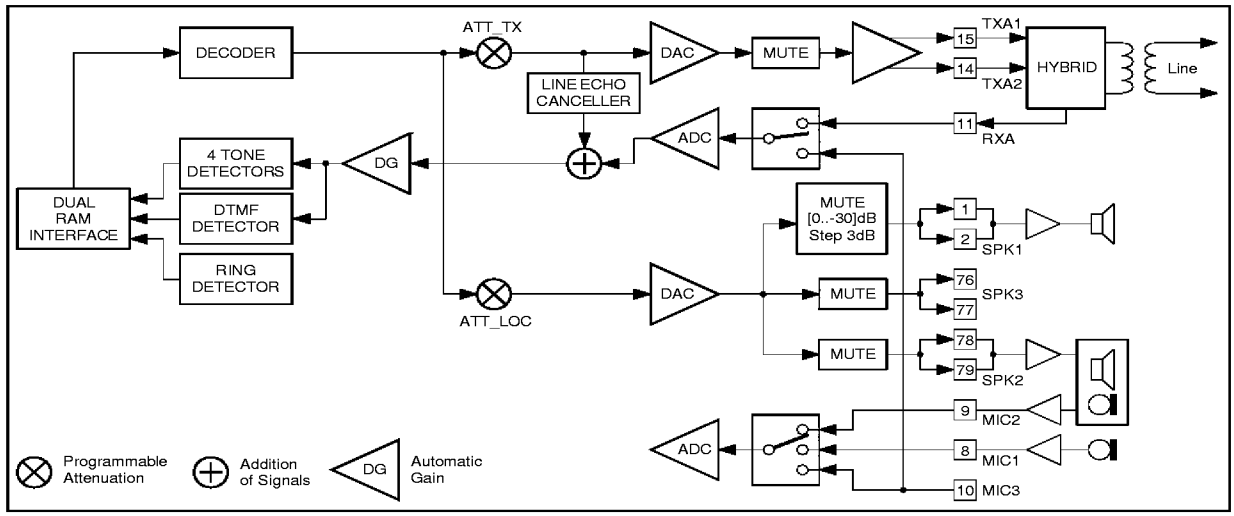
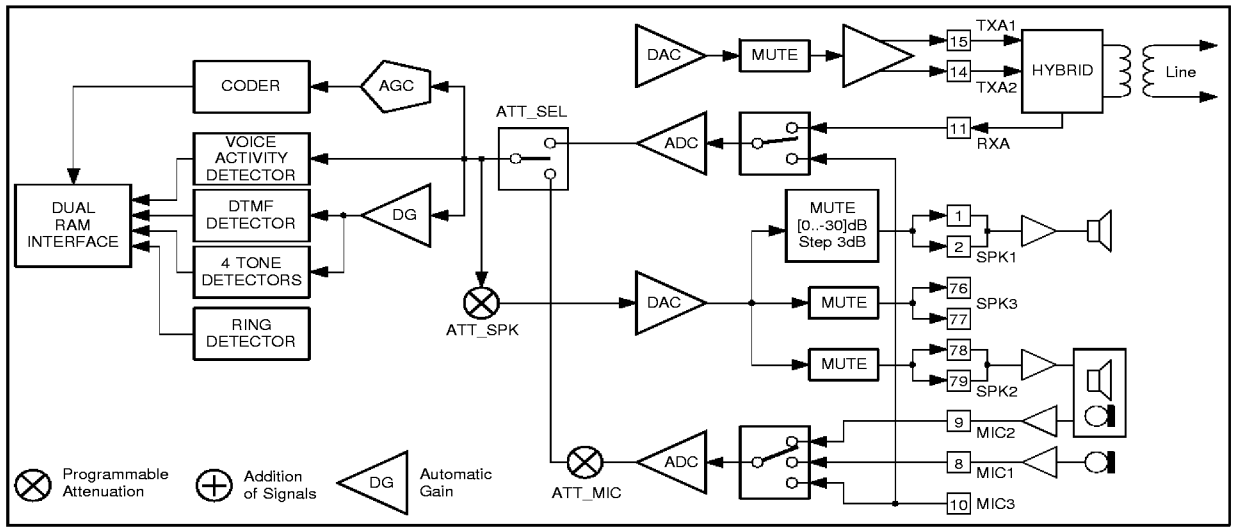


Figure 54 : Coder Mode (CODER)



XVII - APPENDIX A : MODES OF OPERATION (continued)

Figure 55 : Mode Room Monitoring (ROOM)

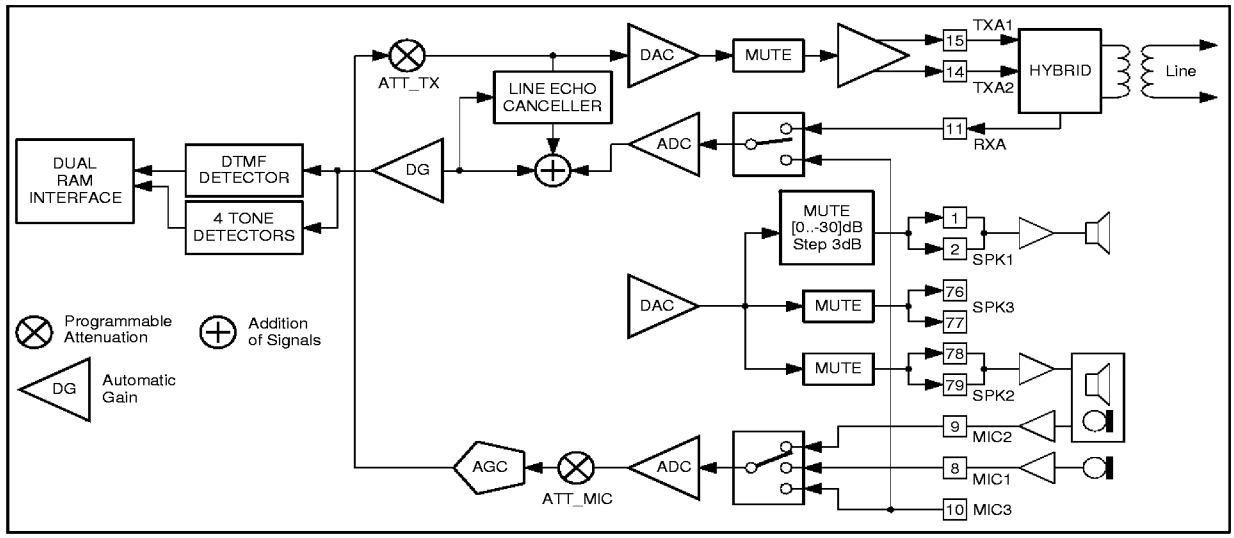
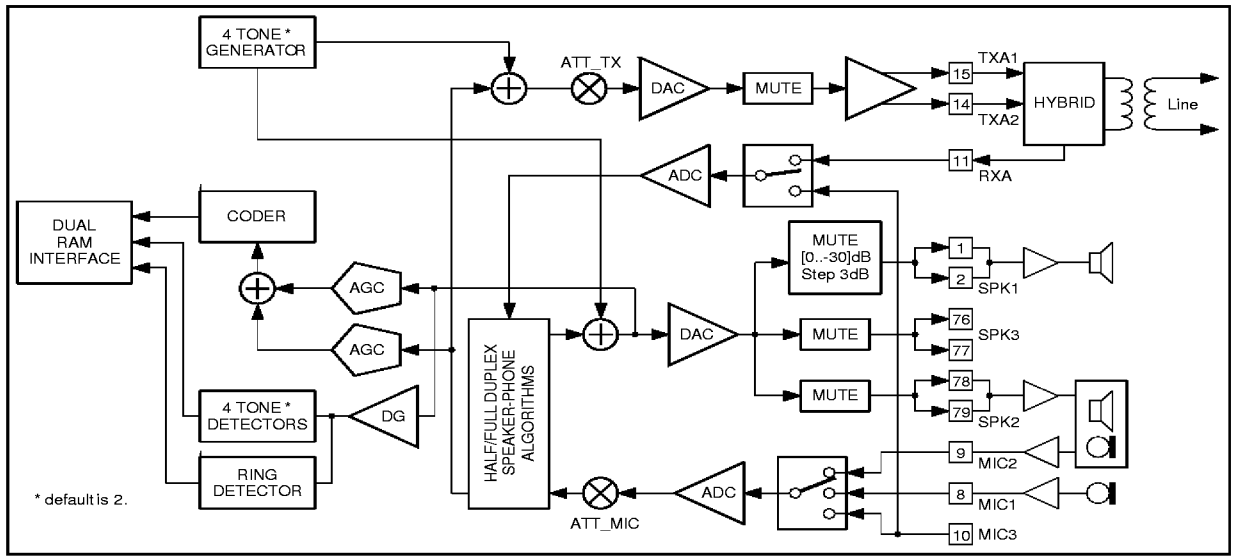
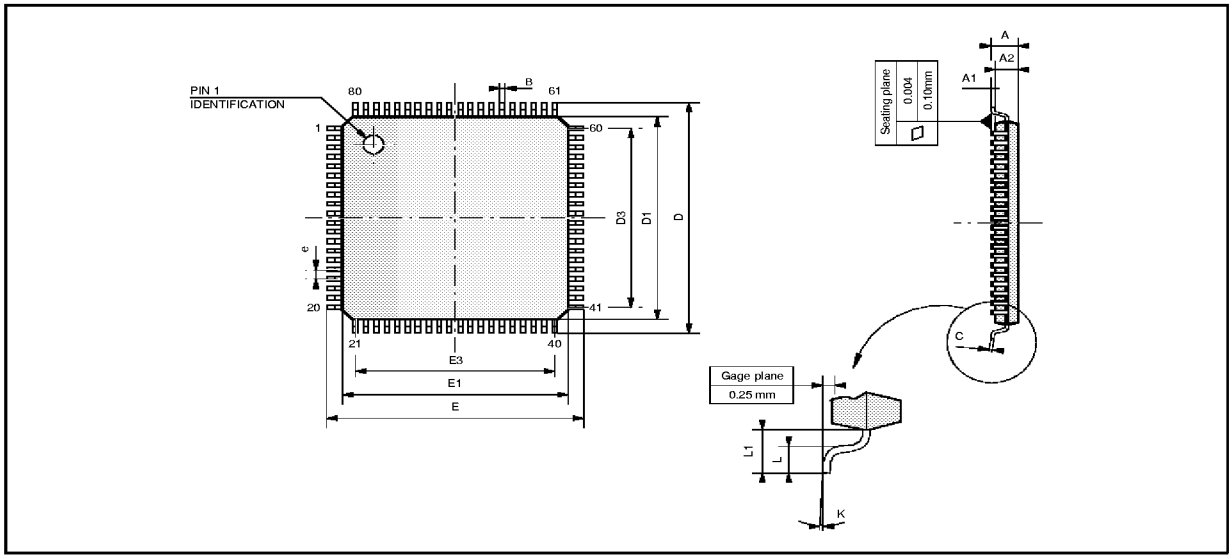


Figure 56 : Mode Telephone (HANDSET)



XVIII - PACKAGE MECHANICAL DATA

80 PINS - PLASTIC QUAD FLAT PACK



PMTQFP80.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.22	0.32	0.38	0.010	0.012	0.014
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.35			0.486	
e		0.65			0.0256	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.35			0.486	
L	0.45	0.60	0.75	0.020	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

TQFP80.TBL