

**16K EPROM HCMOS MCU
WITH EEPROM, RAM AND A/D CONVERTER**

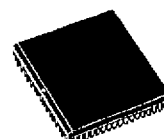
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- Internal Memory :

EPROM	16Kbytes
RAM	256 bytes
EEPROM	512 bytes

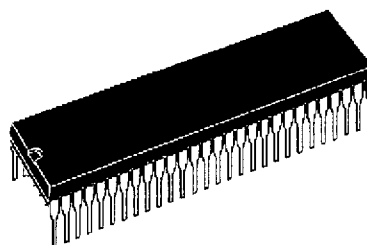
 224 general purpose registers available as RAM, accumulators or index pointers (Register File)
- 80-pin Plastic Quad Flat Pack package for ST90T40Q
- 68-lead Plastic Leaded Chip Carrier package for ST90T40C
- 56-pin shrink DIP package for ST90T40B
- 80-pin Windowed Ceramic Quad Flat Pack package for ST90E40G
- 68-lead Windowed Ceramic Leaded Chip Carrier package for ST90E40L
- 56-pin Shrink Windowed Ceramic package for ST90E40D
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9036 and ST9040 16K ROM devices



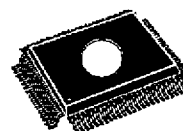
PQFP80



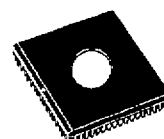
PLCC68



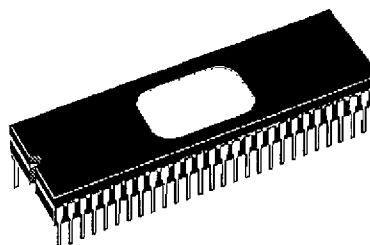
PSDIP56



CQFP80W



CLCC68W



CSDIP56W

(Ordering Information at the end of the Datasheet)

ST90E40 - ST90T40

Figure 1. 80 Pin QFP Package

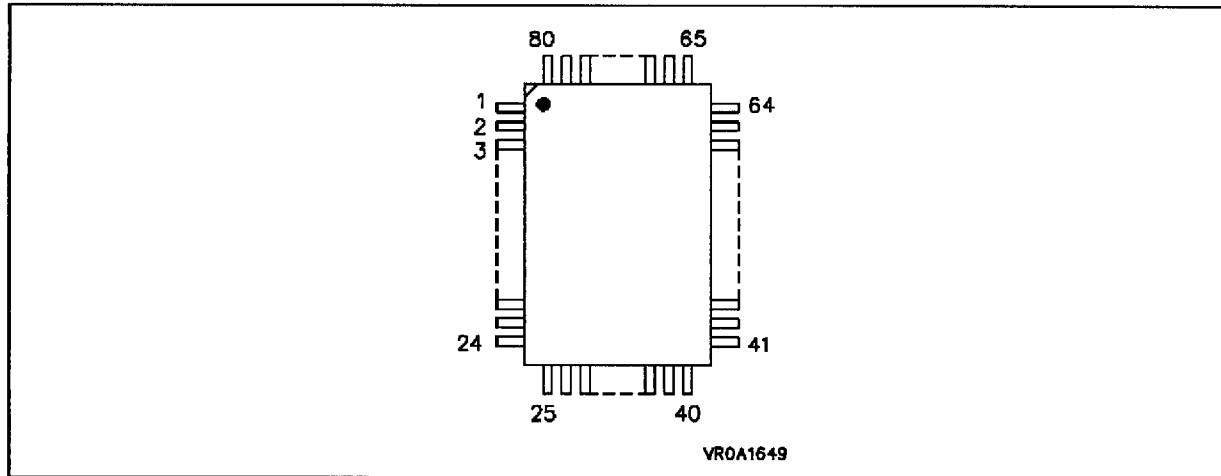


Table 1. ST90E40G-ST90T40Q Pin Description

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AV _{SS}	25	P34/T1INA	64	P20/NMI	80	AV _{DD}
2	AV _{SS}	26	P33/T0OUTB	63	NC	79	NC
3	NC	27	P32/T0INB	62	V _{SS}	78	P47/AIN7
4	P44/AIN4	28	P31/T0OUTA	61	P70/SIN	77	P46/AIN6
5	P57	29	P30/P/D/T0INA	60	P71/SOUT	76	P45/AIN5
6	P56	30	P17/A15	59	P72/INT4/TXCLK /CLKOUT	75	P43/AIN3
7	P55	31	P16/A14	58	P73/INT5 /RXCLK/ADTRG	74	P42/AIN2
8	P54	32	NC	57	P74/P/D/INT6	73	P41/AIN1
9	INT7	33	P15/A13	56	P75/WAIT	72	P40/AIN0
10	INT0	34	P14/A12	55	P76/WDOUT /BUSREQ	71	P27/RRDY5
11	P53	35	P13/A11	54	P77/WDIN /BUSACK	70	P26/INT3 /RDSTB5/P/D
12	NC	36	P12/A10	53	R/W	69	P25/WRRDY5
13	P52	37	P11/A9	52	NC	68	P24/INT1 /WRSTB5
14	P51	38	P10/A8	51	DS	67	P23/SDO
15	P50	39	P00/A0/D0	50	AS	66	P22/INT2/SCK
16	OSCOU	40	P01/A1/D1	49	NC	65	P21/SDI/P/D
17	V _{SS}			48	V _{DD}		
18	V _{SS}			47	V _{DD}		
19	NC			46	P07/A7/D7		
20	OSCIN			45	P06/A6/D6		
21	RESET/V _{PP}			44	P05/A5/D5		
22	P37/T1OUTB			43	P04/A4/D4		
23	P36/T1INB			42	P03/A3/D3		
24	P35/T1OUTA			41	P02/A2/D2		

Figure 2. 68 Pin LCC Package

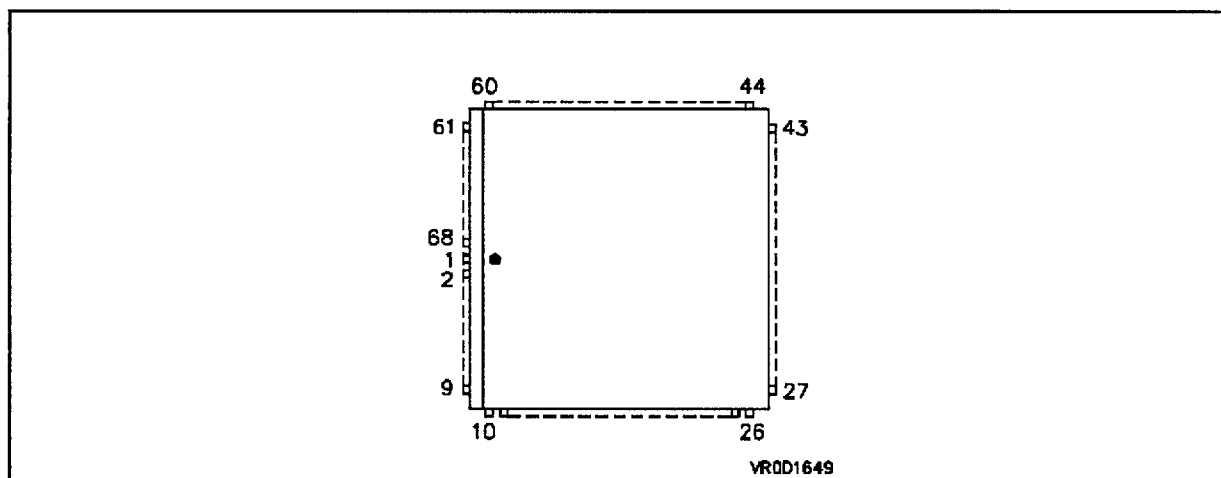


Table 2. ST90E40L-ST90T40C

Pin	Name	Pin	Name	Pin	Name	Pin	Name
61	P44/AIN4	10	P35/T1OUTA	43	P70/SIN	60	AV _{SS}
62	P57	11	P34/T1INA	42	P71/SOUT	59	AV _{DD}
63	P56	12	P33/T0OUTB	41	P72/CLKOUT /TXCLK/INT4	58	P47/AIN7
64	P55	13	P32/T0INB	40	P73/ADTRG /RXCLK/INT5	57	P46/AIN6
65	P54	14	P31/T0OUTA	39	P74/P/D/INT6	56	P45/AIN5
66	INT7	15	P30/P/D/T0INA	38	P75/WAIT	55	P43/AIN3
67	INT0	16	P17/A15	37	P76/WDOUT /BUSREQ	54	P42/AIN2
68	P53	17	P16/A14	36	P77/WDIN /BUSACK	53	P41/AIN1
● 1	P52	18	P15/A13	35	R/W	52	P40/AIN0
2	P51	19	P14/A12	34	DS	51	P27/RRDY5
3	P50	20	P13/A11	33	AS	50	P26/INT3 /RDSTB5/P/D
4	OSCOUT	21	P12/A10	32	V _{DD}	49	P25/WRRDY5
5	V _{SS}	22	P11/A9	31	P07/A7/D7	48	P24/INT1 /WRSTB5
6	OSCIN	23	P10/A8	30	P06/A6/D6	47	P23/SDO
7	RESET/V _{PP}	24	P00/A0/D0	29	P05/A5/D5	46	P22/INT2/SCK
8	P37/T1OUTB	25	P01/A1/D1	28	P04/A4/D4	45	P21/SDI/P/D
9	P36/T1INB	26	P02/A2/D2	27	P03/A3/D3	44	P20/NMI

Figure 1b. 56 Pin Shrink DIP Pinout

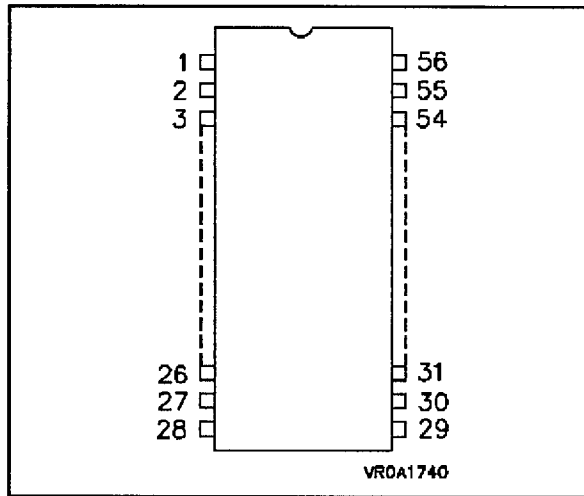


Table 3. ST90E40D-ST90T40B Pin Description

Pin	Pin name	Pin	Pin name
1	P42/AIN2	56	P41/AIN1
2	P43/AIN3	55	P40/AIN0
3	P45/AIN5	54	P23/SDO
4	P46/AIN6	53	P22/INT2/SCK
5	P47/AIN7	52	P21/SDI/P/D
6	AVDD	51	P20/NMI
7	AVSS	50	P70/SIN
8	P44/AIN4	49	P71/SOUT
9	P57	48	P72/CLKOUT TXCLK/INT4
10	P56	47	P73/ADTRG RXCLK/INT5
11	P55	46	P76/WDOUT/BUSREQ
12	P54	45	P77/WDIN/BUSACK
13	P53	44	R/W
14	P52	43	DS
15	OSCOU	42	AS
16	VSS	41	VDD
17	OSCIN	40	VSS
18	RESET	39	P07/A7/D7
19	P37/T1OUTB	38	P06/A6/D6
20	P36/T1INB	37	P05/A5/D5
21	NC	36	P04/A4/D4
22	P35/T1OUTA	35	P03/A3/D3
23	P34/T1INA	34	P02/A2/D2
24	P33/T0OUTB	33	P01/A1/D1
25	P32/T0INB	32	P00/A0/D0
26	P31/T0OUTA	31	P10/A8
27	P30/P/D/T0INA	30	P11/A9
28	P13/A11	29	P12/A10

1.1 GENERAL DESCRIPTION

The ST90E40 and ST90T40 (following mentioned as ST90E40) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

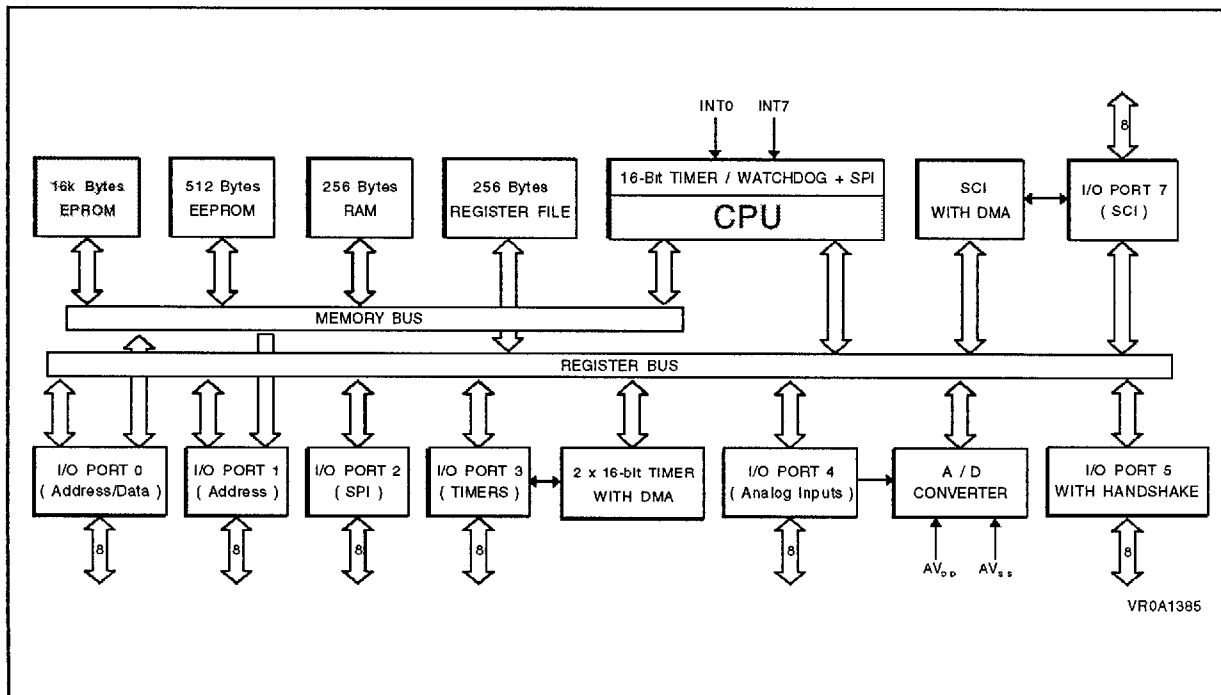
THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E40 may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip EPROM, a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST90E40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I²C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E40 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Figure 3. ST90E40 Block Diagram



GENERAL DESCRIPTION (Continued)

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

1.2 PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/W), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/W.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9040 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/W.

R/W. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/W is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}/V_{PP}$. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input V_{PP} .

INT0, INT7. External interrupts (input, active on rising or falling edge). External interrupt inputs 0 and 7 respectively. INT0 channel may also be used for the timer watchdog interrupt.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11 μ s conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD} . Analog V_{DD} of the Analog to Digital Converter.

AV_{SS} . Analog V_{SS} of the Analog to Digital Converter. *Must be tied to V_{SS} .*

V_{DD} . Main Power Supply Voltage (5V $\pm$ 10%)

V_{SS} . Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 56 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as alternate functions.

1.2.1 I/O PORT ALTERNATE FUNCTIONS

Each pin of the I/O ports of the ST90E40/T30 may assume software programmable Alternative Functions as shown in the Pin Configuration Tables. Due to Bonding options for the packages, some functions may not be present. Table 4 shows the Functions allocated to each I/O Port pin and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 4. ST90E40, T40 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
				PLCC	PQFP	PSDIP
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24	39	32
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25	40	33
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26	41	34
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27	42	35
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28	43	36
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29	44	37
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30	45	38
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31	46	39
P1.0	A8	O	Address bit 8	23	38	31
P1.1	A9	O	Address bit 9	22	37	30
P1.2	A10	O	Address bit 10	21	36	29
P1.3	A11	O	Address bit 11	20	35	28
P1.4	A12	O	Address bit 12	19	34	
P1.5	A13	O	Address bit 13	18	33	
P1.6	A14	O	Address bit 14	17	31	
P1.7	A15	O	Address bit 15	16	30	
P2.0	NMI	I	Non-Maskable Interrupt	44	64	51
P2.0	ROMless	I	ROMless Select (Mask option)	44	64	51
P2.1	P/D	O	Program/Data Space Select	45	65	NC
P2.1	SDI	I	SPI Serial Data Out	45	65	52
P2.2	INT2	I	External Interrupt 2	46	66	53
P2.2	SCK	O	SPI Serial Clock	46	66	53
P2.3	SDO	O	SPI Serial Data In	47	67	54
P2.4	INT1	I	External Interrupt 1	48	68	
P2.4	WRSTB5	I	Handshake Write Strobe P5	48	68	
P2.5	WRDY5	O	Handshake Write Ready P5	49	69	
P2.6	INT3	I	External Interrupt 3	50	70	
P2.6	RDSTB5	I	Handshake Read Strobe P5	50	70	
P2.6	P/D	O	Program/Data Space Select	50	70	
P2.7	RDRDY5	O	Handshake Read Ready P5	51	71	
P3.0	T0INA	I	MF Timer 0 Input A	15	29	27
P3.0	P/D	O	Program/Data Space Select	15	29	27
P3.1	T0OUTA	O	MF Timer 0 Output A	14	28	26
P3.2	T0INB	I	MF Timer 0 Input B	13	27	25
P3.3	T0OUTB	O	MF Timer 0 Output B	12	26	24
P3.4	T1INA	I	MF Timer 1 Input A	11	25	23

PIN DESCRIPTION (Continued)
Table 4. ST90E40, T40 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
				PLCC	PQFP	PSDIP
P3.5	T1OUTA	O	MF Timer 1 Output A	10	24	22
P3.6	T1INB	I	MF Timer 1 Input B	9	23	20
P3.7	T1OUTB	O	MF Timer 1 Output B	8	22	19
P4.0	Ain0	I	A/D Analog Input 0	52	72	55
P4.1	Ain1	I	A/D Analog Input 1	53	73	56
P4.2	Ain2	I	A/D Analog Input 2	54	74	1
P4.3	Ain3	I	A/D Analog Input 3	55	75	2
P4.4	Ain4	I	A/D Analog Input 4	61	4	8
P4.5	Ain5	I	A/D Analog Input 5	56	76	3
P4.6	Ain6	I	A/D Analog Input 6	57	77	4
P4.7	Ain7	I	A/D Analog Input 7	58	78	5
P5.0		I/O	I/O Handshake Port 5	3	15	
P5.1		I/O	I/O Handshake Port 5	2	14	
P5.2		I/O	I/O Handshake Port 5	1	13	14
P5.3		I/O	I/O Handshake Port 5	68	11	13
P5.4		I/O	I/O Handshake Port 5	65	8	12
P5.5		I/O	I/O Handshake Port 5	64	7	11
P5.6		I/O	I/O Handshake Port 5	63	6	10
P5.7		I/O	I/O Handshake Port 5	62	5	9
P7.0	SIN	I	SCI Serial Input	43	61	50
P7.1	SOUT	O	SCI Serial Output	42	60	49
P7.1	ROMless	I	ROMless Select (Mask option)	42	60	49
P7.2	INT4	I	External Interrupt 4	41	59	48
P7.2	TXCLK	I	SCI Transmit Clock Input	41	59	48
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41	59	48
P7.3	INT5	I	External Interrupt 5	40	58	47
P7.3	RXCLK	I	SCI Receive Clock Input	40	58	47
P7.3	ADTRG	I	A/D Conversion Trigger	40	58	47
P7.4	INT6	I	External Interrupt 6	39	57	
P7.4	P/D	O	Program/Data Space Select	39	57	
P7.5	WAIT	I	External Wait Input	38	56	
P7.6	WDOUT	O	T/WD Output	37	55	46
P7.6	BUSREQ	I	External Bus Request	37	55	46
P7.7	WDIN	I	T/WD Input	36	54	45
P7.7	BUSACK	O	External Bus Acknowledge	36	54	45

1.1 MEMORY

The memory of the ST90E40 is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E40 16K bytes of on-chip EPROM memory are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space, while the ST90T40 OTP version has the top 64 bytes of the EPROM reserved by SGS-THOMSON for testing purposes. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at memory addresses 200h through 2FFh.

WARNING. The ST90T40 has its 64 upper bytes in the internal EPROM reserved for testing purpose.

External memory may be addressed using the multiplexed address and data buses (Alternate Functions of Ports 0 and 1). At addresses greater than the first 16K of program space, the ST90E40 executes external memory cycles for instruction fetches. Additional Data Memory may be decoded externally by using the P/D Alternate Function output. The on-chip general purpose (GP) Registers may also be used as RAM memory for minimum chip count systems.

1.2 EPROM PROGRAMMING

The 16384 bytes of EPROM memory of the ST90E40 (16320 for the ST90T40) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

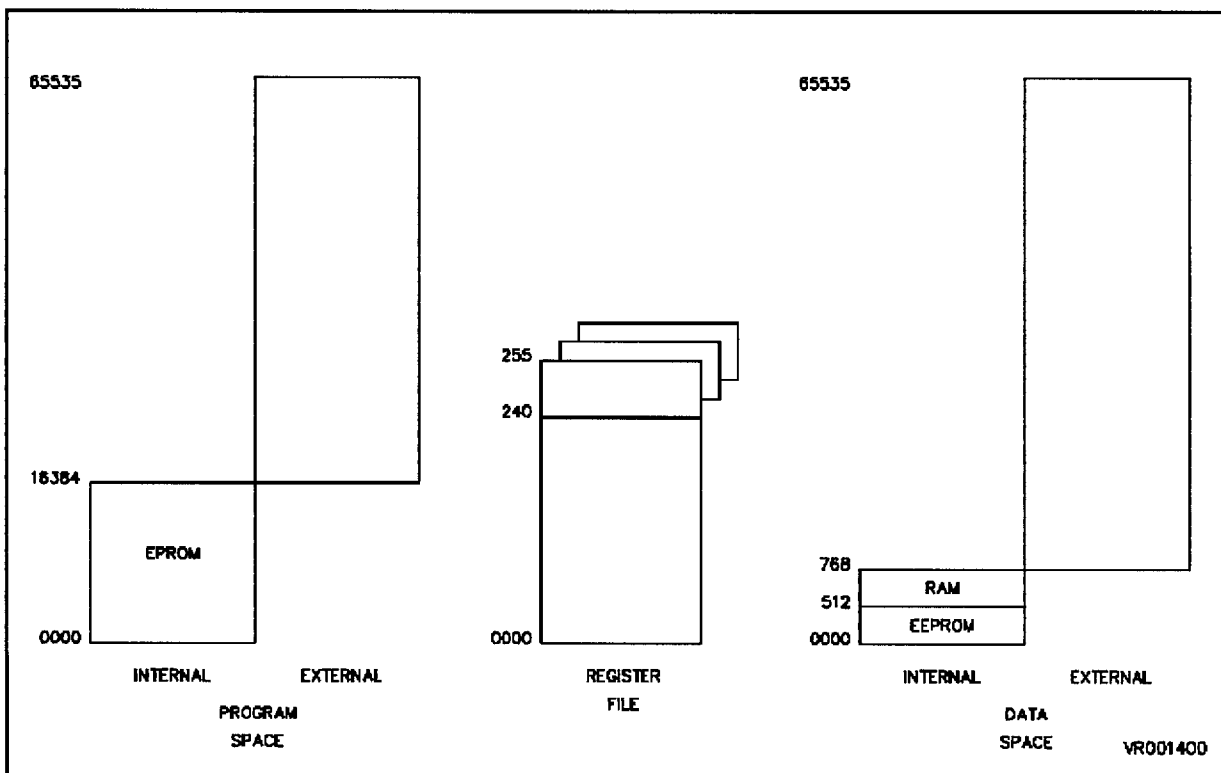
1.2.1 Eprom Erasing

The EPROM of the windowed package of the ST90E40 may be erased by exposure to Ultra-Violet light.

The erasure characteristic of the ST90E40 is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST90E40 packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537Å. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm² power rating. The ST90E40 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Figure 4. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	- 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} = AV_{SS} < AV_{DD} \leq V_{DD}$	V
V_I	Input Voltage	- 0.3 to $V_{DD} + 0.3$	V
V_O	Output Voltage	- 0.3 to $V_{DD} + 0.3$	V
V_{PP}	Input Voltage on V_{PP} Pin	-0.3 to 13.5	V
T_{STG}	Storage Temperature	- 55 to + 150	°C
I_{INJ}	Pin Injection Current Digital	-5 to 5	mA
I_{INJ}	Pin Injection Current Analog	-5 to 5	mA
	Maximum accumulated pin injection Current in the device	-50 to 50	mA

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages are referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	- 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Clock Frequency (INTCLK)		12	MHz

DC ELECTRICAL CHARACTERISTICS

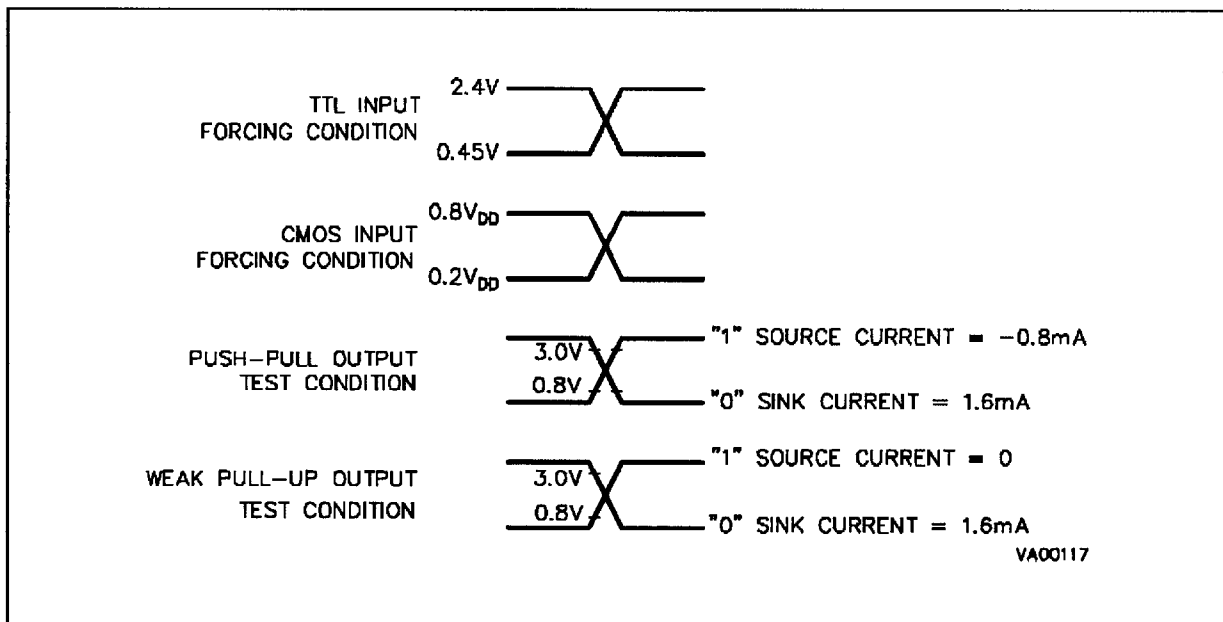
$V_{DD} = 5V \pm 10\%$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	$0.7 V_{DD}$		$V_{DD} + 0.3$	V
V_{ILCK}	Clock Input Low Level	External Clock	- 0.3		$0.3 V_{DD}$	V
V_{IH}	Input High Level	TTL	2.0		$V_{DD} + 0.3$	V
		CMOS	$0.7 V_{DD}$		$V_{DD} + 0.3$	V
V_{IL}	Input Low Level	TTL	- 0.3		0.8	V
		CMOS	- 0.3		$0.3 V_{DD}$	V
V_{IHRS}	$\overline{\text{RESET}}$ Input High Level		$0.7 V_{DD}$		$V_{DD} + 0.3$	V
V_{ILRS}	$\overline{\text{RESET}}$ Input Low Level		-0.3		$0.3 V_{DD}$	V
V_{HYRS}	$\overline{\text{RESET}}$ Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, $I_{load} = -0.8\text{mA}$	$V_{DD} - 0.8$			V
V_{OL}	Output Low Level	Push Pull or Open Drain, $I_{load} = 1.6\text{mA}$			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, $V_{OL} = 0V$	- 50	- 200	- 420	μA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$, under Reset	- 80	- 200	- 420	μA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	- 10		+ 10	μA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	- 30		+ 30	μA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	- 3		+3	μA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	- 10		+ 10	μA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	- 10		+ 10	μA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

DC TEST CONDITIONS

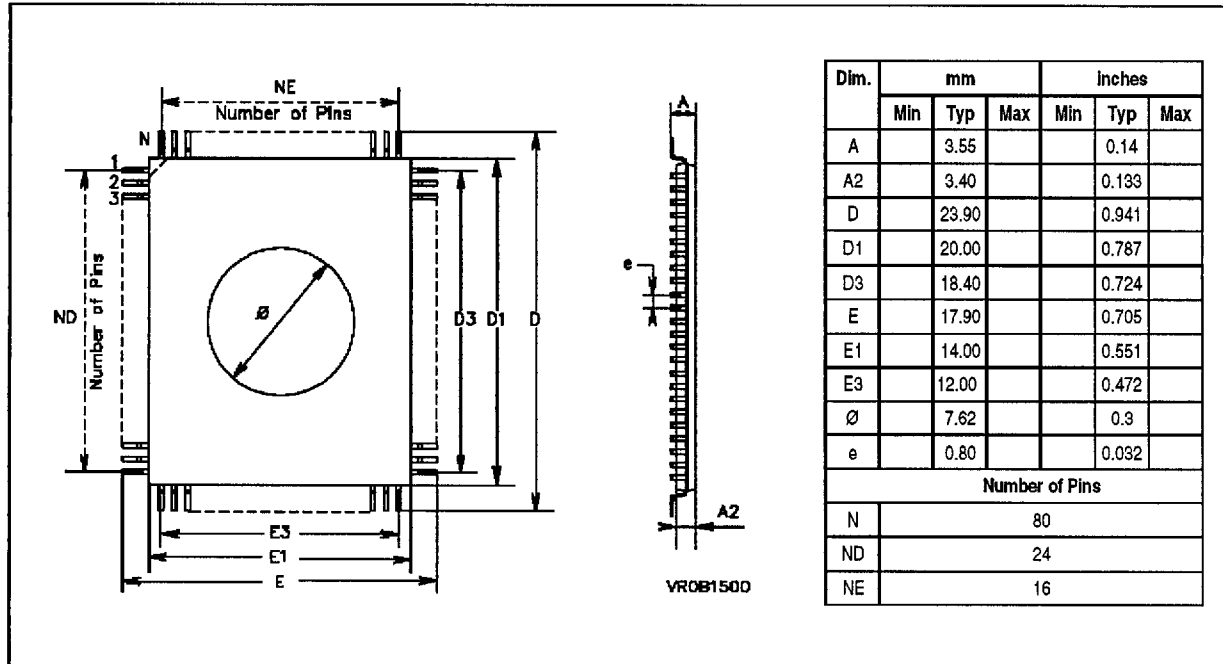


AC ELECTRICAL CHARACTERISTICS(V_{DD} = 5V ± 10% T_A = – 40°C to + 85°C, unless otherwise specified)

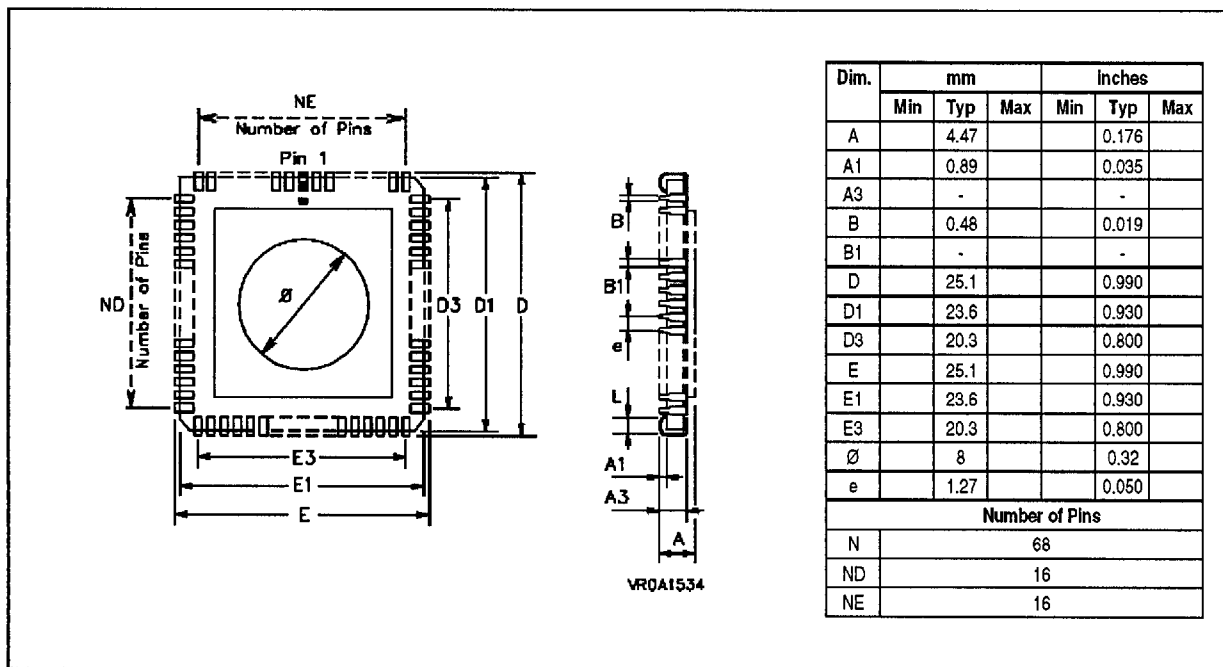
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I _{DD}	Run Mode Current no CPUCLK prescale, Clock divide by 2	24MHz			50	mA
I _{DP2}	Run Mode Current Prescale by 2 Clock divide by 2	24MHz			30	mA
I _{WFI}	WFI Mode Current no CPUCLK prescale, Clock divide by 2	24MHz			20	mA
I _{HALT}	HALT Mode Current	24MHz		50	100	µA

PACKAGE MECHANICAL DATA

80-Pin Ceramic Quad Flat Package with Window

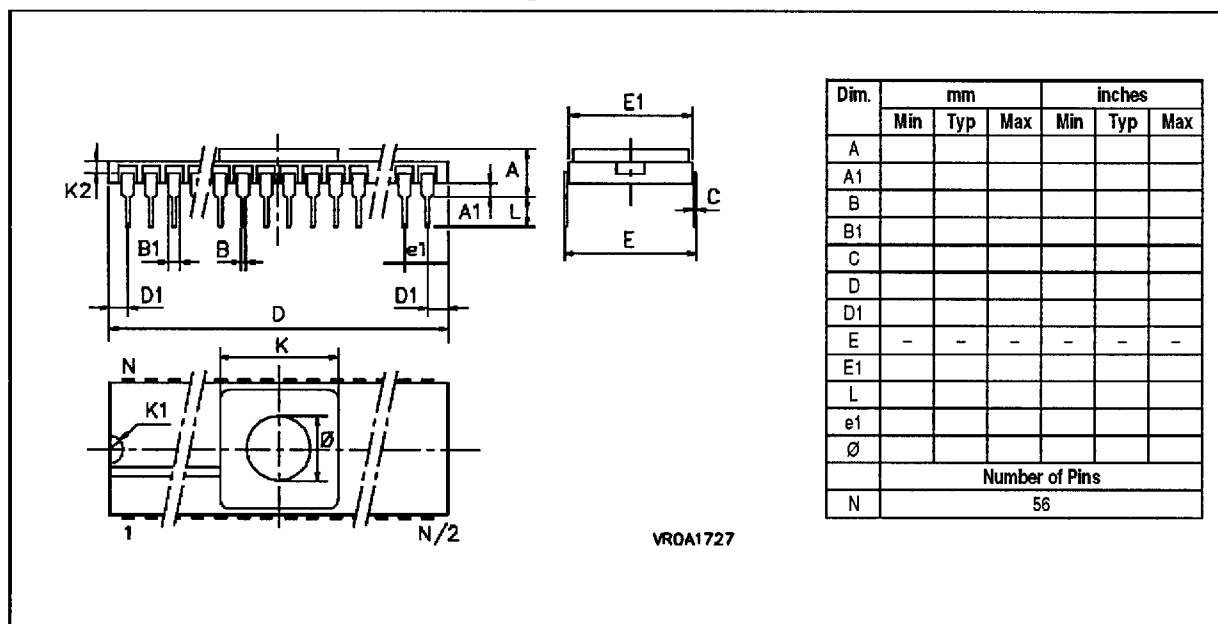


68-Pin Ceramic Leadless Chip Carrier with Window



ST90E40 - ST90T40

56-Pin Ceramic Shrink Dual-In-line Package with window, 600 Mil Width



ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E40L1/ES ⁽¹⁾	24MHz	0°C to + 70°C	CLCC68W
ST90E40G1/ES ⁽¹⁾		0°C to + 70°C	CQFP80W
ST90E40D1/ES ⁽¹⁾		0°C to + 70°C	CSDIP56W
ST90T40C6	24MHz	-40°C to + 85°C	PLCC68
ST90T40Q1		0°C to + 70°C	PQFP80
ST90T40B6		-40°C to + 85°C	PSDIP56

Note . EPROM parts are tested at 25°C only