T-75-37-07

Z8030 Military Z8000® Z-SCC Serial Communications Controller

Zilog

Military Electrical Specification

July 1985

FEATURES

- Two independent, 0 to 1.5M bit/second, full-duplex channels, each with a separate crystal oscillator, baud rate generator, and Digital Phase-Locked Loop for clock recovery.
- Multi-protocol operation under program control; programmable for NRZ, NRZI, or FM data encoding.
- Asynchronous mode with five to eight bits and one, one and one-half, or two stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection.
- Synchronous mode with internal or external character synchronization on one or two synchronous characters and CRC generation and checking with CRC-16 or CRC-CCITT preset to either 1s or 0s.
- SDLC/HDLC mode with comprehensive frame-level control, automatic zero insertion and deletion, I-field residue handling, abort generation and detection, CRC generation and checking, and SDLC Loop mode operation.
- Local Loopback and Auto Echo modes.
- 1.544M bit/second T1 digital trunk compatible version available.

GENERAL DESCRIPTION

The Z8030 Z-SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with the Zilog Z-BUS. The Z-SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The Z-SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, Digital Phase-Locked Loops, and crystal oscillators that dramatically reduce the need for external logic.

The Z-SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and Synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

The device can generate and check CRC codes in any Synchronous mode and can be programmed to check data integrity in various modes. The Z-SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The Z-BUS daisy-chain interrupt hierarchy is also supported—as is standard for Zilog peripheral components.

The Z8030 Z-SCC is packaged in a 40-pin ceramic DIP and 44-pin chip carrier and uses a single +5V power supply.

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TIMING

The Z-SCC generates internal control signals from $\overline{AS}$ and $\overline{DS}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{AS}$ and $\overline{DS}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the Z-SCC. The recovery time required for proper operation is specified from the rising edge of $\overline{DS}$ in the first transaction involving the Z-SCC to the falling edge of $\overline{DS}$ in the second transaction involving the Z-SCC. This time must be at least 6 PCLK cycles plus 200 ns.

Read Cycle Timing. Figure 1 illustrates read cycle timing. The address on AD_0-AD_7 and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be High to indicate a Read cycle. CS_1 must also be High for the Read cycle to occur. The data bus drivers in the Z-SCC are then enabled while $\overline{DS}$ is Low.

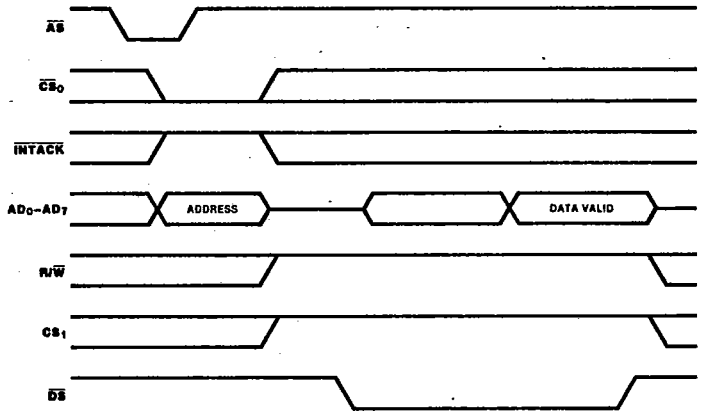

Figure 1. Read Cycle Timing

Write Cycle Timing. Figure 2 illustrates Write cycle timing. The address on AD_0-AD_7 and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be Low to indicate a Write cycle. CS_1 must be High for the Write cycle to occur. $\overline{DS}$ Low strobes the data into the Z-SCC.

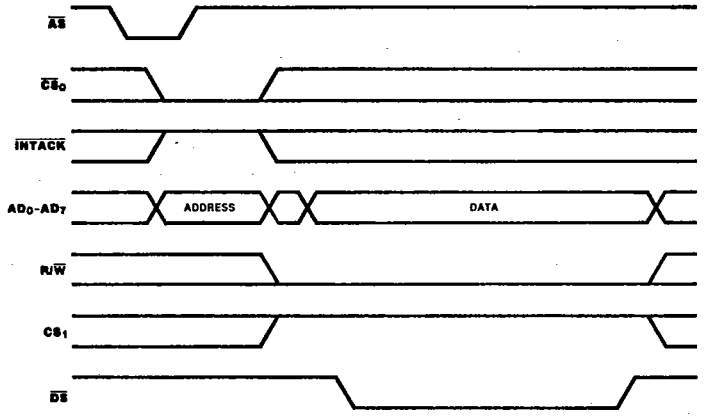

Figure 2. Write Cycle Timing

Interrupt Acknowledge Cycle Timing. Figure 3 illustrates Interrupt Acknowledge cycle timing. The address on AD_0-AD_7 and the state of $\overline{CS}_0$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. However, if $\overline{INTACK}$ is Low, the address and $\overline{CS}_0$ are ignored. The state of the R/$\overline{W}$ and CS_1 are also ignored for the duration of the Interrupt Acknowledge cycle. Between the rising edge of $\overline{AS}$ and the falling edge of $\overline{DS}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the Z-SCC and IEI is High when $\overline{DS}$ falls, the Acknowledge cycle was intended for the Z-SCC. In this case, the Z-SCC may be programmed to respond to $\overline{DS}$ Low by placing its interrupt vector on AD_0-AD_7. It then sets the appropriate Interrupt-Under-Service latch internally.

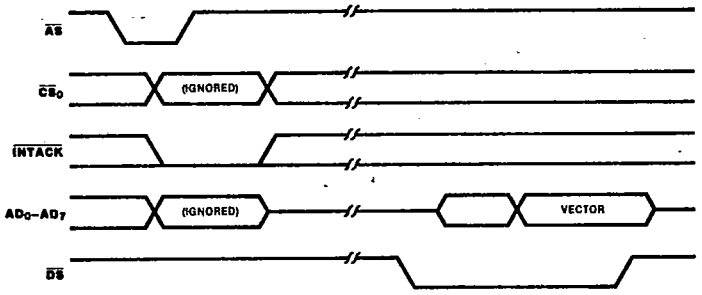

Figure 3. Interrupt Acknowledge Cycle Timing

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ABSOLUTE MAXIMUM RATINGS

Guaranteed by characterization/design.

Voltages on all inputs and outputs
with respect to ground. . . . . −0.3V to +7.0V
Operating Case Temperature. . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Absolute Maximum Power Dissipation 2.0W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

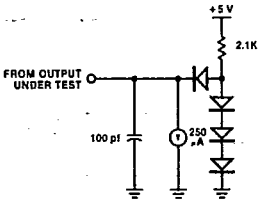
The DC Characteristics and Capacitance sections listed below apply for the following standard test conditions, unless otherwise noted.

Military Operating Temperature Range (T_C)
−55°C to +125°C

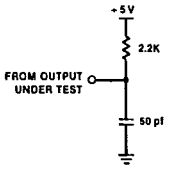
Standard Military Test Condition
$+4.5V \leq V_{CC} \leq +5.5V$

All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All ac parameters assume a load capacitance of 50 pf max.



Standard Test Load



Open-Drain Test Load

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	+2.2[a]	V_{CC} + 0.3[c]	V	
V_{IL}	Input Low Voltage	−0.3[c]	+0.8[a]	V	
V_{OH}	Output High Voltage	+2.4[c]		V	I_{OH} = −250 µA
V_{OL}	Output Low Voltage		+0.4[c]	V	I_{OL} = 2.0 mA
I_{IL}	Input Leakage Current		±10[a]	µA	$+0.4 \leq V_{IN} \leq +2.4V$
I_{OL}	Output Leakage		±10[a]	µA	$+0.4 \leq V_{OUT} \leq +2.4V$
I_{CC}	V_{CC} Supply Current		+350[a]	mA	

V_{CC} = 5V ± 5% unless otherwise specified, over specified temperature range.

CAPACITANCE

Symbol	Parameter	Max	Unit
C_{IN}	Input Capacitance	10[c]	pf
C_{OUT}	Output Capacitance	15[c]	pf
$C_{I/O}$	Bidirectional Capacitance	20[c]	pf

T_A = 25°C, f = 1 MHz
Unmeasured pins returned to ground.

Parameter Test Status:

a Tested
b Guaranteed
c Guaranteed by characterization/design

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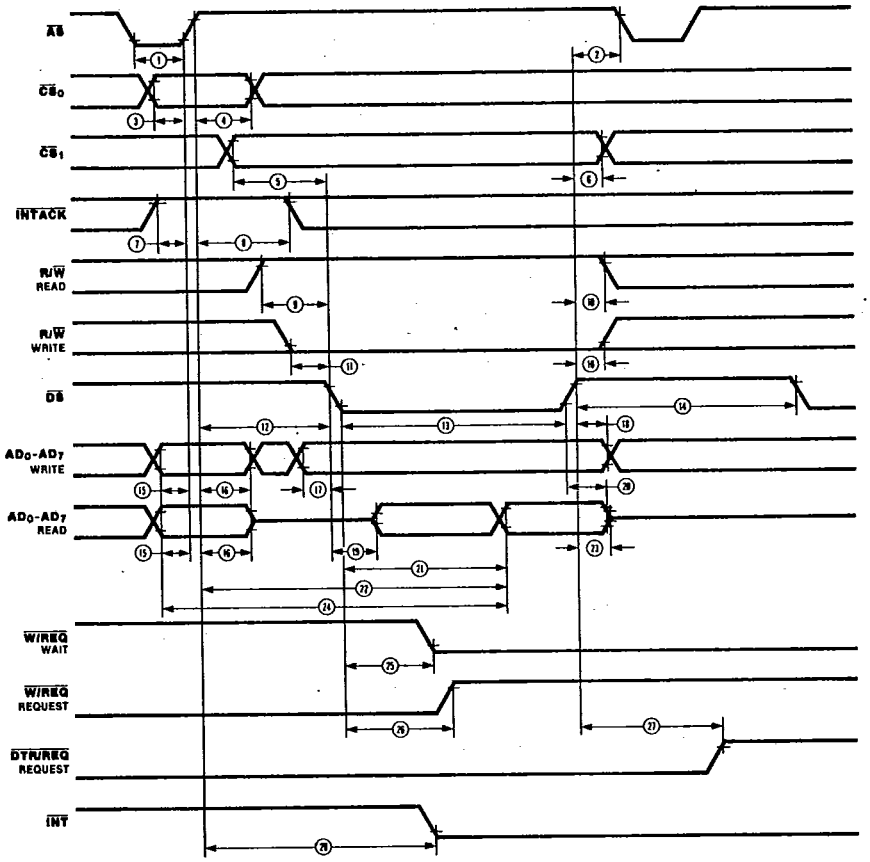
READ AND WRITE TIMING



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AC CHARACTERISTICS

Read and Write Timing

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes†
1	TwAS	$\overline{AS}$ Low Width	70[a]		50[a]		
2	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50[b]		25[b]		
3	TsCS0(AS)	$\overline{CS}_0$ to $\overline{AS}$ ↑ Setup Time	0[b]		0[b]		1
4	ThCS0(AS)	$\overline{CS}_0$ to $\overline{AS}$ ↑ Hold Time	60[a]		40[a]		1
5	TsCS1(DS)	CS_1 to $\overline{DS}$ ↓ Setup Time	100[b]		80[a]		1
6	ThCS1(DS)	CS_1 to $\overline{DS}$ ↑ Hold Time	55[a]		40[b]		1
7	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0[b]		0[b]		
8	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250[b]		250[b]		
9	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100[a]		80[a]		
10	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55[b]		40[b]		
11	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0[b]		0[b]		
12	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	85[b]		50[b]		
13	TwDSI	$\overline{DS}$ Low Width	390[b]		250[b]		
14	TrC	Valid Access Recovery Time	6TcPC +200[b]		6TcPC +130[b]		2
15	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30[a]		10[a]		1
16	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50[a]		30[a]		1
17	TsDW(DS)	Write Data to $\overline{DS}$↓ Setup Time	30[a]		20[a]		
18	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30[b]		20[b]		
19	TdDS(DA)	$\overline{DS}$ ↓ to Data Active Delay	0[b]		0[b]		
20	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0[b]		0[a]		
21	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250[b]		180[b]	
22	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Valid Delay		520[b]		335[b]	

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the SCC.
†Units in nanoseconds (ns).

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design.

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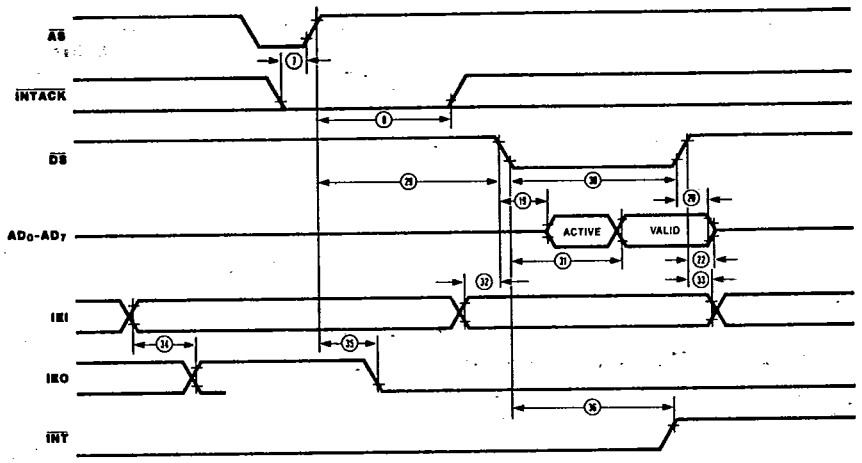
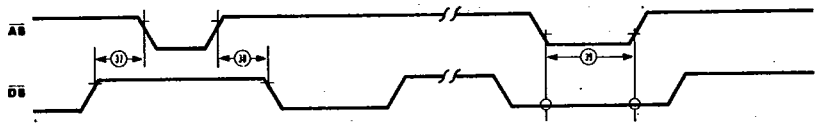
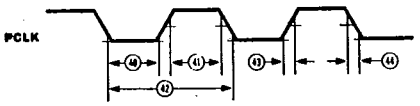
INTERRUPT ACKNOWLEDGE TIMING



RESET TIMING



CYCLE TIMING



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AC CHARACTERISTICS

Read and Write Timing (Continued)

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes*†
23	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70[b]		45[b]	3
24	TdA(DR)	Address Required Valid to Read Data Valid Delay		570[b]		420[a]	
25	TdDS(W)	$\overline{DS}$ ↓ to Wait Valid Delay		240[b]		200[b]	4
26	TdDSf(REQ)	$\overline{DS}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240[b]		200[b]	
27	TdDSr(REQ)	$\overline{DS}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		5TcPC +300[b]		5TcPC +500[b]	
28	TdAS(INT)	$\overline{AS}$ ↑ to $\overline{INT}$ Valid Delay		500[b]		500[b]	4
29	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay	250[b]		250[b]		5
30	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390[b]		250[b]		
31	TdDSA(DR)	$\overline{DS}$ ↓ (Acknowledge) to Read Data Valid Delay		250[b]		180[b]	
32	TsIEI(DSA)	IEI to $\overline{DS}$ ↓ (Acknowledge) Setup Time	120[b]		100[b]		
33	ThIEI(DSA)	IEI to $\overline{DS}$ ↑ (Acknowledge) Hold Time	0[b]		0[b]		
34	TdIEI(IEO)	IEI to IEO Delay		120[b]		100[b]	
35	TdAS(IEO)	$\overline{AS}$ ↑ to IEO Delay		250[b]		250[b]	6
36	TdDSA(INT)	$\overline{DS}$ ↓ (Acknowledge) to $\overline{INT}$ Inactive Delay		500[b]		500[b]	4
37	TdDS(ASQ)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay for No Reset	30[b]		15[b]		
38	TdASQ(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay for No Reset	30[b]		30[b]		1
39	TwRES	$\overline{AS}$ and $\overline{DS}$ Coincident Low for Reset	250[b]		250[b]		7
40	TwPCl	PCLK Low Width	105[b]	2000[b]	70[a]	1000[b]	
41	TwPCh	PCLK High Width	105[b]	2000[b]	70[a]	1000[b]	
42	TcPC	PCLK Cycle Time	250[a]	4000[b]	165[a]	2000[b]	
43	TrPC	PCLK Rise Time		20[b]		15[b]	
44	TfPC	PCLK Fall Time		20[b]		10[a]	

NOTES:

3. Float delay is defined as the time required for a ±0.5V change in the output with a maximum DC load and minimum AC load.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any Z-SCC in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain, TsIEI(DSA) for the Z-SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.
6. Parameter applies only to a Z-SCC pulling $\overline{INT}$ Low at the beginning of the Interrupt Acknowledge transaction.
7. Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the Z-SCC.

*All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0."

†Units in nanoseconds (ns).

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design.

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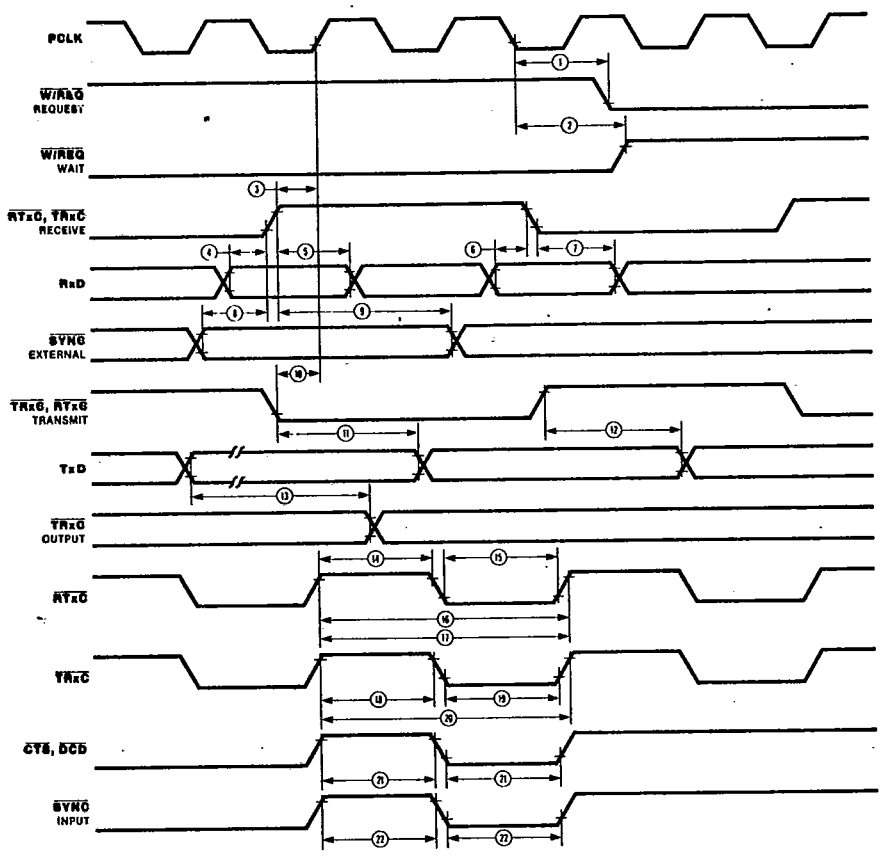
GENERAL TIMING



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AC CHARACTERISTICS

General Timing

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes†
1	TdPC(REQ)	PCLK ↓ to W/$\overline{REQ}$ Valid		250[b]		250[b]	
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350[b]		350[b]	
3	TsRXC(PC)	$\overline{RxC}$ ↑ to PCLK ↑ Setup Time (PCLK ÷ 4 case only)	80[a]	TwPCL[b]	70[a]	TwPCL[b]	1,4
4	TsRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Setup Time (X1 Mode)	0[b]		0[b]		1
5	ThRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Hold Time (X1 Mode)	150[b]		150[a]		1
6	TsRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Setup Time (X1 Mode)	0[b]		0[b]		1,5
7	ThRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Hold Time (X1 Mode)	150[b]		150[a]		1,5
8	TsSY(RXC)	$\overline{SYNC}$ to $\overline{RxC}$ ↑ Setup Time	−200[b]		−200[b]		1
9	ThSY(RXC)	$\overline{SYNC}$ to $\overline{RxC}$ ↑ Hold Time	3TcPC +200[b]		3TcPC +200[b]		1
10	TsTXC(PC)	$\overline{TxC}$ ↓ to PCLK ↑ Setup Time	0[a]		0[a]		2,4
11	TdTXCf(TXD)	$\overline{TxC}$ ↓ to TxD Delay (X1 Mode)		300[a]		230[a]	2
12	TdTXCr(TXD)	$\overline{TxC}$ ↑ to TxD Delay (X1 Mode)		300[a]		230[a]	2,5
13	TdTXD(TRX)	TxD to $\overline{TRxC}$ Delay (Send Clock Echo)		200[b]		200[b]	
14	TwRTXh	$\overline{RTxC}$ High Width	180[b]		180[b]		6
15	TwRTXl	$\overline{RTxC}$ Low Width	180[b]		180[b]		6
16	TcRTX	$\overline{RTxC}$ Cycle Time	400[b]		400[b]		6
17	TcRTXX	Crystal Oscillator Period	250[b]	1000[b]	250[b]	1000[b]	3
18	TwTRXh	$\overline{TRxC}$ High Width	180[b]		180[b]		6
19	TwTRXl	$\overline{TRxC}$ Low Width	180[b]		180[b]		6
20	TcTRX	$\overline{TRxC}$ Cycle Time	400[b]		400[b]		6
21	TwEXT	$\overline{DCD}$ or $\overline{CTS}$ Pulse Width	200[b]		200[b]		
22	TwSY	$\overline{SYNC}$ Pulse Width	200[b]		200[b]		

NOTES:
1. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
2. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
3. Both $\overline{RTxC}$ and $\overline{SYNC}$ have 30 pf capacitors to the ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between $\overline{RxC}$ and PCLK or $\overline{TxC}$ and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.

†Units in nanoseconds (ns).

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design.

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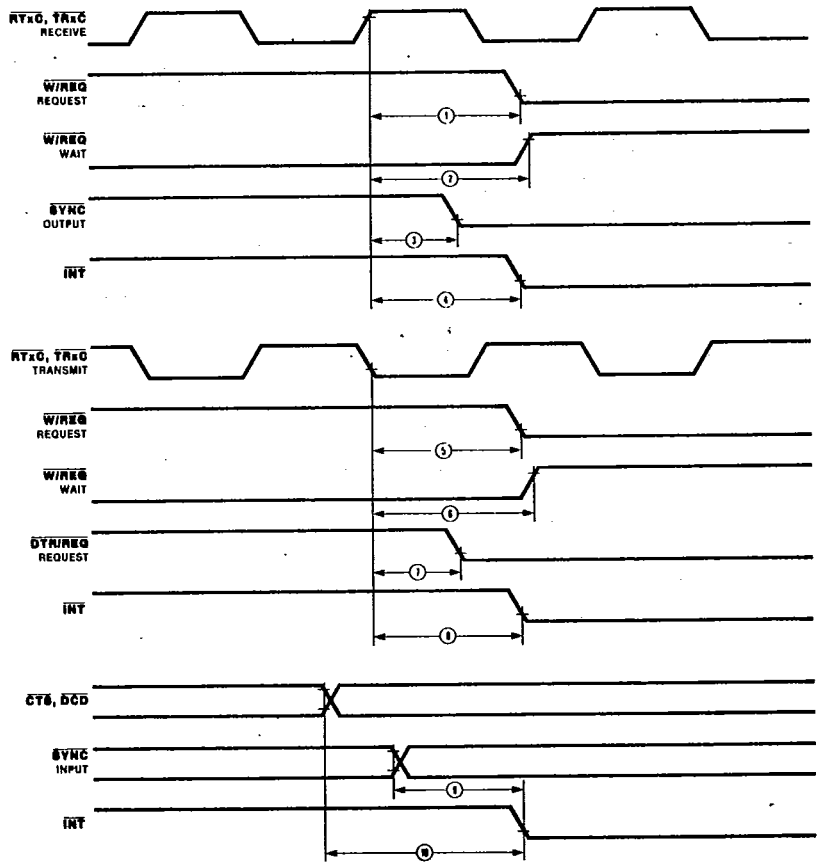
SYSTEM TIMING



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AC CHARACTERISTICS

System Timing

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes
1	TdRXC(REQ)	$\overline{RxC}$ ↑ to $\overline{W/REQ}$ Valid Delay	8[b]	12[b]	8[b]	12[b]	2,4
2	TdRXC(W)	$\overline{RxC}$ ↑ to Wait Inactive Delay	8[b]	12[b]	8[b]	12[b]	1,2,4
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay	4[b]	7[b]	4[b]	7[b]	2,4
4	TdRXC(INT)	$\overline{RxC}$ ↑ $\overline{INT}$ Valid Delay	8[b]	12[b]	8[b]	12[b]	1,2,4
			+2	+3	+2	+3	5
5	TdTXC(REQ)	$\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay	5[b]	8[b]	5[b]	8[b]	3,4
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay	5[b]	8[b]	5[b]	8[b]	1,3,4
7	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay	4[b]	7[b]	4[b]	7[b]	3,4
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay	4[b]	6[b]	4[b]	6[b]	1,3,4
			+2	+3	+2	+3	5
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay	2[b]	3[b]	2[b]	3[b]	1,5
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay	2[b]	3[b]	2[b]	3[b]	1,5

NOTES:
1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RtxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RtxC}$, whichever is supplying the transmit clock.
4. Units equal to TcPC.
5. Units equal to $\overline{AS}$.

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design.

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PIN DESCRIPTION

The following section describes the pin functions of the Z-SCC. Figures 1 and 2 detail the respective pin functions and pin assignments.

AD_0-AD_7. *Address/Data Bus* (bidirectional, active High, 3-state). These multiplexed lines carry register addresses to the Z-SCC as well as data or control information to and from the Z-SCC.

$\overline{AS}$. *Address Strobe* (input, active Low). Addresses on AD_0-AD_7 are latched by the rising edge of this signal.

$\overline{CS_0}$. *Chip Select 0* (input, active Low). This signal is latched concurrently with the addresses on AD_0-AD_7 and must be active for the intended bus transaction to occur.

CS_1. *Chip Select 1* (input, active High). This second select signal must also be active before the intended bus transaction can occur. CS_1 must remain active throughout the transaction.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear to Send* (inputs, active Low). If these pins are programmed as Auto Enables, a Low on the inputs enables their respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The Z-SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs active Low). These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The Z-SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

$\overline{DS}$. *Data Strobe* (input, active Low). This signal provides timing for the transfer of data into and out of the Z-SCC. If $\overline{AS}$ and $\overline{DS}$ coincide, this is interpreted as a reset.

$\overline{DTR/REQA}$, $\overline{DTR/REQB}$. *Data Terminal Ready/Request* (outputs, active Low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request lines for a DMA controller.

IEI. *Interrupt Enable In* (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing a Z-SCC interrupt or the Z-SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$. *Interrupt Request* (output, open-drain, active Low) This signal is activated when the Z-SCC requests an interrupt.

$\overline{INTACK}$. *Interrupt Acknowledge* (input, active Low). This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the Z-SCC interrupt daisy chain settles. When $\overline{DS}$ becomes active, the Z-SCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of $\overline{AS}$.

PCLK. *Clock* (input). This is the master Z-SCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock, although the frequency of this clock must be at least 90% of the CPU clock frequency for a Z8000. PCLK is a TTL level signal.

RxDA, RxDB. *Receive Data* (inputs, active High). These input signals receive serial data at standard TTL levels.

$\overline{RTxCA}$, $\overline{RTxCB}$. *Receive/Transmit Clocks* (inputs, active Low). These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock of the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in Asynchronous modes.

$\overline{RTSA}$, $\overline{RTSB}$. *Request To Send* (outputs, active Low). When the Request To Send (RTS) bit in Write Register 5 is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

R/$\overline{W}$. *Read/Write* (input). This signal specifies whether the operation to be performed is a read or a write.

$\overline{SYNCA}$, $\overline{SYNCB}$. *Synchronization* (inputs or outputs, active Low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit.

In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven Low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern

is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

TxDA, TxDB. *Transmit Data* (outputs, active High). These output signals transmit serial data at standard TTL levels.

$\overline{\text{TRxCA}}$, $\overline{\text{TRxCB}}$. *Transmit/Receive Clocks* (inputs or outputs, active Low). These pins can be programmed in several different modes of operation. $\overline{\text{TRxC}}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

$\overline{\text{W/REQA}}$, $\overline{\text{W/REQB}}$. *Wait/Request* (outputs, open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function). These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the Z-SCC data rate. The reset state is Wait.

PACKAGE PINOUTS

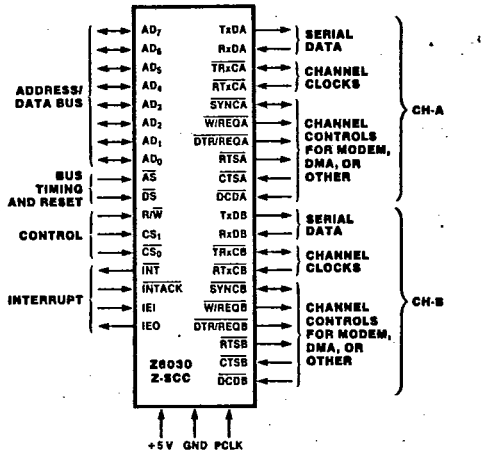

Figure 4. Pin Functions

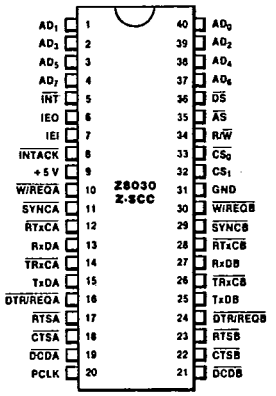

Figure 5. 40-pin Dual-In-Line Package (DIP), Pin Assignments

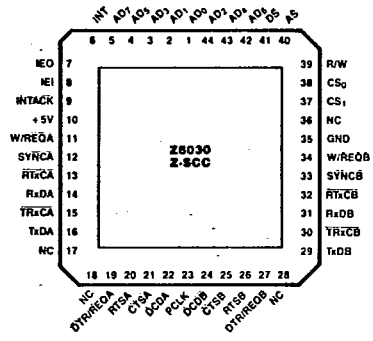

Figure 6. 44-pin Chip Carrier, Pin Assignments

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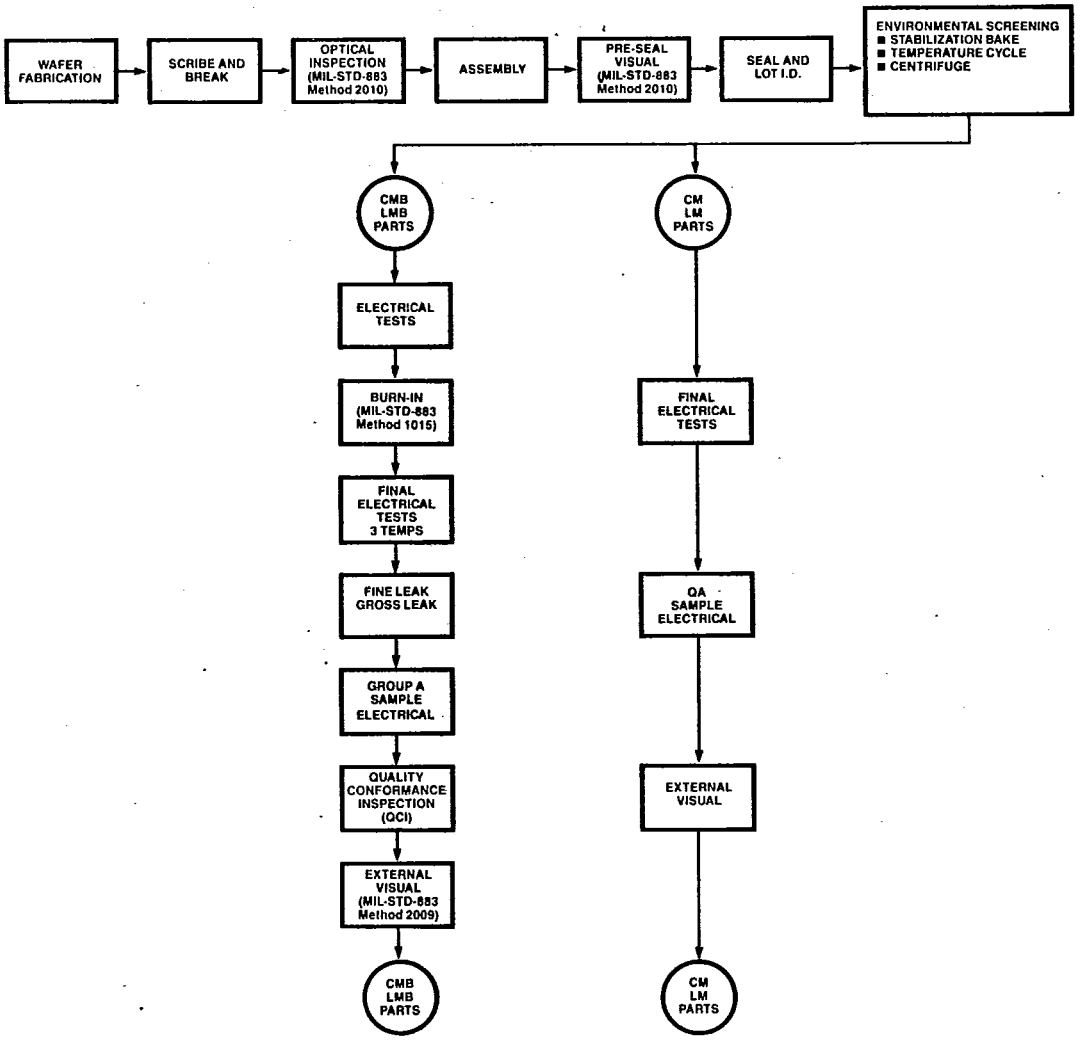
MIL-STD-883 MILITARY PROCESSED PRODUCT

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/ Quality Conformance testing required.

Zilog Military Product Flow



T-75-37-07

Table I
MIL-STD-883 Class B Screening Requirements
Method 5004

Test	Mil-Std-883 Method	Test Condition	Requirement
Internal Visual	2010	Condition B	100%
Stabilization Bake	1008	Condition C	100%
Temperature Cycle	1010	Condition C	100%
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 1), Y_1 Axis Only	100%
Initial Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
Burn-In	1015	Condition D(Note 2), 160 hours, T_A = +125°C	100%
Interim Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
PDA Calculation		PDA = 5%	100%
Final Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +125°C, −55°C Functional, Switching/AC T_C = +25°C	100%
Fine Leak	1014	Condition A_2	100%
Gross Leak	1014	Condition C	100%
Quality Conformance Inspection (QCI)			
Group A Each Inspection Lot	5005	(See Table II)	Sample
Group B Every Week	5005	(See Table III)	Sample
Group C Periodically(Note 3)	5005	(See Table IV)	Sample
Group D Periodically(Note 3)	5005	(See Table V)	Sample
External Visual	2009		100%
QA—Ship			100%

NOTES:
1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).

Table II Group A
Sample Electrical Tests
MIL-STD-883 Method 5005

Subgroup	Tests	Temperature (T_C)	LTPD Max Accept = 2
Subgroup 1	Static/DC	+25°C	2
Subgroup 2	Static/DC	+125°C	3
Subgroup 3	Static/DC	−55°C	5
Subgroup 7	Functional	+25°C	2
Subgroup 8	Functional	−55°C and +125°C	5
Subgroup 9	Switching/AC	+25°C	2
Subgroup 10	Switching/AC	+125°C	3
Subgroup 11	Switching/AC	−55°C	5

NOTES:
- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

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Table III Group B

Sample Test Performed Every Week to Test Construction and Insure Integrity of Assembly Process. MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1 Physical Dimensions	2016		2/0
Subgroup 2 Resistance to Solvents	2015		4/0
Subgroup 3 Solderability	2003	Solder Temperature +245°C ± 5°C	15(Note 1)
Subgroup 4 Internal Visual and Mechanical	2014		1/0
Subgroup 5 Bond Strength	2011	C	15(Note 2)
Subgroup 6(Note 3) Internal Water Vapor Content	1018	1000 ppm. maximum at +100°C	3/0 or 5/1
Subgroup 7(Note 4) Seal 7a) Fine Leak 7b) Gross Leak	1014	 7a) A_2 7b) C	5
Subgroup 8(Note 5) Electrostatic Discharge Sensitivity	3015	Zilog Military Electrical Specification Static/DC T_C = +25°C A = 20-2000V B = >2000V Zilog Military Electrical Specification Static/DC T_C = +25°C	15/0

NOTES:
1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

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Table IV Group C

Sample Test Performed Periodically to Verify Integrity of the Die.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Steady State Operating Life	1005	Condition D(Note 1), 1000 hours at +125°C	5
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 2			
Temperature Cycle	1010	Condition C	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	
Seal	1014		15
2a) Fine Leak		2a) Condition A_2	
2b) Gross Leak		2b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	

NOTE:
1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.

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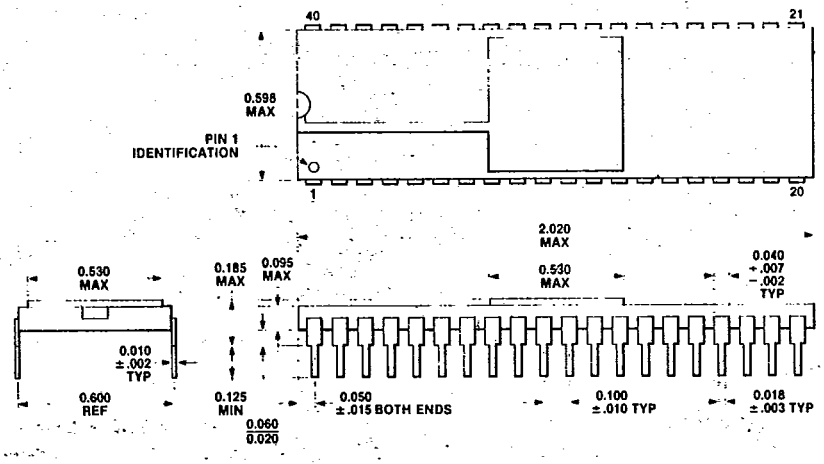
Table V Group D

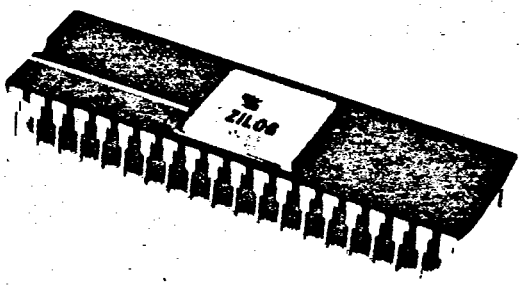
Sample Test Performed Periodically to Insure Integrity of the Package.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Condition B_2 or D(Note 1)	15
Subgroup 3			
Thermal Shock	1011	Condition B minimum, 15 cycles minimum	
Temperature Cycling	1010	Condition C, 100 cycles minimum	15
Moisture Resistance	1004		
Seal	1014		
3a) Fine Leak		3a) Condition A_2	
3b) Gross Leak		3b) Condition C	
Visual Examination	1004 or 1010		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 4			
Mechanical Shock	2002	Condition B minimum	
Vibration Variable Frequency	2007	Condition A minimum	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	15
Seal	1014		
4a) Fine Leak		4a) Condition A_2	
4b) Gross Leak		4b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 5			
Salt Atmosphere	1009	Condition A minimum	
Seal	1014		15
5a) Fine Leak		5a) Condition A_2	
5b) Gross Leak		5b) Condition C	
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm. maximum water content at +100°C	3/0 or 5/1
Subgroup 7(Note 3)			
Adhesion of Lead Finish	2025		15(Note 4)
Subgroup 8(Note 5)			
Lid Torque	2024		5/0

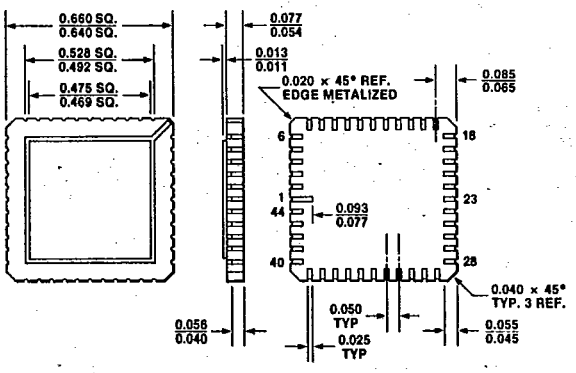
NOTES:
1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

PACKAGE INFORMATION





40-Pin Dual-In-Line Package (DIP), Ceramic



44-Pin Leadless Chip Carrier (LCC), Ceramic, Jedec Type C

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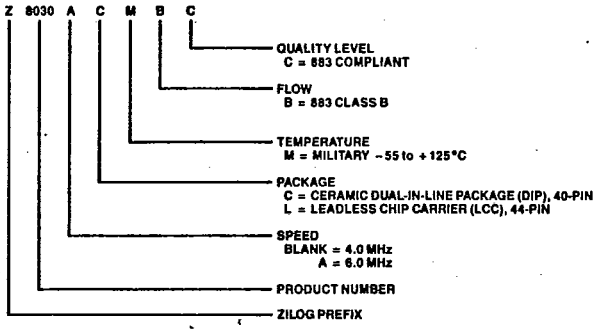
ZILOG ORDERING INFORMATION



AVAILABLE MILITARY PRODUCTS

Z8030 Z-SCC, 4.0 MHz		Z8030 Z-SCC, 6.0 MHz	
40-pin DIP	**44-pin LCC**	**40-pin DIP**	**44-pin LCC**
Z8030 CM	Z8030 LM	Z8030A CM	Z8030A LM
Z8030 CMBC	Z8030 LMBC	Z8030A CMBC	Z8030A LMBC