# Z8031 Z8000® Z-ASCC Asynchronous Serial Communications Controller

Zilog

## Product Specification

April 1985



**Features**

- Two independent, 0 to 1M bit/second, full-duplex channels, each with a separate crystal oscillator and baud rate generator.
- Programmable for NRZ, NRZI, or FM data encoding.
- Local Loopback and Auto Echo modes.
- Asynchronous communications with five to eight bits per character and one, one and one-half, or two stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection.

**General Description**

The Z8031 Z-ASCC Asynchronous Serial Communications Controller is a dual-channel data communications peripheral designed for use with the Zilog Z-BUS. The Z-ASCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators and crystal oscillators that dramatically reduce the need for external logic.

The Z-ASCC has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The Z-BUS daisy-chain interrupt hierarchy is also supported—as is standard for Zilog peripheral components.

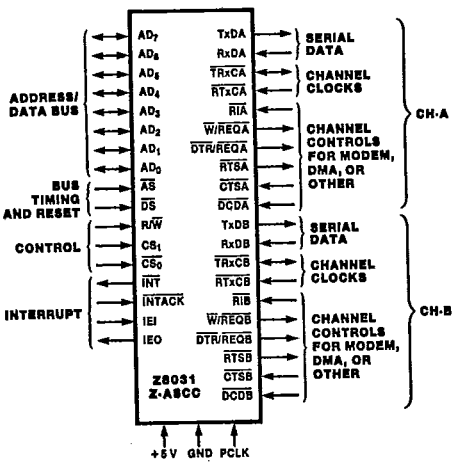


Figure 1. Pin Functions

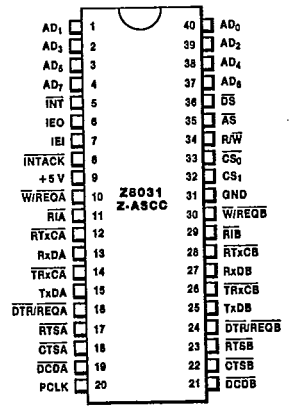


Figure 2a. 40-Pin Dual-In-Line Package (DIP), Pin Assignments

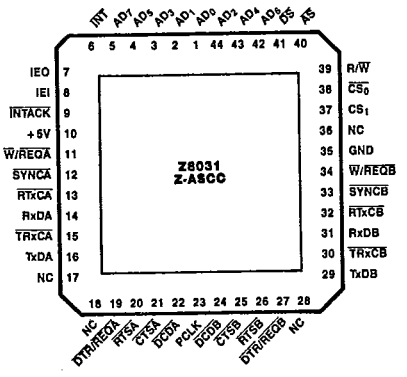


Figure 2b. 44-Pin Chip Carrier, Pin Assignments

**Pin Description**

The following section describes the pin functions of the Z-ASCC. Figures 1 and 2 detail the respective pin functions and pin assignments.

**$AD_0$-$AD_7$.** *Address/Data Bus* (bidirectional, active High, 3-state). These multiplexed lines carry register addresses to the Z-ASCC as well as data or control information to and from the Z-ASCC.

**$\overline{AS}$.** *Address Strobe* (input, active Low). Addresses on $AD_0$-$AD_7$ are latched by the rising edge of this signal.

**$\overline{CS_0}$.** *Chip Select 0* (input, active Low). This signal is latched concurrently with the addresses on $AD_0$-$AD_7$ and must be active for the intended bus transaction to occur.

**$CS_1$.** *Chip Select 1* (input, active High). This second select signal must also be active before the intended bus transaction can occur. $CS_1$ must remain active throughout the transaction.

**$\overline{CTSA}$, $\overline{CTSB}$.** *Clear to Send* (inputs, active Low). If these pins are programmed as Auto Enables, a Low on the inputs enables their respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The Z-ASCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

**$\overline{DCDA}$, $\overline{DCDB}$.** *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The Z-ASCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

**$\overline{DS}$.** *Data Strobe* (input, active Low). This signal provides timing for the transfer of data into and out of the Z-ASCC. If $\overline{AS}$ and $\overline{DS}$ coincide, this is interpreted as a reset.

**$\overline{DTR}/\overline{REQA}$, $\overline{DTR}/\overline{REQB}$.** *Data Terminal Ready/Request* (outputs, active Low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request lines for a DMA controller.

**IEI.** *Interrupt Enable In* (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

**IEO.** *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing a Z-ASCC interrupt or the Z-ASCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

**$\overline{INT}$.** *Interrupt Request* (output, open-drain, active Low). This signal is activated when the Z-ASCC requests an interrupt.

**$\overline{INTACK}$.** *Interrupt Acknowledge* (input, active Low). This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the Z-ASCC interrupt daisy chain settles. When $\overline{DS}$ becomes active, the Z-ASCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of $\overline{AS}$.

**PCLK.** *Clock* (input). This is the master Z-ASCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock, although the frequency of this clock must be at least 90% of the CPU clock frequency for a Z8000. PCLK is a TTL level signal.

**RxDA, RxDB.** *Receive Data* (inputs, active High). These input signals receive serial data at standard TTL levels.

**$\overline{RIA}$, $\overline{RIB}$.** *Ring Indicator* (inputs, active Low). These pins can act either as inputs or as part of the crystal oscillator circuit.

In normal operation (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Ring Indicator status bits in Read Register 0 (Figure 8) but have no other function.

**$\overline{RTxCA}$, $\overline{RTxCB}$.** *Receive/Transmit Clocks* (inputs, active Low). These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock of the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective $\overline{RI}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in Asynchronous modes.

**$\overline{RTSA}$, $\overline{RTSB}$.** *Request To Send* (outputs, active Low). When the Request To Send (RTS) bit in Write Register 5 (Figure 9) is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset and Auto Enable is on, the signal goes High after the transmitter is empty. With Auto Enable off, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

**R/$\overline{W}$.** *Read/Write* (input). This signal specifies whether the operation to be performed is a read or a write.

**TxDA, TxDB.** *Transmit Data* (outputs, active High). These output signals transmit serial data at standard TTL levels.

**Pin Description** (Continued)

**$\overline{\text{TRxCA}}$, $\overline{\text{TRxCB}}$.** *Transmit/Receive Clocks* (inputs or outputs, active Low). These pins can be programmed in several different modes of operation. $\overline{\text{TRxC}}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

**$\overline{\text{W}}/\overline{\text{REQA}}$, $\overline{\text{W}}/\overline{\text{REQB}}$.** *Wait/Request* (outputs, open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function). These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the Z-ASCC data rate. The reset state is Wait.

**Functional Description**

The functional capabilities of the Z-ASCC can be described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a Z8000 peripheral, it interacts with the CPU and other peripheral circuits and is part of the system interrupt structure.

**Data Communications Capabilities.** The Z-ASCC provides two independent full-duplex channels programmable for use in any common Asynchronous data communication protocol. Figure 3 and the following description briefly detail this protocol.

*Asynchronous Modes.* Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half, or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 1). If the Low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The Z-ASCC does not require symmetric transmit and receive clock signals—a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs.

**Baud Rate Generator.** Each channel in the Z-ASCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching 0, the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the Digital Phase-Locked Loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{\text{TRxC}}$ pin, the output of the baud rate generator may be echoed out via the $\overline{\text{TRxC}}$ pin.

The following formula relates the time constant to the baud rate (the baud rate is in bits/second and the BR clock period is in seconds):

$$\text{time constant} = \frac{\text{PCLK}}{2\,(\text{clock factor})\,(\text{baud})} - 2$$

**Digital Phase-Locked Loop.** The Z-ASCC contains a Digital Phase-Locked Loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the Z-ASCC receive clock, the transmit clock, or both.

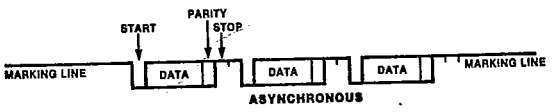


**Figure 3. Z-ASCC Protocol**

**Functional Description** (Continued)

For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the $\overline{\text{RTxC}}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the Z-ASCC via the $\overline{\text{TRxC}}$ pin (if this pin is not being used as an input).

**Data Encoding** The Z-ASCC may be programmed to encode and decode the serial data in four different ways (Figure 4). In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level. In FM1 (more properly, bi-phase mark) a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the Z-ASCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0 the bit is a 1.

**Auto Echo and Local Loopback.** The Z-ASCC is capable of automatically echoing everything it receives. In Auto Echo mode, RxD is connected to TxD internally. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{\text{CTS}}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and $\overline{\text{WAIT/REQUEST}}$ on transmit.

The Z-ASCC is also capable of Local Loopback. In this mode TxD is connected to RxD internally, just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works with NRZ, NRZI or FM coding of the data stream.

**I/O Interface Capabilities.** The Z-ASCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

**Polling.** All interrupts are disabled. Three status registers in the Z-ASCC are automatically updated whenever any function is performed. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the

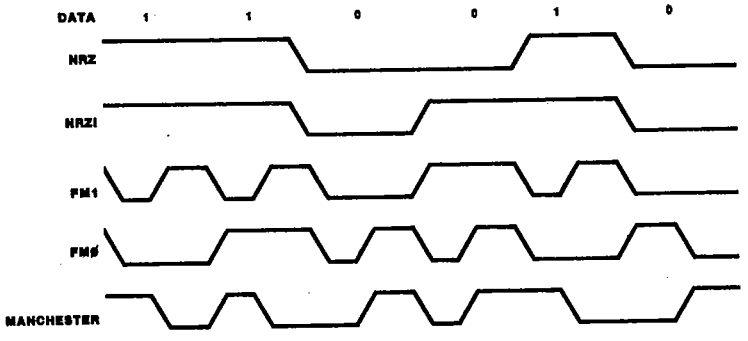


**Figure 4. Data Encoding Methods**

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**Functional Description** (Continued)

Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

**Interrupts.** The Z-ASCC interrupt scheme conforms to the Z-BUS specification. When a Z-ASCC responds to an Interrupt Acknowledge signal ($\overline{INTACK}$) from the CPU, an interrupt vector may be placed on the A/D bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 8 and 9).

To speed interrupt response time, the Z-ASCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the Z-ASCC (Transmit, Receive, and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write only.

The other two bits are related to the Z-BUS interrupt priority chain (Figure 5). The Z-ASCC may request an interrupt only when no higher priority device is requesting one, e.g., when IEI is High. If the device in question requests an interrupt, it pulls down $\overline{INT}$. The CPU then responds with $\overline{INTACK}$, and the interrupting device places the vector on the A/D bus.

In the Z-ASCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the $\overline{INT}$ output is pulled Low, requesting an interrupt. In the Z-ASCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP is set two or three $\overline{AS}$ cycles after the interrupt condition occurs. Two or three $\overline{AS}$ rising edges are required from the time an interrupt condition occurs until $\overline{INT}$ is activated. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the Z-ASCC and external to the Z-ASCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the Z-ASCC being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive, and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receiver, Transmit, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the receiver can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive Condition.
- Interrupt on All Receive Characters or Special Receive Condition.
- Interrupt on Special Receive Condition Only.

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is receiver overrun, and, optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary receive character available interrupt only in the status placed in the vector during the Interrupt Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive Conditions any time after the first receive character interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{RI}$ pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, or a zero count in the baud rate generator, or by the detection of a Break.



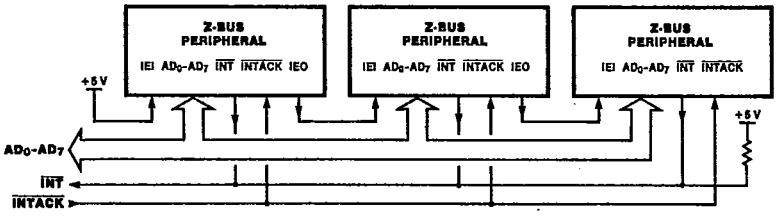


**Figure 5. Z-BUS Interrupt Schedule**

**Functional Description** (Continued)

**CPU/DMA Block Transfer.** The Z-ASCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the $\overline{\text{WAIT/REQUEST}}$ output in conjunction with the Wait/Request bits in WR1. The $\overline{\text{WAIT/REQUEST}}$ output can be defined under software control as a $\overline{\text{WAIT}}$ line in the CPU Block Transfer mode or as a $\overline{\text{REQUEST}}$ line in the DMA Block Transfer mode.

To a DMA controller, the Z-ASCC $\overline{\text{REQUEST}}$ output indicates that the Z-ASCC is ready to transfer data to or from memory. To the CPU, the $\overline{\text{WAIT}}$ line indicates that the Z-ASCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{\text{DTR/REQUEST}}$ line allows full-duplex operation under DMA control.

**Architecture**

The Z-ASCC internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to the Zilog Z-BUS. Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface to modems or other external devices (Figure 6).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the

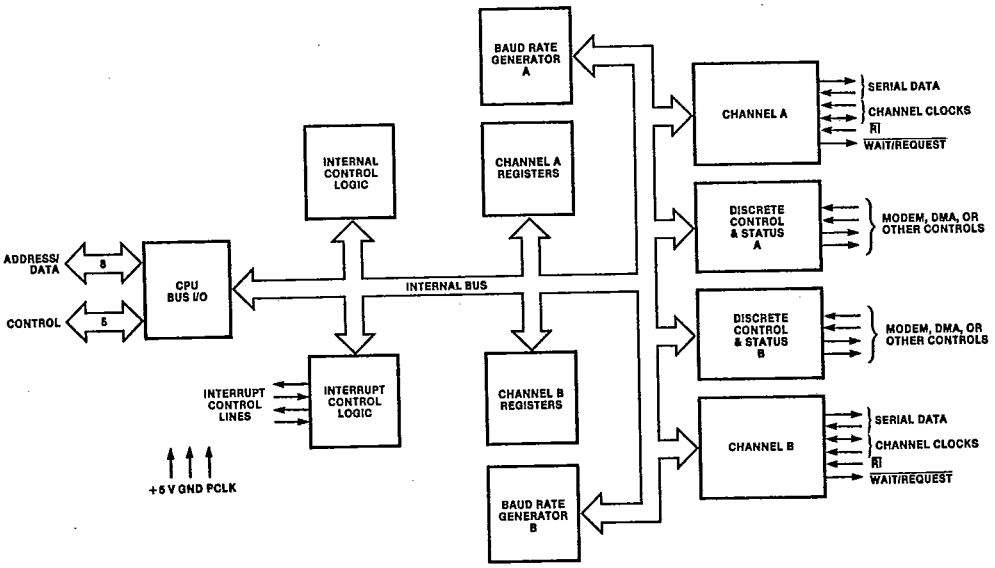


**Figure 6. Block Diagram of Z-ASCC Architecture**



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## Architecture
(Continued)

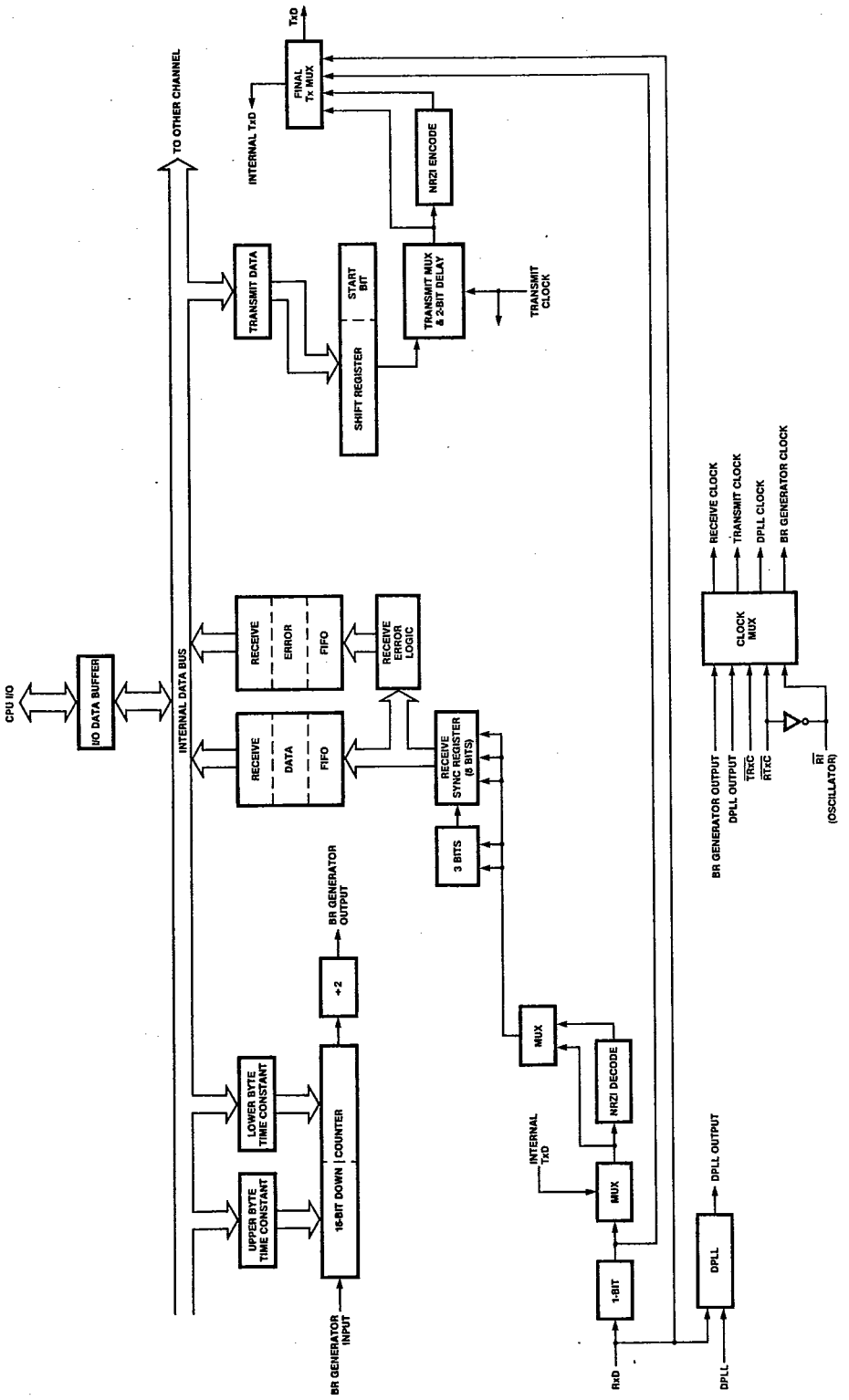


Figure 7. Data Path

**Architecture** (Continued)

baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write-only Master Interrupt Control register and three read registers: one containing the vector with status infomation (Channel B only), one containing the vector without status (Channel A only), and one containing the Interrupt Pending bits (Channel A only).

The registers for each channel are designated as follows:

WR0–WR15 — Write Registers 0-5, 8-15.

RR0–RR3, RR10, RR12, RR13, RR15 — Read Registers 0 through 3, 10, 12, 13, 15.

Table 1 lists the functions assigned to each read or write register. The Z-ASCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

**Data Path.** The transmit and receive data path illustrated in Figure 7 is identical for both channels. The receiver has three 8-bit buffer registers in an FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high speed data. Incoming data is routed through one of several paths depending on the selected mode (the character length determines the data path).

The transmitter has an 8-bit Transmit Data buffer register loaded from the internal data bus and an 11-bit Transmit Shift register that is loaded from the Transmit Data register.

| Read Register Functions | |
|---|---|
| RR0 | Transmit/Receive buffer status and External status |
| RR1 | Special Receive Condition status |
| RR2 | Modified interrupt vector (Channel B only) Unmodified interrupt vector (Channel A only) |
| RR3 | Interrupt Pending bits (Channel A only) |
| RR8 | Receive buffer |
| RR10 | Miscellaneous status |
| RR12 | Lower byte of baud rate generator time constant |
| RR13 | Upper byte of baud rate generator time constant |
| RR15 | External/Status interrupt information |
| **Write Register Functions** | |
| WR0 | CRC initialize, initialization commands for the various modes, shift right/shift left command |
| WR1 | Transmit/Receive interrupt and data transfer mode definition |
| WR2 | Interrupt vector (accessed through either channel) |
| WR3 | Receive parameters and control |
| WR4 | Transmit/Receive miscellaneous parameters and modes |
| WR5 | Transmit parameters and controls |
| WR8 | Transmit buffer |
| WR9 | Master interrupt control and reset (accessed through either channel) |
| WR10 | Miscellaneous transmitter/receiver control bits |
| WR11 | Clock mode control |
| WR12 | Lower byte of baud rate generator time constant |
| WR13 | Upper byte of baud rate generator time constant |
| WR14 | Miscellaneous control bits |
| WR15 | External/Status interrupt control |

**Table 1. Read and Write Register Functions**

**Programming**

The Z-ASCC contains 11 write registers in each channel that are programmed by the system separately to configure the functional personality of the channels. All of the registers in the Z-ASCC are directly addressable. How the Z-ASCC decodes the address placed on the address/data bus at the beginning of a Read or Write cycle is controlled by a command issued in WR0B. In the shift right mode, the channel select A/$\overline{B}$ is taken from $AD_0$ and the state of $AD_5$ is ignored. In the shift left mode, A/$\overline{B}$ is taken from $AD_5$ and the state of $AD_0$ is ignored. $AD_7$ and $AD_6$ are always ignored as address bits and the register address itself occupies $AD_4$ - $AD_1$.

The system program first issues a series of commands to initialize the basic mode of operation. For example, the character length, clock rate, number of stop bits, even or odd parity might be set first. Then the Interrupt mode would be set, and finally, receiver or transmitter enable.

**Programming** (Continued)

**Read Registers.** The Z-ASCC contains eight read registers (actually nine, counting the receive buffer [RR8]) in each channel. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). Figure 8 shows the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).



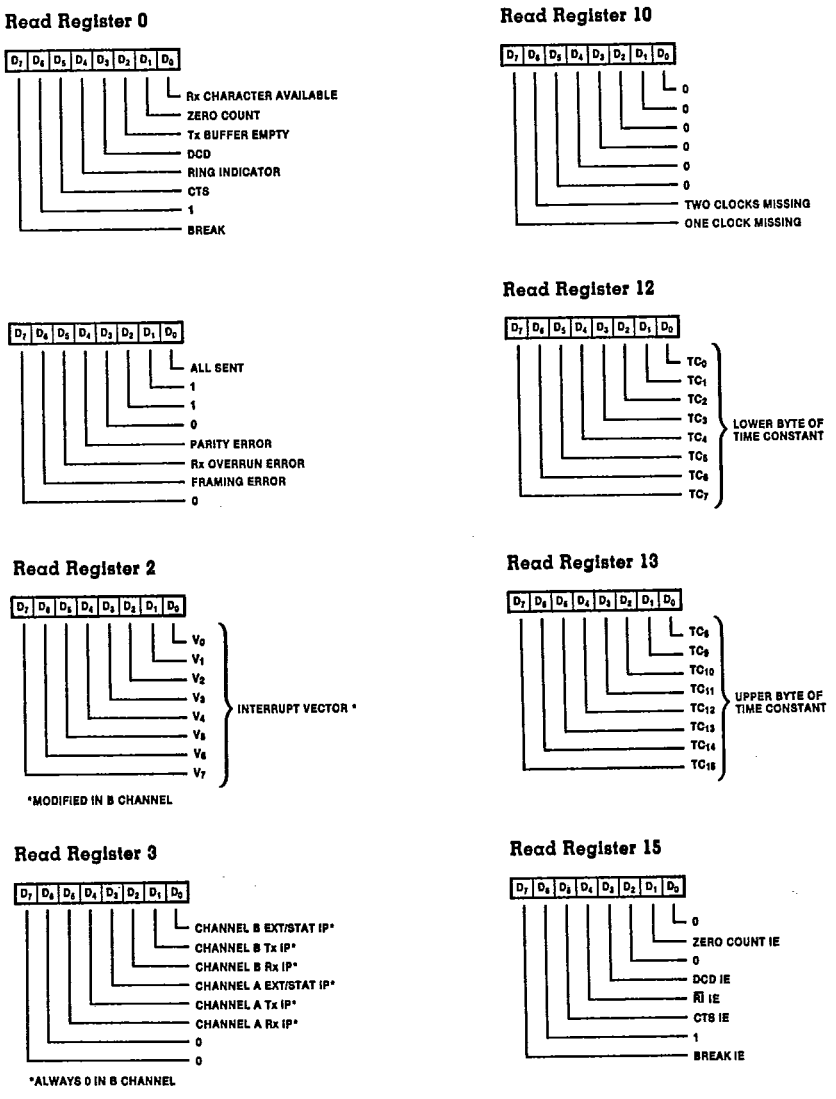


**Figure 8. Read Register Bit Functions**

**Programming** (Continued)

**Write Registers.** The Z-ASCC contains 11 write registers (12 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 9 shows the format of each write register.

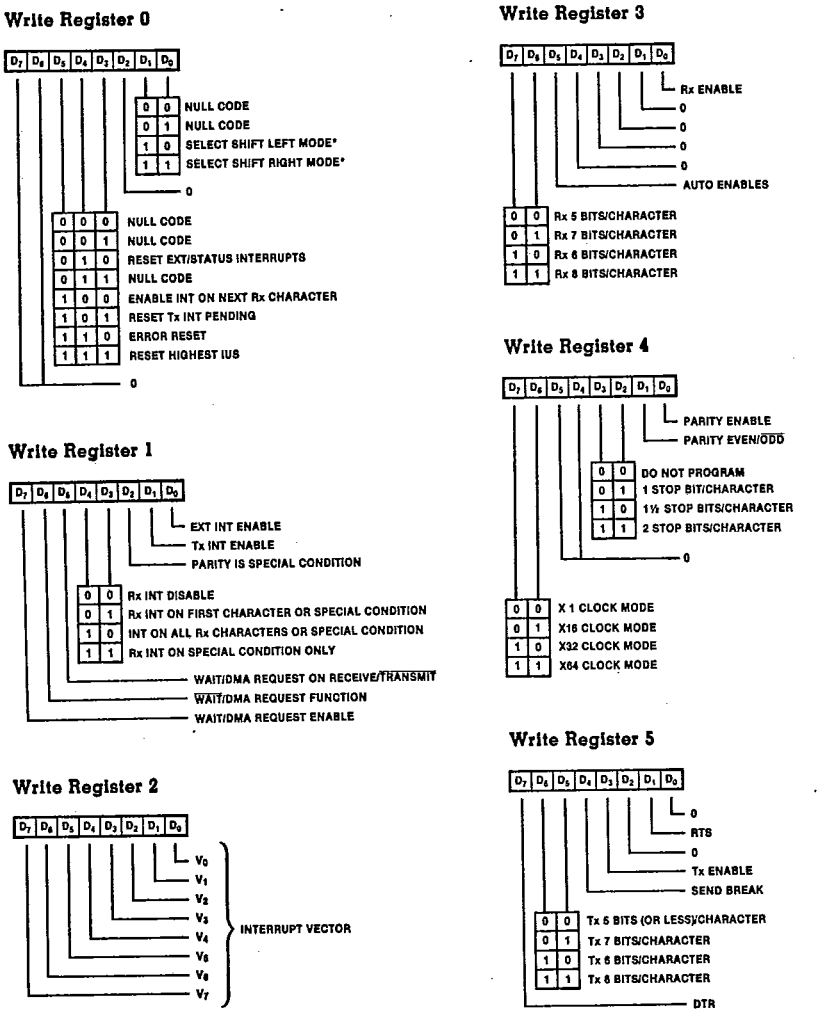


**Figure 9. Write Register Bit Functions**



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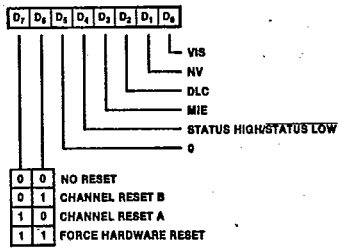
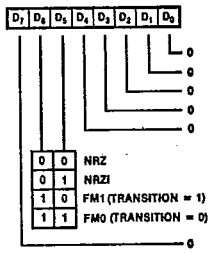
**Programming** (Continued)

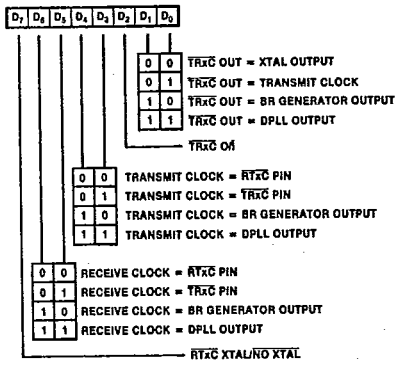
### Write Register 9



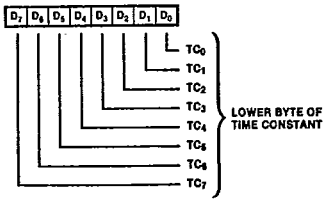

### Writer Register 10



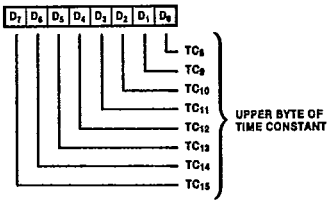

### Write Register 11



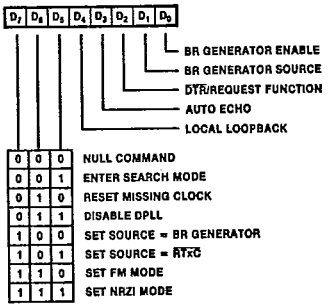

### Write Register 12




### Write Register 13




### Write Register 14




### Write Register 15

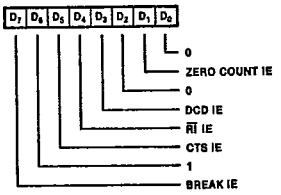



**Figure 9. Write Register Bit Functions** (Continued)

Z8031 Z-ASC

## Timing

The Z-ASCC generates internal control signals from $\overline{AS}$ and $\overline{DS}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{AS}$ and $\overline{DS}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the Z-ASCC. The recovery time required for proper operation is specified from the rising edge of $\overline{DS}$ in the first transaction involving the Z-ASCC to the falling edge of $\overline{DS}$ in the second transaction involving the Z-ASCC. This time must be at least 6 PCLK cycles plus 200 ns.

**Read Cycle Timing.** Figure 10 illustrates Read cycle timing. The address on $AD_0$–$AD_7$ and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be High to indicate a Read cycle. $CS_1$ must also be High for the Read cycle to occur. The data bus drivers in the Z-ASCC are then enabled while $\overline{DS}$ is Low.

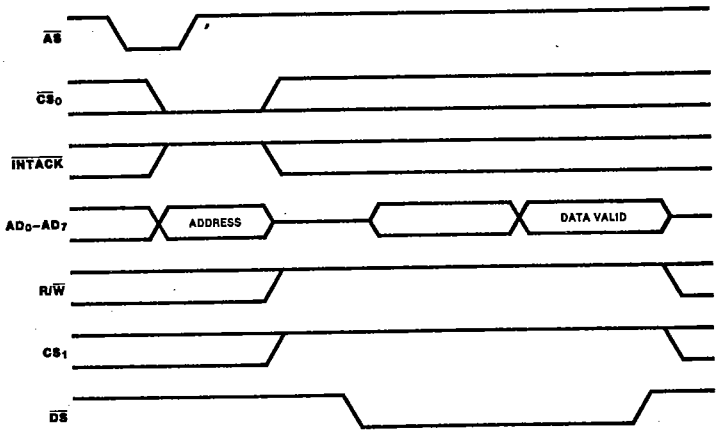



Figure 10. Read Cycle Timing

**Write Cycle Timing.** Figure 11 illustrates Write cycle timing. The address on $AD_0$–$AD_7$ and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be Low to indicate a Write cycle. $CS_1$ must be High for the Write cycle to occur. $\overline{DS}$ Low strobes the data into the Z-ASCC.

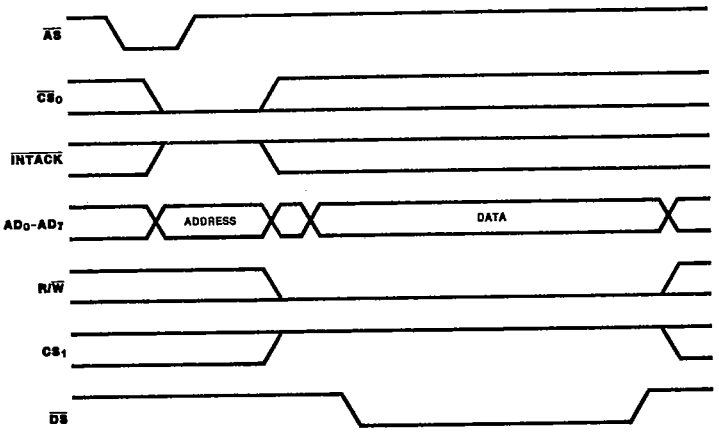



Figure 11. Write Cycle Timing

**Interrupt Acknowledge Cycle Timing.** Figure 12 illustrates Interrupt Acknowledge cycle timing. The address on $AD_0$–$AD_7$ and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. However, if $\overline{INTACK}$ is Low, the address and $\overline{CS_0}$ are ignored. The state of the R/$\overline{W}$ and $CS_1$ are also ignored for the duration of the Interrupt Acknowledge

**Timing** (Continued)

cycle. Between the rising edge of $\overline{AS}$ and the falling edge of $\overline{DS}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the Z-ASCC and IEI is High when $\overline{DS}$ falls, the Acknowledge cycle was intended for the Z-ASCC. In this case, the Z-ASCC may be programmed to respond to $\overline{DS}$ Low by placing its interrupt vector on $AD_0$–$AD_7$. It then sets the appropriate Interrupt-Under-Service latch internally.

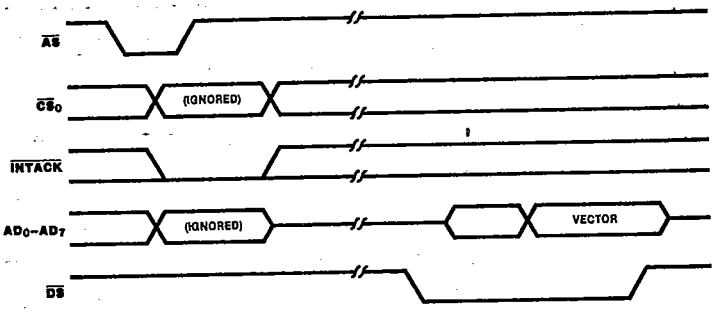



**Figure 12. Interrupt Acknowledge Cycle Timing**

**Absolute Maximum Ratings**

Voltages on all pins with respect to GND ..... −0.3V to +7.0V
Operating Ambient Temperature .....See Ordering Information
Storage Temperature..... −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Standard Test Conditions**

The DC characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- +4.75 V ≤ $V_{CC}$ ≤ +5.25 V
- GND = 0 V
- $T_A$ as specified in Ordering Information

All ac parameters assume a load capacitance of 50 pf max.

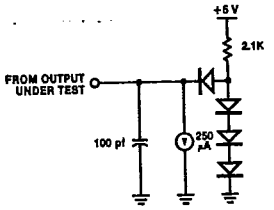



**Figure 13. Standard Test Load**

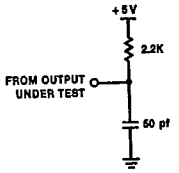



**Figure 14. Open-Drain Test Load**

**DC Characteristics**

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$+0.3 | V | |
| $V_{IL}$ | Input Low Voltage | -0.3 | 0.8 | V | |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH}$ = −250 µA |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = +2.0 mA |
| $I_{IL}$ | Input Leakage | | ±10.0 | µA | 0.4 ≤ $V_{IN}$ ≤ +2.4V |
| $I_{OL}$ | Output Leakage | | ±10.0 | µA | 0.4 ≤ $V_{OUT}$ ≤ +2.4V |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 250 | mA | |

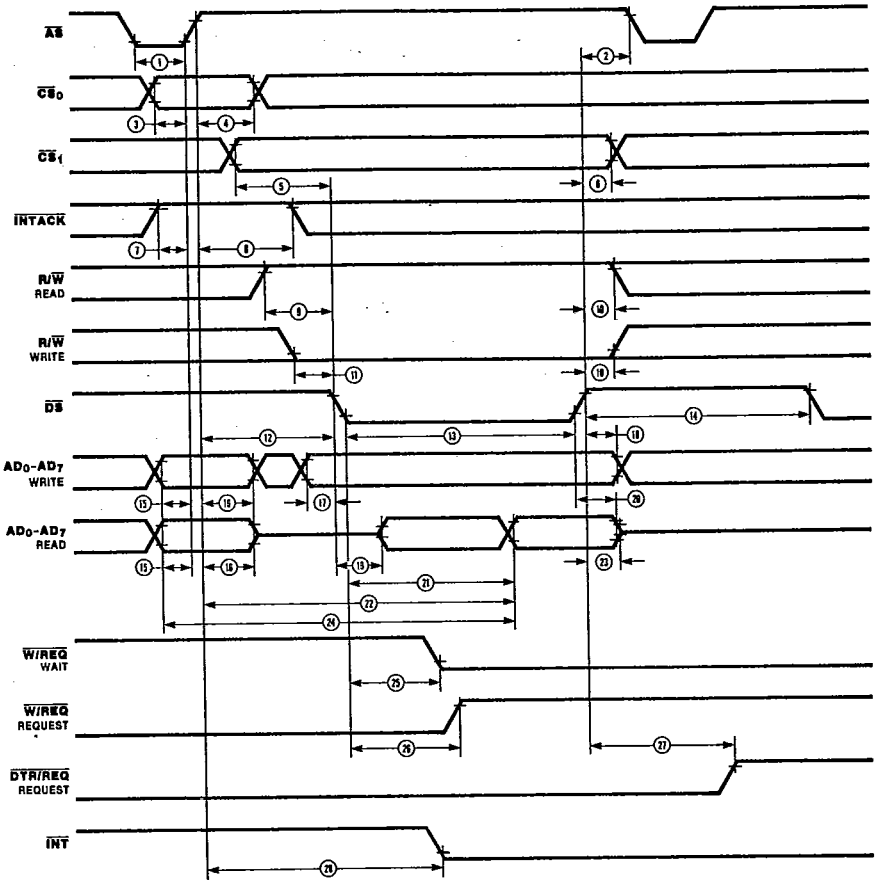
$V_{CC}$ = 5 V ± 5% unless otherwise specified, over specified temperature range.

**Capacitance**

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pf | |
| $C_{OUT}$ | Output Capacitance | | 15 | pf | |
| $C_{I/O}$ | Bidirectional Capacitance | | 20 | pf | |

f = 1 MHz, over specified temperature range.
Unmeasured pins returned to ground.

## Read and Write Timing




| No. | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 1 | TwAS | $\overline{AS}$ Low Width | 70 | | 50 | | |
| 2 | TdDS(AS) | $\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay | 50 | | 25 | | |
| 3 | TsCSO(AS) | $\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time | 0 | | 0 | | 1 |
| 4 | ThCSO(AS) | $\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time | 60 | | 40 | | 1 |
| 5 | TsCS1(DS) | $CS_1$ to $\overline{DS}$ ↓ Setup Time | 100 | | 80 | | 1 |
| 6 | ThCS1(DS) | $CS_1$ to $\overline{DS}$ ↑ Hold Time | 55 | | 40 | | 1 |
| 7 | TsIA(AS) | $\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time | 0 | | 0 | | |
| 8 | ThIA(AS) | $\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time | 250 | | 250 | | |
| 9 | TsRWR(DS) | R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time | 100 | | 80 | | |
| 10 | ThRW(DS) | R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time | 55 | | 40 | | |
| 11 | TsRWW(DS) | R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time | 0 | | 0 | | |
| 12 | TdAS(DS) | $\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay | 60 | | 40 | | |
| 13 | TwDS1 | $\overline{DS}$ Low Width | 390 | | 250 | | |
| 14 | TrC | Valid Access Recovery Time | 6TcPC +200 | | 6TcPC +130 | | 2 |
| 15 | TsA(AS) | Address to $\overline{AS}$ ↑ Setup Time | 30 | | 10 | | 1 |
| 16 | ThA(AS) | Address to $\overline{AS}$ ↑ Hold Time | 50 | | 30 | | 1 |
| 17 | TsDW(DS) | Write Data to $\overline{DS}$ ↓ Setup Time | 30 | | 20 | | |
| 18 | ThDW(DS) | Write Data to $\overline{DS}$ ↑ Hold Time | 30 | | 20 | | |
| 19 | TdDS(DA) | $\overline{DS}$ ↓ to Data Active Delay | 0 | | 0 | | |
| 20 | TdDSr(DR) | $\overline{DS}$ ↑ to Read Data Not Valid Delay | 0 | | 0 | | |
| 21 | TdDSf(DR) | $\overline{DS}$ ↓ to Read Data Valid Delay | | 250 | | 180 | |
| 22 | TdAS(DR) | $\overline{AS}$ ↑ to Read Data Valid Delay | | 520 | | 335 | |

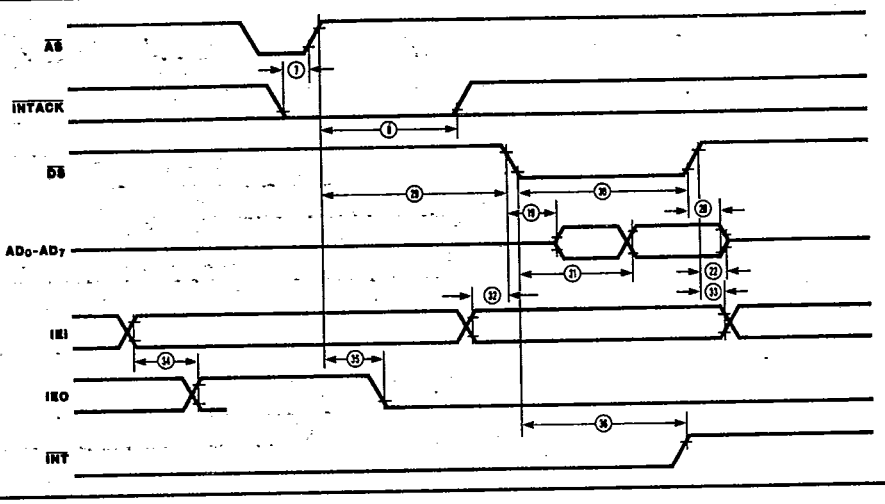
NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the Z-ASCC.

*Timings are preliminary and subject to change.
† Units in nanoseconds (ns).

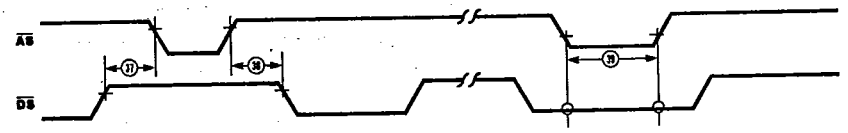


2016-015

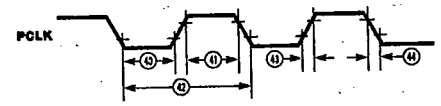
**Interrupt Acknowledge Timing**




**Reset Timing**




**Cycle Timing**




| No. | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 23 | TdDS(DRz) | $\overline{DS}$ ↑ to Read Data Float Delay | | 70 | | 45 | 3 |
| 24 | TdA(DR) | Address Required Valid to Read Data Valid Delay | | 570 | | 420 | |
| 25 | TdDS(W) | $\overline{DS}$ ↓ to Wait Valid Delay | | 240 | | 200 | 4 |
| 26 | TdDSf(REQ) | $\overline{DS}$ ↓ to $\overline{W/REQ}$ Not Valid Delay | | 240 | | 200 | |
| 27 | TdDSr(REQ) | $\overline{DS}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay | | 5TcPC +300 | | 5TcPC +250 | |
| 28 | TdAS(INT) | $\overline{AS}$ ↑ to $\overline{INT}$ Valid Delay | | 500 | | 500 | 4 |
| 29 | TdAS(DSA) | $\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay | | | | | 5 |
| 30 | TwDSA | $\overline{DS}$ (Acknowledge) Low Width | 390 | | 250 | | |
| 31 | TdDSA(DR) | $\overline{DS}$ ↓ (Acknowledge) to Read Data Valid Delay | | 250 | | 180 | |
| 32 | TsIEI(DSA) | IEI to $\overline{DS}$ ↓ (Acknowledge) Setup Time | 120 | | 100 | | |
| 33 | ThIEI(DSA) | IEI to $\overline{DS}$ ↑ (Acknowledge) Hold Time | 0 | | 0 | | |
| 34 | TdIEI(IEO) | IEI to IEO Delay | | 120 | | 100 | |
| 35 | TdAS(IEO) | $\overline{AS}$ ↑ to IEO Delay | | 250 | | 250 | 6 |
| 36 | TdDSA(INT) | $\overline{DS}$ ↓ (Acknowledge) to $\overline{INT}$ Inactive Delay | | 500 | | 500 | 4 |
| 37 | TdDS(ASQ) | $\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay for No Reset | 30 | | 15 | | |
| 38 | TdASQ(DS) | $\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay for No Reset | 30 | | 30 | | |
| 39 | TwRES | $\overline{AS}$ and $\overline{DS}$ Coincident Low for Reset | 250 | | 250 | | 7 |
| 40 | TwPCl | PCLK Low Width | 105 | 2000 | 70 | 1000 | |
| 41 | TwPCh | PCLK High Width | 105 | 2000 | 70 | 1000 | |
| 42 | TcPC | PCLK Cycle Time | 250 | 4000 | 165 | 2000 | |
| 43 | TrPC | PCLK Rise Time | | 20 | | 15 | |
| 44 | TfPC | PCLK Fall Time | | 20 | | 10 | |

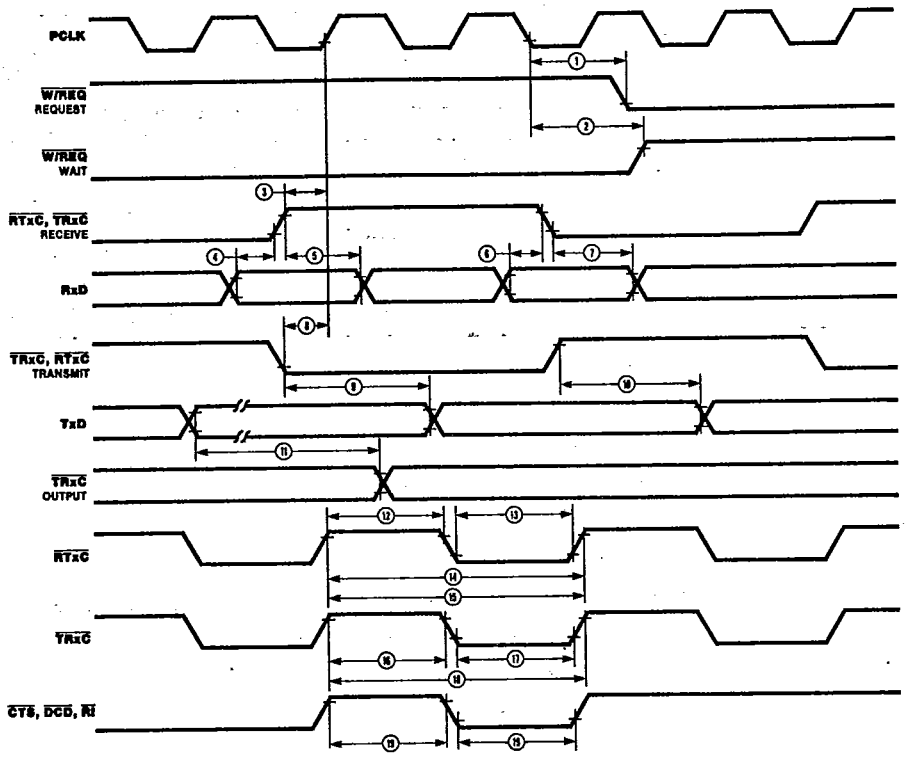
NOTES:

3. Float delay is defined as the time required for a ±0.5 V change in the output with a maximum dc load and minimum ac load.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any Z-ASCC in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain, TsIEI(DSA) for the Z-ASCC, and TdIEI(IEO) for each device separating them in the daisy chain.
6. Parameter applies only to a Z-ASCC pulling $\overline{INT}$ Low at the beginning of the Interrupt Acknowledge transaction.
7. Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the Z-ASCC.

* Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

† Units in nanoseconds (ns).

## General Timing





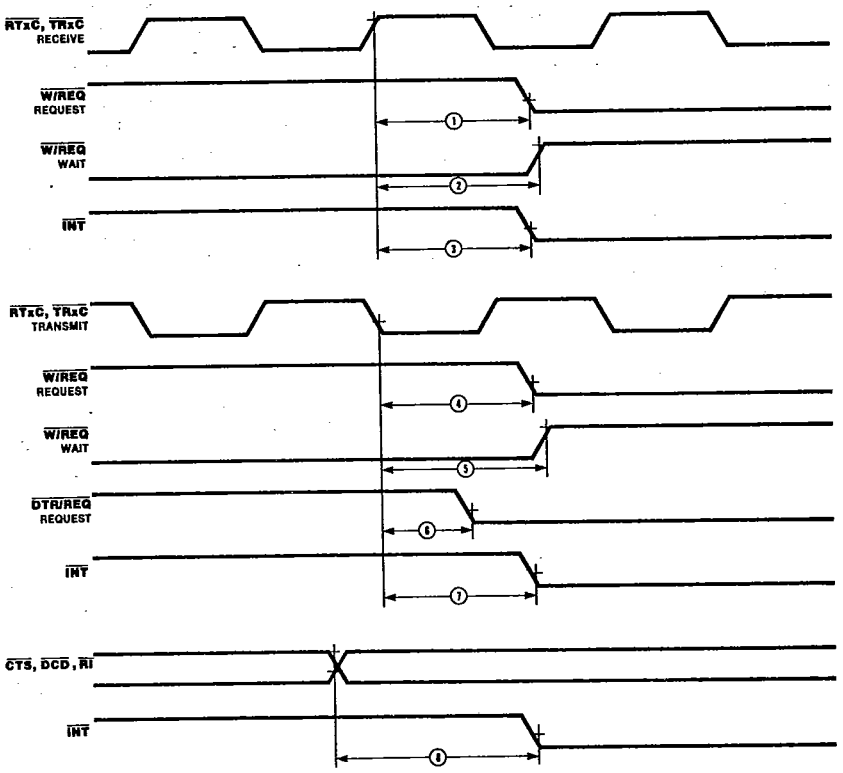

2245-007

| No. | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes*† |
|---|---|---|---|---|---|---|---|
| 1 | TdPC(REQ) | PCLK ↓ to $\overline{W/REQ}$ Valid | | 250 | | 250 | |
| 2 | TdPC(W) | PCLK ↓ to Wait Inactive Delay | | 350 | | 350 | |
| 3 | TsRXC(PC) | $\overline{RxC}$ ↑ to PCLK ↑ Setup Time (PCLK ÷ 4 case only) | 80 | TwPCl | 70 | TwPCl | 1,4 |
| 4 | TsRXD(RXCr) | RxD to $\overline{RxC}$ ↑ Setup Time (X1 Mode) | 0 | | 0 | | 1 |
| 5 | ThRXD(RXCr) | RxD to $\overline{RxC}$ ↑ Hold Time (X1 Mode) | 150 | | 150 | | 1 |
| 6 | TsRXD(RXCf) | RxD to $\overline{RxC}$ ↓ Setup Time (X1 Mode) | 0 | | 0 | | 1,5 |
| 7 | ThRXD(RXCf) | RxD to $\overline{RxC}$ ↓ Hold Time (X1 Mode) | 150 | | 150 | | 1,5 |
| 8 | TsTXC(PC) | $\overline{TxC}$ ↓ to PCLK ↑ Setup Time | 0 | | 0 | | 2,4 |
| 9 | TdTXCf(TXD) | $\overline{TxC}$ ↓ to TxD Delay (X1 Mode) | | 300 | | 300 | 2 |
| 10 | TdTXCr(TXD) | $\overline{TxC}$ ↑ to TxD Delay (X1 Mode) | | 300 | | 300 | 2,5 |
| 11 | TdTXD(TRX) | TxD to $\overline{TRxC}$ Delay (Send Clock Echo) | | | | | |
| 12 | TwRTXh | $\overline{RTxC}$ High Width | 180 | | 180 | | 6 |
| 13 | TwRTXl | $\overline{RTxC}$ Low Width | 180 | | 180 | | 6 |
| 14 | TcRTX | $\overline{RTxC}$ Cycle Time | 400 | | 400 | | 6 |
| 15 | TcRTXX | Crystal Oscillator Period | 250 | 1000 | 250 | 1000 | 3 |
| 16 | TwTRXh | $\overline{TRxC}$ High Width | 180 | | 180 | | 6 |
| 17 | TwTRXl | $\overline{TRxC}$ Low Width | 180 | | 180 | | 6 |
| 18 | TcTRX | $\overline{TRxC}$ Cycle Time | 400 | | 400 | | 6 |
| 19 | TwEXT | $\overline{DCD}$ or $\overline{CTS}$ or $\overline{RI}$ Pulse Width | 200 | | 200 | | |

NOTES:
1. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
2. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
3. Both $\overline{RTxC}$ and $\overline{RI}$ have 30 pF capacitors to the ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between $\overline{RxC}$ and PCLK or $\overline{TxC}$ and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.

* Timings are preliminary and subject to change.
† Units in nanoseconds (ns).

## System Timing




| No. | Symbol | Parameter | 4 MHz Min | 4 MHz Max | 6 MHz Min | 6 MHz Max | Notes* |
|---|---|---|---|---|---|---|---|
| 1 | TdRXC(REQ) | $\overline{RxC}$ ↑ to $\overline{W/REQ}$ Valid Delay | 8 | 12 | 8 | 12 | 2,4 |
| 2 | TdRXC(W) | $\overline{RxC}$ ↑ to Wait Inactive Delay | 8 | 12 | 8 | 12 | 1,2,4 |
| 3 | TdRXC(INT) | $\overline{RxC}$ ↑ $\overline{INT}$ Valid Delay | 8<br>+2 | 12<br>+3 | 8<br>+2 | 12<br>+3 | 1,2,4<br>5 |
| 4 | TdTXC(REQ) | $\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay | 5 | 8 | 5 | 8 | 3,4 |
| 5 | TdTXC(W) | $\overline{TxC}$ ↓ to Wait Inactive Delay | 5 | 8 | 5 | 8 | 1,3,4 |
| 6 | TdTXC(DRQ) | $\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay | 4 | 7 | 4 | 7 | 3,4 |
| 7 | TdTXC(INT) | $\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay | 4<br>+2 | 6<br>+3 | 4<br>+2 | 6<br>+3 | 1,3,4<br>5 |
| 8 | TdEXT(INT) | $\overline{DCD}$, $\overline{RI}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay | 2 | 3 | 2 | 3 | 1,5 |

NOTES:
1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
4. Units equal to $\overline{TcPC}$.
5. Units equal to $\overline{AS}$.

* Timings are preliminary and subject to change.

## ORDERING INFORMATION

**Z8031 Z-ASCC, 4.0 MHz**
**40-pin DIP**
Z8031 PS
Z8031 CS

**Z8031A Z-ASCC, 6.0 MHz**
**40-pin DIP**
Z8031A PS
Z8031A CS

**Z8031 Z-ASCC, 4.0 MHz**
**44-pin PCC**
Z8031 VS

**Z8031 Z-ASCC, 6.0 MHz**
**44-pin PCC**
Z8031A VS

### Codes

First letter is for package; second letter is for temperature.

C = Ceramic DIP
P = Plastic DIP
L = Ceramic LCC
V = Plastic PCC

R = Protopack
T = Low Profile Protopack
DIP = Dual-In-Line Package
LCC = Leadless Chip Carrier
PCC = Plastic Chip Carrier (Leaded)

TEMPERATURE
S = 0°C to +70°C
E = −40°C to +85°C
M*= −55°C to +125°C

FLOW
B = 883 Class B

Example: PS is a plastic DIP, 0°C to +70°C.

†Available soon.
*For Military Orders, contact your local Zilog Sales Office for Military Electrical Specifications.