Z8036 Military Z8000® Z-CIO Counter/Timer and Parallel I/O Unit

Zilog

Military Electrical Specification

July 1985

FEATURES

- Two independent 8-bit, double-buffered, bidirectional I/O ports plus a 4-bit special-purpose I/O port. I/O ports feature programmable polarity, programmable direction (Bit mode), "pulse catchers," and programmable open-drain outputs.
- Four handshake modes, including 3-Wire (like the IEEE-488).
- Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
- REQUEST/$\overline{\text{WAIT}}$ signal for high-speed data transfer.
- Three independent 16-bit counter/timers with up to four external access lines per counter/timer (count input, output, gate, and trigger), and three output duty cycles (pulsed, one-shot, and square-wave), programmable as retriggerable or nonretriggerable.
- Easy to use since all registers are read/write and directly addressable.

GENERAL DESCRIPTION

The Z8036 Z-CIO Counter/Timer and Parallel I/O element is a general-purpose peripheral circuit, satisfying most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers. Many programmable options tailor its configuration to specific applications.

The use of the device is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. In addition, each register is given its own unique address so that it can be accessed directly—no special sequential operations are required. The Z-CIO is directly Z-BUS compatible.

TIMING

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Read Cycle. The CPU places an address on the address/data bus. The more significant bits and status information are combined and decoded by external logic to provide two Chip Selects ($\overline{CS_0}$ and CS_1). Six bits of the least significant byte of the address are latched within the Z-CIO and used to specify a Z-CIO register. The data from the register specified is strobed onto the address/data bus when the CPU issues a Data Strobe ($\overline{DS}$). If the register indicated by the address does not exist, the Z-CIO remains high-impedance.

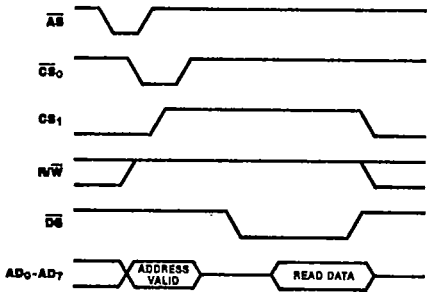


Figure 1. Read Cycle Timing

Write Cycle. The CPU places an address on the address/data bus. The more significant bits and status information are combined and decoded by external logic to provide two Chip Selects ($\overline{CS_0}$ and CS_1). Six bits of the least significant byte of the address are latched within the Z-CIO and used to specify a Z-CIO register. The CPU places the data on the address/data bus and strobes it into the Z-CIO register by issuing a Data Strobe ($\overline{DS}$).

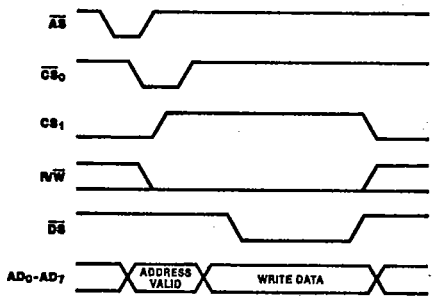
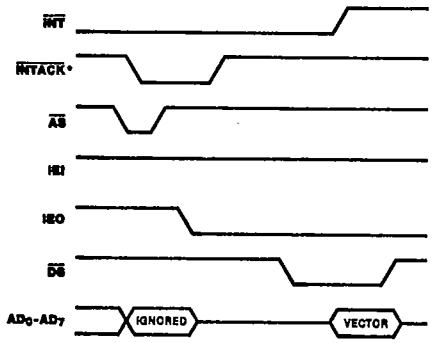


Figure 2. Write Cycle Timing

Interrupt Acknowledge Cycle. When one of the IP bits in the Z-CIO goes High and interrupts are enabled, the Z-CIO pulls its $\overline{INT}$ output line Low, requesting an interrupt. The CPU responds with an Interrupt Acknowledge cycle. When $\overline{INTACK}$ goes Low with IP set, the Z-CIO pulls its Interrupt Enable Out (IEO) Low, disabling all lower priority devices on the daisy chain. The CPU reads the Z-CIO interrupt vector by issuing a Low $\overline{DS}$, thereby strobing the interrupt vector onto the address/ data bus. The IUS that corresponds to the IP is also set, which causes IEO to remain Low.



*$\overline{INTACK}$ is decoded from Z8000 status.

Figure 3. Interrupt Acknowledge Timing

ABSOLUTE MAXIMUM RATINGS

Guaranteed by characterization/design.

Voltages on all pins with respect to GND . . . . . −0.3V to +7V
Operating Case Temperature . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Absolute Maximum Power Dissipation 1.2W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

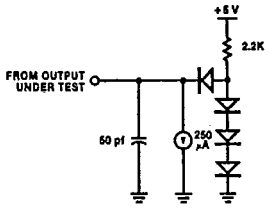
The DC Characteristics and Capacitance sections listed below apply for the following standard test conditions, unless otherwise noted.

Military Operating Temperature Range (T_C)
−55°C to +125°C

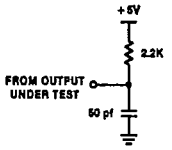
Standard Military Test Condition
$+4.5V \leq V_{CC} \leq +5.5V$

All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 50 pf max.



Standard Test Load



Open-Drain Test Load

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	2.2[a]	V_{CC} + 0.3[c]	V	
V_{IL}	Input Low Voltage	−0.3[c]	0.8[a]	V	
V_{OH}	Output High Voltage	2.4[a]		V	I_{OH} = −250 µA
V_{OL}	Output Low Voltage		0.4[a]	V	I_{OL} = +2.0 mA
			0.5[b]	V	I_{OL} = +3.2 mA
I_{IL}	Input Leakage Current		±10[a]	µA	$0.4 \leq V_{IN} \leq +2.4V$
I_{OL}	Output Leakage		±10[a]	µA	$0.4 \leq V_{OUT} \leq +2.4V$
I_{CC}	I_{CC} Supply Current		200[a]	mA	

V_{CC} = 5V ±5% unless otherwise specified, over specified temperature range.

CAPACITANCE

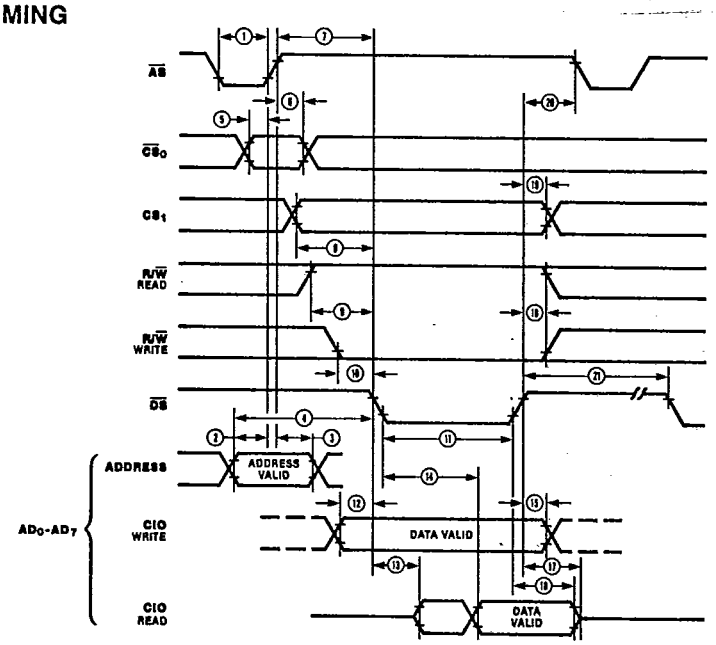
Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance		10[b]	pf
C_{OUT}	Output Capacitance		15[b]	pf
$C_{I/O}$	Bidirectional Capacitance		20[b]	pf

f = 1 MHz, over specified temperature range.
Unmeasured pins returned to ground.

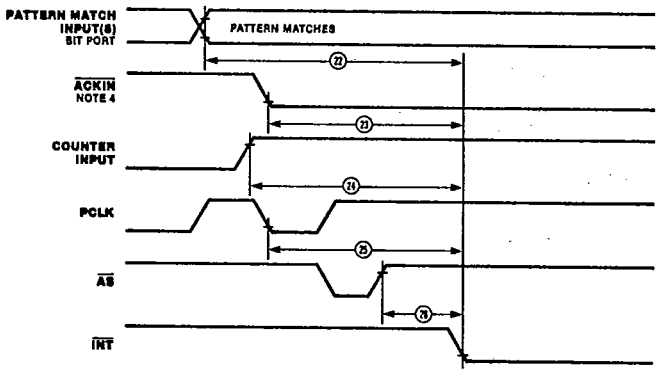
Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design

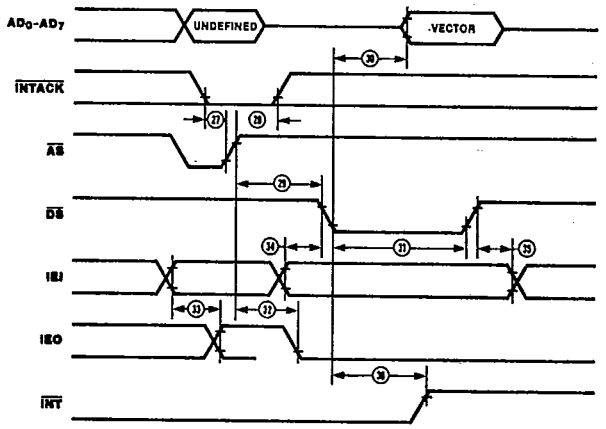
CPU INTERFACE TIMING



INTERRUPT TIMING



INTERRUPT ACKNOWLEDGE TIMING



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AC CHARACTERISTICS

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Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes†
1	TwAS	$\overline{AS}$ Low Width	70[a]	2000[a]	50[a]	2000[a]	
2	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30[a]		10[a]		1
3	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50[a]		30[a]		1
4	TsA(DS)	Address to $\overline{DS}$ ↓ Setup Time	130[b]		100[b]		1
5	TsCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time	0[b]		0[b]		1
6	ThCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time	60[a]		40[b]		1
7	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	85[b]		55[b]		1
8	TsCS1(DS)	CS_1 to $\overline{DS}$ ↓ Setup time	100[a]		80[b]		
9	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100[a]		80[a]		
10	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup time	0[b]		0[b]		
11	TwDS	$\overline{DS}$ Low Width	390[b]		250[b]		
12	TsDW(DSf)	Write Data to $\overline{DS}$ ↓ Setup Time	30[b]		20[b]		
13	TdDS(DRV)	$\overline{DS}$ (Read) ↓ to Address Data Bus Driven	0[b]		0[b]		
14	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250[b]		180[b]	
15	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30[b]		20[b]		
16	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0[b]		0[b]		
17	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70[b]		45[b]	2
18	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55[b]		40[b]		
19	ThCS1(DS)	CS_1 to $\overline{DS}$ ↑ Hold Time	55[b]		40[b]		
20	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50[b]		25[b]		
21	Trc	Valid Access Recovery Time	1000[b]		650[b]		3
22	TdPM(INT)	Pattern Match to $\overline{INT}$ Delay (Bit Port)		1+800[b]		1+800[b]	6
23	TdACK(INT)	$\overline{ACKIN}$ to $\overline{INT}$ Delay (Port with Handshake)		4+600[b]		4+600[b]	4,6
24	TdCI(INT)	Counter Input to $\overline{INT}$ Delay (Counter Mode)		1+700[b]		1+700[b]	6
25	TdPC(INT)	PCLK to $\overline{INT}$ Delay (Timer Mode)		1+700[b]		1+700[b]	6
26	TdAS(INT)	$\overline{AS}$ to $\overline{INT}$ Delay		300[b]		d	
27	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0[a]		0[b]		
28	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250[a]		250[a]		
29	TsAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Setup Time	350[b]		250[b]		5
30	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Valid Delay		250[b]		180[b]	

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured to the time when the output has changed 0.5V from steady state with minimum AC load and maximum DC load.
3. This is the delay from $\overline{DS}$ ↑ of one CIO access to $\overline{DS}$ ↓ of another CIO access.
4. The delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake. One additional AS cycle is required for ports in the Single Buffered mode.
5. The parameters for the devices in any particular daisy chain must meet the following constraint: the delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ must be greater than the sum of TdAS(IEO) for the highest priority peripheral, TsIEI(DSA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.
6. Units equal to AS cycle + ns.

† Units in nanoseconds, except as noted.

Parameter Test Status:

a Tested
b Guaranteed
c Guaranteed by characterization/design
d Parameter not tested, not guaranteed

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AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes†
31	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390[b]		250[b]		
32	TdAS(IEO)	$\overline{AS}$ ↑ to IEO ↓ Delay ($\overline{INTACK}$ Cycle)		350[b]		250[b]	5
33	TdIEI(IEO)	IEI to IEO Delay		150[b]		100[b]	5
34	TsIEI(DSA)	IEO to $\overline{DS}$ (Acknowledge) ↓ Setup Time	100[b]		70[b]		5
35	ThIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↑ Hold Time	100[b]		70[b]		
36	TdDSA(INT)	$\overline{DS}$ (Acknowledge) ↓ to $\overline{INT}$ ↑ Delay		600[b]		600[b]	

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured to the time when the output has changed 0.5V from steady state with minimum AC load and maximum DC load.
3. This is the delay from $\overline{DS}$ ↑ of one CIO access to $\overline{DS}$ ↓ of another CIO access.
4. The delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake. One additional AS cycle is required for ports in the Single Buffered mode.
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6. Units equal to AS cycle + ns.

† Units in nanoseconds, except as noted.

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by characterization/design
[d] Parameter not tested, not guaranteed

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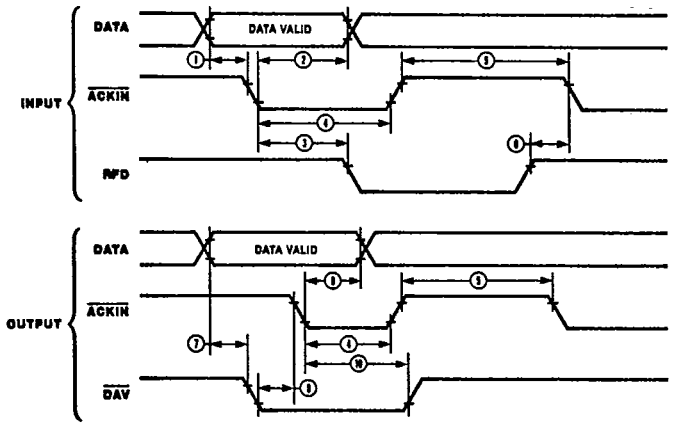
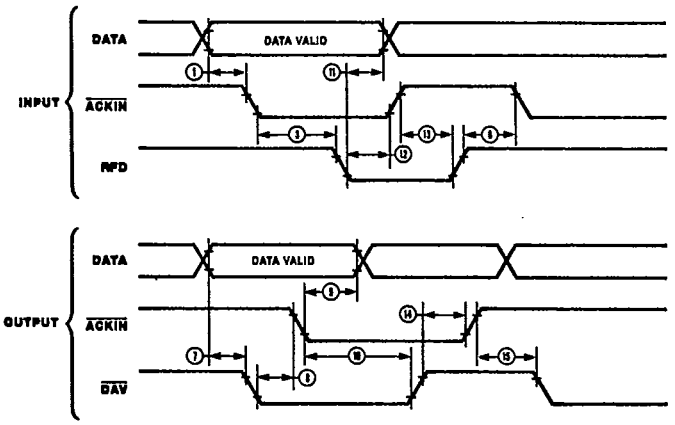
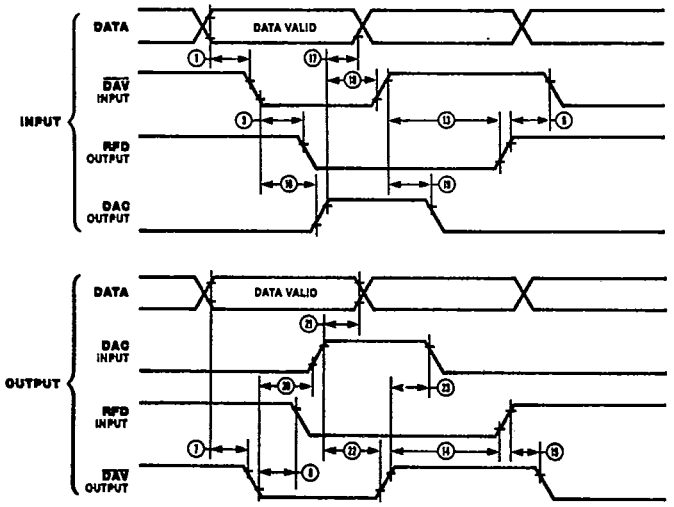
STROBED HANDSHAKE



INTERLOCKED HANDSHAKE



3-WIRE HANDSHAKE



AC CHARACTERISTICS (Continued)

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Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes*†
1	TsDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Setup time	0[b]		0[b]		
2	ThDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Hold Time—Strobed Handshake	500[b]		d		
3	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ Delay	0[b]		0[b]		
4	TwACKl	$\overline{ACKIN}$ Low Width—Strobed Handshake	250[b]		d		
5	TwACKh	$\overline{ACKIN}$ High Width—Strobed Handshake	250[b]		d		
6	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ Delay	0[b]		0[b]		
7	TsDO(DAV)	Data Out to $\overline{DAV}$ ↓ Setup Time	25[b]		20[b]		1
8	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay	0[b]		0[b]		
9	ThDO(ACK)	Data Out to $\overline{ACKIN}$ ↓ Hold Time	1[b]		1[b]		2
10	TdACK(DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ Delay	1[b]		1[b]		2
11	ThDI(RFD)	Data Input to RFD ↓ Hold Time—Interlocked Handshake	0[b]		0[b]		
12	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ Delay—Interlocked Handshake	0[b]		0[b]		
13	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ Delay—Interlocked and 3-Wire Handshake	0[b]		0[b]		
14	TdDAVr(ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↑)—Interlocked and 3-Wire Handshake	0[b]		0[b]		
15	TdACK(DAV)	$\overline{ACKIN}$ ↑ (RFD ↑) to $\overline{DAV}$ ↓ Delay—Interlocked and 3-Wire Handshake	0[b]		0[b]		
16	TdDAVlf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay—Input 3-Wire Handshake	0[b]		0[b]		
17	ThDI(DAC)	Data Input to DAC ↑ Hold Time—3-Wire Handshake	0[b]		0[b]		
18	TdDACOr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay—Input 3-Wire Handshake	0[b]		0[b]		
19	TdDAVlr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay—Input 3-Wire Handshake	0[b]		0[b]		
20	TdDAVOf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay—Output 3-Wire Handshake	0[b]		0[b]		
21	ThDO(DAC)	Data Output to DAC ↑ Hold Time—3-Wire Handshake	1[b]		1[b]		2
22	TdDACIr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay—Output 3-Wire Handshake	1[b]		1[b]		
23	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay—Output 3-Wire Handshake	0[b]		0[b]		

NOTES:
1. This time can be extended through the use of the deskew timers.
2. Units equal to AS cycle.

* All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".
† Units in nanoseconds (ns), except as noted.

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design
[d] Parameter Not Tested, Not Guaranteed

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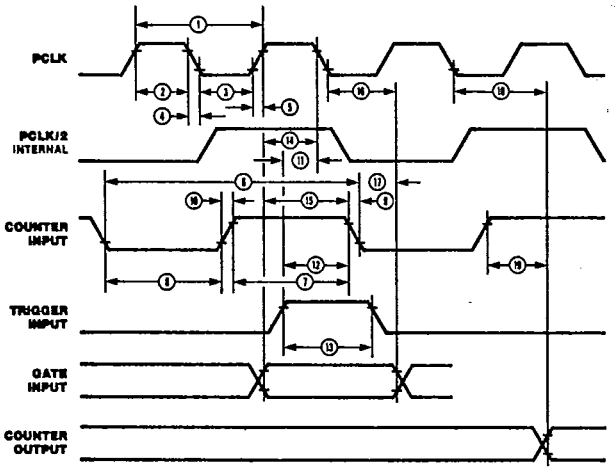
COUNTER/TIMER TIMING



Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes*†
1	TcPC	PCLK Cycle Time	250[a]	4000[a]	165[a]	4000[a]	1
2	TwPCh	PCLK High Width	105[b]	2000[a]	70[b]	2000[a]	
3	TwPCl	PCLK Low Width	105[a]	2000[a]	70[a]	2000[a]	
4	TfPC	PCLK Fall Time		20[b]		10[a]	
5	TrPC	PCLK Rise Time		20[b]		15[b]	
6	TcCI	Counter Input Cycle Time	500[b]		330[b]		
7	TCIh	Counter Input High Width	230[b]		150[b]		
8	TwCIl	Counter Input Low Width	230[b]		150[b]		
9	TfCI	Counter Input Fall Time		20[b]		15[b]	
10	TrCI	Counter Input Rise Time		20[b]		15[b]	
11	TsTI(PC)	Trigger Input to PCLK ↓ Setup Time (Timer Mode)	150[b]			d	2
12	TsTI(CI)	Trigger Input to Counter Input ↓ Setup Time (Counter Mode)	150[b]			d	2
13	TwTI	Trigger Input Pulse Width (High or Low)	200[b]			d	
14	TsGI(PC)	Gate Input to PCLK ↓ Setup Time (Timer Mode)	100[b]			d	2
15	TsGI(CI)	Gate Input to Counter Input ↓ Setup Time (Counter Mode)	100[b]			d	2
16	ThGI(PC)	Gate Input to PCLK ↓ Hold Time (Timer Mode)	100[b]			d	2
17	ThGI(CI)	Gate Input to Counter Input ↓ Hold Time (Counter Mode)	100[b]			d	2
18	TdPC(CO)	PCLK To Counter Output Delay (Timer Mode)		475[b]		d	
19	TdCI(CO)	Counter Input to Counter Output Delay (Counter Mode)		475[b]		d	

NOTES:
1. PCLK is only used with the counter/timers (in Timer mode), the deskew timers, and the REQUEST/$\overline{\text{WAIT}}$ logic. If these functions are not used, the PCLK input can be held low.
2. These parameters must be met to guarantee the trigger or gate is valid for the next counter/timer cycle.

* All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".
† Units in nanoseconds (ns), except as noted.

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design
[d] Parameter Not Tested, Not Guaranteed

REQUEST/$\overline{WAIT}$ TIMING

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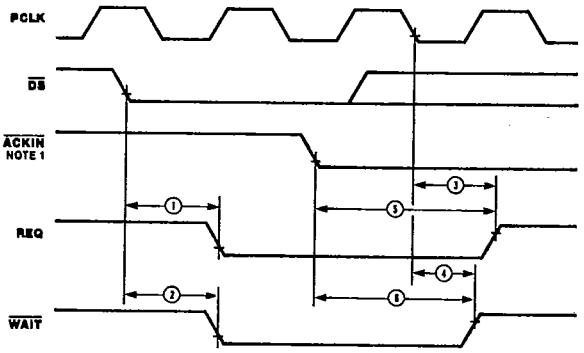
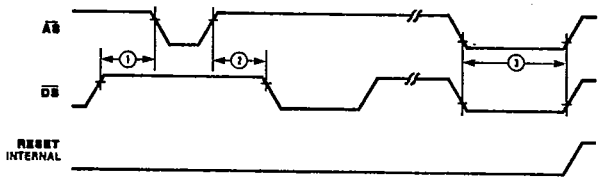


Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes*†
1	TdDS(REQ)	$\overline{DS}$ ↓ to REQ ↓ Delay		500[b]		d	
2	TdDS(WAIT)	$\overline{DS}$ ↓ to $\overline{WAIT}$ ↓ Delay		500[b]		d	
3	TdPC(REQ)	PCLK ↓ to REQ ↑ Delay		300[b]		d	
4	TdPC(WAIT)	PCLK ↓ to $\overline{WAIT}$ ↑ Delay		300[b]		d	
5	TdACK(REQ)	$\overline{ACKIN}$ ↓ to REQ ↑ Delay		3+2		d	
				+1000[b]		d	1,2
6	TdACK(WAIT)	$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ ↑ Delay		10+600[b]		d	3

NOTES:
1. The Delay is from $\overline{DAV}$ ↓ for the 3-Wire Input Handshake. The delay is from DAC ↑ for the 3-Wire Output Handshake.
2. Units equal to AS cycles + PCLK cycles + ns.
3. Units equal to PCLK cycles + ns.
* All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".
† Units in nanoseconds (ns), except as noted.

RESET TIMING



Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes*†
1	TdDSQ(AS)	Delay from $\overline{DS}$ ↑ to $\overline{AS}$ ↓ for No Reset	40[b]		15[b]		
2	TdASQ(DS)	Delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ for No Reset	50[b]		30[b]		
3	TwRES	Minimum Width of $\overline{AS}$ and $\overline{DS}$ both Low for Reset	250[a]		170[a]		1

NOTES:
1. Internal circuitry allows for the reset provided by the Z8 ($\overline{DS}$ held Low while $\overline{AS}$ pulses) to be sufficient.
* All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".
† Units in nanoseconds (ns).

Parameter Test Status:

a Tested
b Guaranteed
c Guaranteed by Characterization/Design
d Parameter Not Tested, Not Guaranteed

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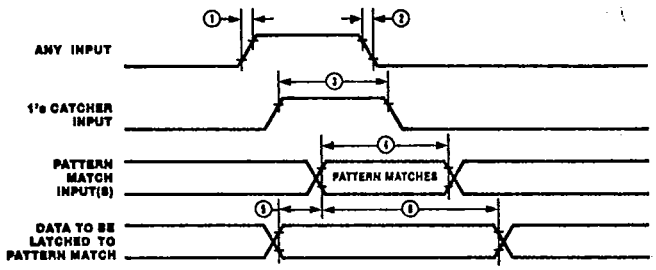
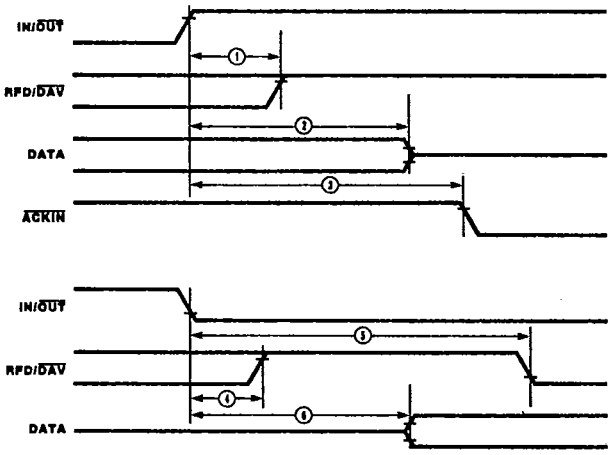
MISCELLANEOUS PORT TIMING



Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes*†
1	Trl	Any Input Rise Time		100[b]		100[b]	
2	Tfl	Any Input Fall Time		100[b]		100[b]	
3	Tw1's	1's Catcher High Width	250[b]		170[b]		1
4	TwPM	Pattern Match Input Valid (Bit Port)	750[b]		500[b]		
5	TsPMD	Data Latched on Pattern Match Setup Time (Bit Port)	0[b]		0[b]		
6	ThPMD	Data Latched on Pattern Match Hold Time (Bit Port)	1000[b]		650[b]		

NOTES:
1. If the input is programmed inverting, a Low-going pulse of the same width will be detected.
* All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".
† Units in nanoseconds (ns), except as noted.

BIDIRECTIONAL PORT TIMING



Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Notes*†
1	TdIOr(DAV)	I/$\overline{O}$ ↑ to RFD/$\overline{DAV}$ High Delay		500[b]		500[b]	
2	TdIOr(DRZ)	I/$\overline{O}$ ↑ to Data Float Delay		500[b]		500[b]	
3	TdIOr(ACK)	I/$\overline{O}$ ↑ to $\overline{ACKIN}$ ↓ Delay					2
4	TdIOf(RFD)	I/$\overline{O}$ ↓ to RFD/$\overline{DAV}$ High Delay		500[b]		500[b]	
5	TdIOf(DAV)	I/$\overline{O}$ ↓ to RFD/$\overline{DAV}$ ↓ Delay	3[b]		3[b]		1
6	TdDO(IO)	I/$\overline{O}$ ↓ to Data Bus Driven	2[b]		2[b]		1

NOTES:
1. Units equal to AS cycles.
2. Minimum delay is four AS cycles or one AS cycle after the corresponding IP is cleared, whichever is longer.
* All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".
† Units in nanoseconds (ns).

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design
[d] Parameter Not Tested, Not Guaranteed

PIN DESCRIPTION

AD_0-AD_7. *Z-BUS Address/Data lines* (bidirectional/3-state). These multiplexed Address/Data lines are used for transfers between the CPU and Z-CIO.

$\overline{AS}$*. *Address Strobe* (Input, active Low). Addresses, $\overline{INTACK}$, and $\overline{CS_0}$ are sampled while $\overline{AS}$ is Low.

$\overline{CS_0}$ and CS_1. *Chip Select 0* (input, active Low) and *Chip Select 1* (input, active High). $\overline{CS_0}$ and CS_1 must be Low and High, respectively, in order to select a device. $\overline{CS_0}$ is latched by $\overline{AS}$.

$\overline{DS}$*. *Data Strobe* (input, active Low). $\overline{DS}$ provides timing for the transfer of data into or out of the Z-CIO.

IEI. *Interrupt Enable In* (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from the requesting Z-CIO or is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

*When $\overline{AS}$ and $\overline{DS}$ are detected Low at the same time (normally an illegal condition), the Z-CIO is reset.

$\overline{INT}$. *Interrupt Request* (output, open-drain, active Low). This signal is pulled Low when the Z-CIO requests an interrupt.

$\overline{INTACK}$. *Interrupt Acknowledge* (input, active Low). This signal indicates to the Z-CIO that an Interrupt Acknowledge cycle is in progress. $\overline{INTACK}$ is sampled while $\overline{AS}$ is Low.

PA_0-PA_7. *Port A I/O lines* (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the Z-CIO's Port A and external devices.

PB_0-PB_7. *Port B I/O lines* (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the Z-CIO's Port B and external devices. May also be used to provide external access to Counter/Timers 1 and 2.

PC_0-PC_3. *Port C I/O lines* (bidirectional, 3-state, or open-drain). These four I/O lines are used to provide handshake, $\overline{WAIT}$, and REQUEST lines for Ports A and B or to provide external access to Counter/Timer 3 or access to the Z-CIO's Port C.

PCLK. *(input, TTL-compatible).* This is a peripheral clock that may be, but is not necessarily, the CPU clock. It is used with timers and REQUEST/$\overline{WAIT}$ logic.

R/$\overline{W}$. *Read/Write* (input). R/$\overline{W}$ indicates that the CPU is reading from (High) or writing to (Low) the Z-CIO.

PACKAGE PINOUTS

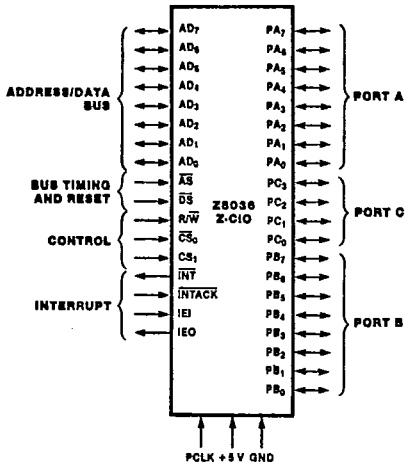


Figure 4. Pin Functions

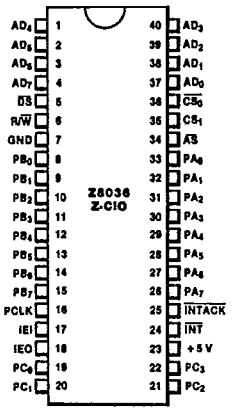


Figure 5. 40-pin Dual-In-Line Package (DIP), Pin Assignments

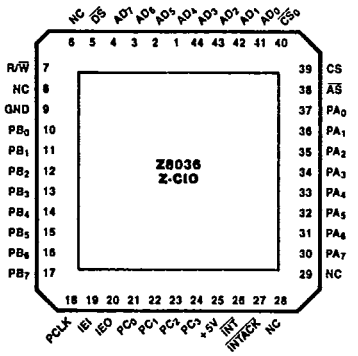


Figure 6. 44-pin Chip Carrier, Pin Assignments

MIL-STD-883 MILITARY PROCESSED PRODUCT

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/ Quality Conformance testing required.

Zilog Military Product Flow

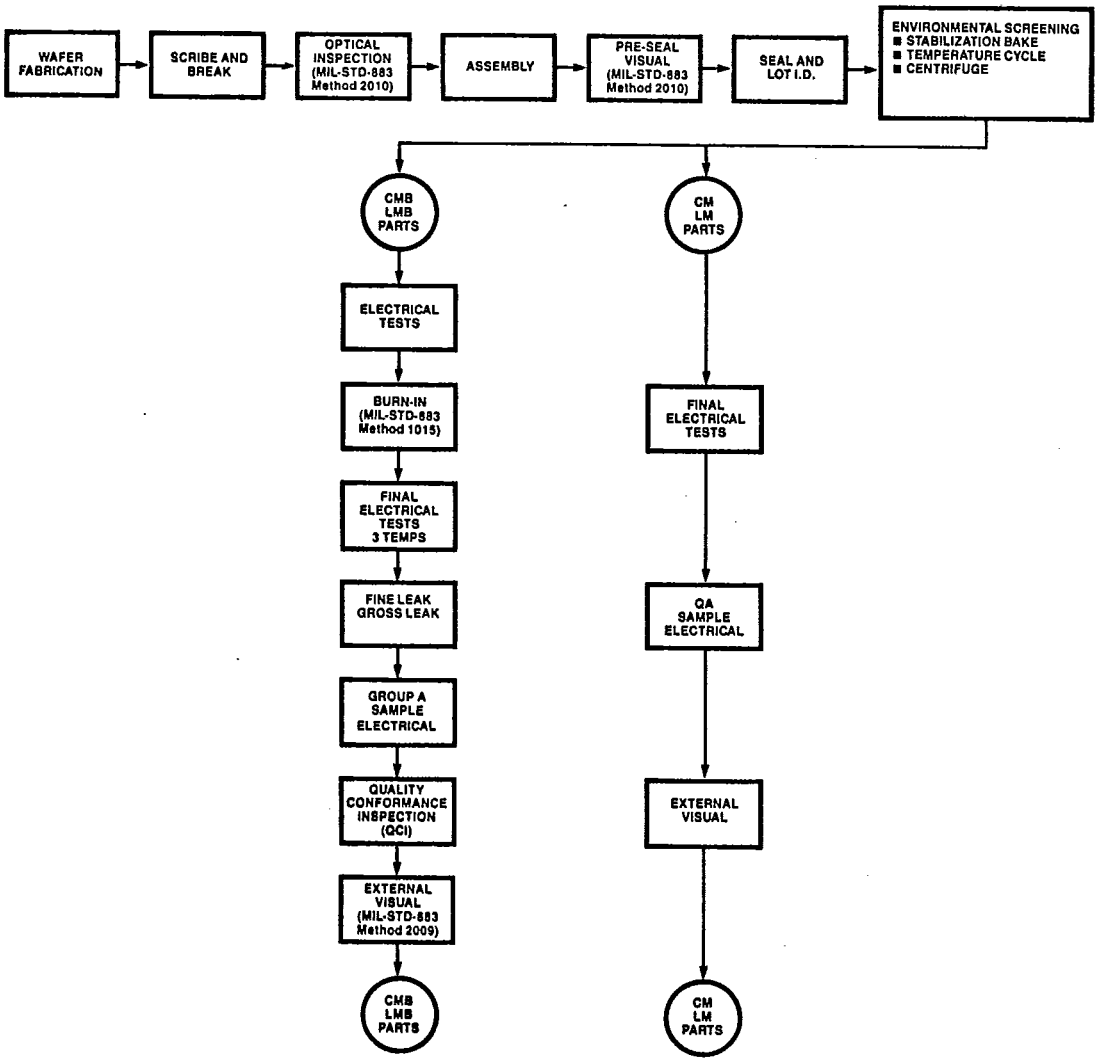


Table I
MIL-STD-883 Class B Screening Requirements
Method 5004

Test	Mil-Std-883 Method	Test Condition	Requirement
Internal Visual	2010	Condition B	100%
Stabilization Bake	1008	Condition C	100%
Temperature Cycle	1010	Condition C	100%
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 1), Y_1 Axis Only	100%
Initial Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
Burn-In	1015	Condition D(Note 2), 160 hours, T_A = +125°C	100%
Interim Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
PDA Calculation		PDA = 5%	100%
Final Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +125°C, −55°C Functional, Switching/AC T_C = +25°C	100%
Fine Leak	1014	Condition A_2	100%
Gross Leak	1014	Condition C	100%
Quality Conformance Inspection (QCI)			
Group A Each Inspection Lot	5005	(See Table II)	Sample
Group B Every Week	5005	(See Table III)	Sample
Group C Periodically (Note 3)	5005	(See Table IV)	Sample
Group D Periodically (Note 3)	5005	(See Table V)	Sample
External Visual	2009		100%
QA—Ship			100%

NOTES:
1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).

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Table II Group A
Sample Electrical Tests
MIL-STD-883 Method 5005

Subgroup	Tests	Temperature (T_C)	LTPD Max Accept = 2
Subgroup 1	Static/DC	+25°C	2
Subgroup 2	Static/DC	+125°C	3
Subgroup 3	Static/DC	−55°C	5
Subgroup 7	Functional	+25°C	2
Subgroup 8	Functional	−55°C and +125°C	5
Subgroup 9	Switching/AC	+25°C	2
Subgroup 10	Switching/AC	+125°C	3
Subgroup 11	Switching/AC	−55°C	5

NOTES:
- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

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Table III Group B

Sample Test Performed Every Week to Test Construction and Insure Integrity of Assembly Process. MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		2/0
Subgroup 2			
Resistance to Solvents	2015		4/0
Subgroup 3			
Solderability	2003	Solder Temperature +245°C ± 5°C	15(Note 1)
Subgroup 4			
Internal Visual and Mechanical	2014		1/0
Subgroup 5			
Bond Strength	2011	C	15(Note 2)
Subgroup 6(Note 3)			
Internal Water Vapor Content	1018	1000 ppm. maximum at +100°C	3/0 or 5/1
Subgroup 7(Note 4)			
Seal	1014		5
7a) Fine Leak		7a) A_2	
7b) Gross Leak		7b) C	
Subgroup 8(Note 5)			
Electrostatic Discharge Sensitivity	3015	Zilog Military Electrical Specification Static/DC T_C = +25°C A = 20-2000V B = >2000V Zilog Military Electrical Specification Static/DC T_C = +25°C	15/0

NOTES:
1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

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Table IV Group C

Sample Test Performed Periodically to Verify Integrity of the Die.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Steady State Operating Life	1005	Condition D(Note 1), 1000 hours at +125°C	5
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 2			
Temperature Cycle	1010	Condition C	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	
Seal	1014		15
2a) Fine Leak		2a) Condition A_2	
2b) Gross Leak		2b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	

NOTE:
1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.

Table V Group D

Sample Test Performed Periodically to Insure Integrity of the Package.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Condition B_2 or D(Note 1)	15
Subgroup 3			
Thermal Shock	1011	Condition B minimum, 15 cycles minimum	
Temperature Cycling	1010	Condition C, 100 cycles minimum	15
Moisture Resistance	1004		
Seal	1014		
3a) Fine Leak		3a) Condition A_2	
3b) Gross Leak		3b) Condition C	
Visual Examination	1004 or 1010		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 4			
Mechanical Shock	2002	Condition B minimum	
Vibration Variable Frequency	2007	Condition A minimum	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	15
Seal	1014		
4a) Fine Leak		4a) Condition A_2	
4b) Gross Leak		4b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 5			
Salt Atmosphere	1009	Condition A minimum	
Seal	1014		15
5a) Fine Leak		5a) Condition A_2	
5b) Gross Leak		5b) Condition C	
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm. maximum water content at +100°C	3/0 or 5/1
Subgroup 7(Note 3)			
Adhesion of Lead Finish	2025		15(Note 4)
Subgroup 8(Note 5)			
Lid Torque	2024		5/0

NOTES:
1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

PACKAGE INFORMATION

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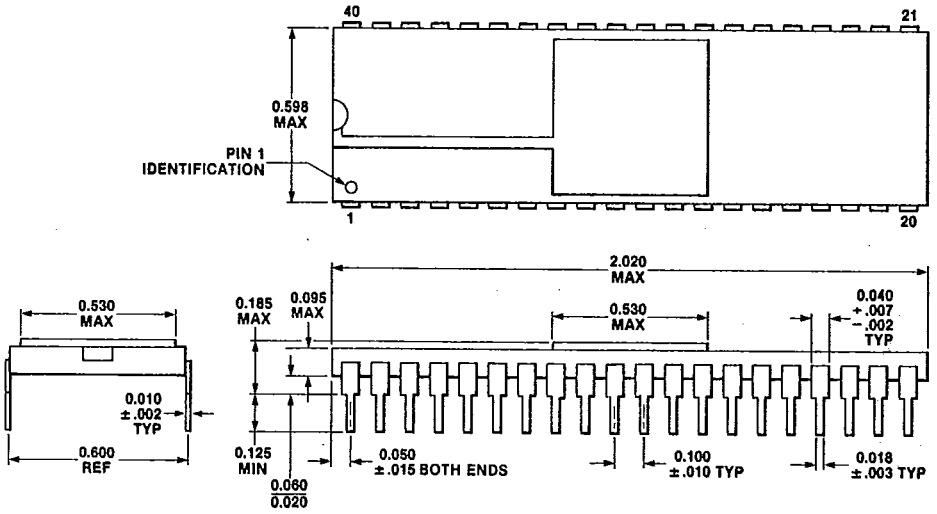
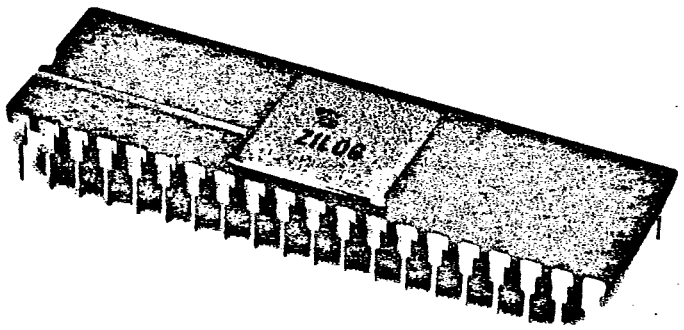
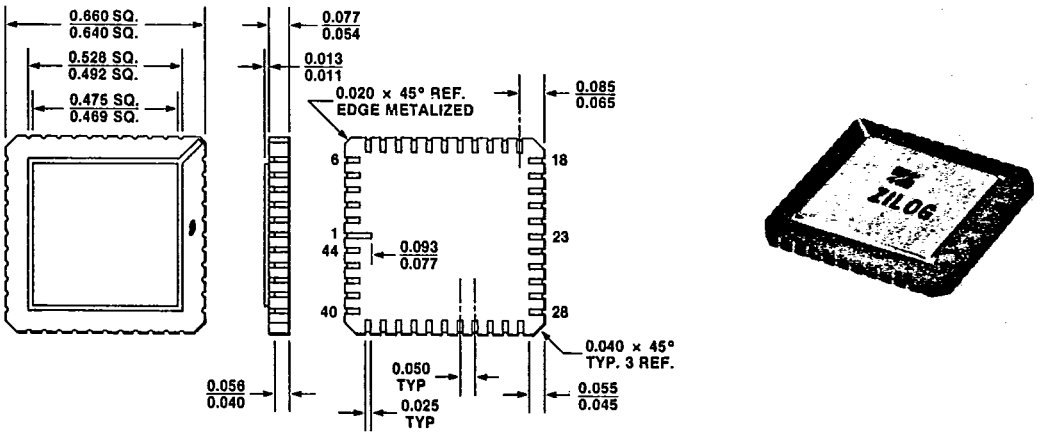


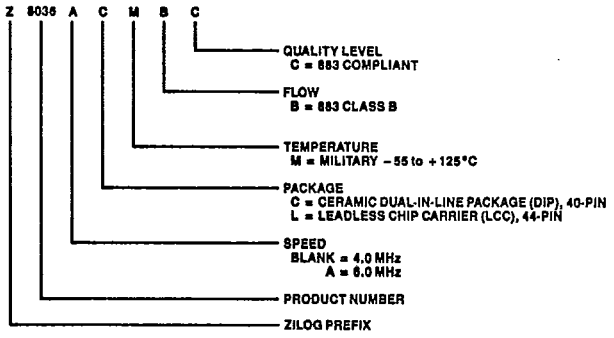


40-Pin Ceramic Dual In-line Package (DIP)



44-Pin Ceramic Leadless Chip Carrier (LCC)

ZILOG ORDERING INFORMATION



AVAILABLE MILITARY PRODUCTS

Z8036 Z-CIO, 4.0 MHz

40-pin DIP	44-pin LCC
Z8036 CM	Z8036 LM
Z8036 CMBC	Z8036 LMBC

Z8036A Z-CIO, 6.0 MHz

40-pin DIP	44-pin LCC
Z8036A CM	Z8036A LM
Z8036A CMBC	Z8036A LMBC