Zilog

Z8152A/53A VSC

Video System Controller

PRELIMINARY PRODUCT SPECIFICATION

DISTINCTIVE CHARACTERISTICS

- 100 MHz Video Dot Rate
- Four-level current driven (75Ω) differential video output
- Digital Video output ECL option (Z8152A provides TTL option)
- On-board crystal driven oscillator
- Proportional Spacing Support (2—17 dots)
- 9-bit dot data parallel input, with expansion capability to seventeen bits
- Trailing blanks (0—3 dots)
- Double Width Characters
- Attribute Support:
  - Character Blink
  - Underline
  - Overstrike
  - Reverse
  - Highlight
- Buffered and Synchronized Character Clock Outputs
- Background color selection
- Buffered and Synchronized Vertical and Horizontal Sync Outputs

GENERAL DESCRIPTION

The Z8152A/53A Video System Controller (VSC) provides interface between a CRT controller and a CRT monitor. The basic chip functions are:

- Support proportional and non-proportional character display
- Correctly synchronize and mix character attributes with video signals
- Output the video information in a four-level analog or digital format

The VSC consists of a parallel-to-serial converter which provides a video bit stream to on-chip attribute logic. This logic, under control of the attribute inputs, operates on the bit stream to generate grey scale video. Video outputs from the VSC are of two forms—analog and digital. The digitally encoded outputs implement four video levels: Blank, Black, Grey and White. Identical information is available in analog form via differential outputs (current driven) into a nominal 75Ω impedance.

The Z8152A/53A also supports proportional spacing using a bit width programmable character clock. Character ROM pixel information is selectable from two to seventeen pixels per character. Up to three blank pixels can be appended to the character ROM input thereby facilitating right justification of text.

The difference between the Z8152A and the Z8153A is in the output scheme. The Z8152A has standard TTL outputs and operates in the 25—60 MHz range, while the Z8153A has 10K ECL outputs and operates in the 40—100 MHz range.

The Z8152A/53A is fabricated using an advanced bipolar process with internal ECL logic. The device is available in conventional 48-pin dual-in-line packages.

Figure 1. Z8152A/53A Block Diagram

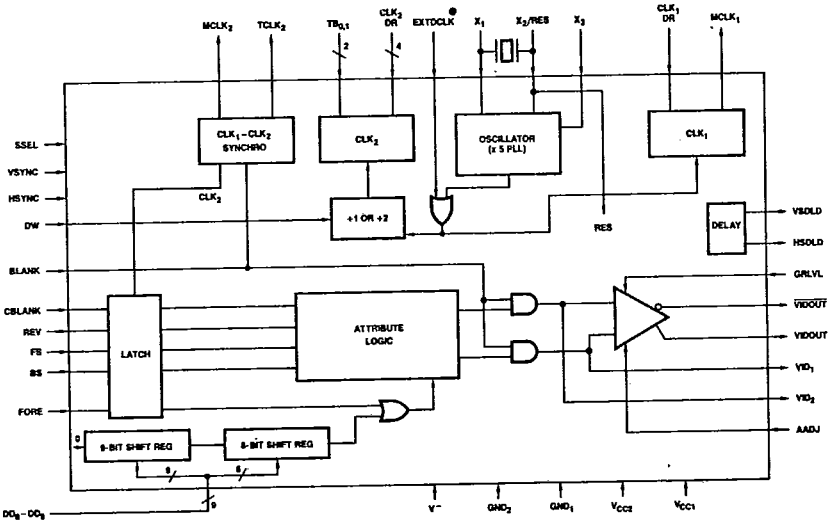


Figure 2. Z8152A/53A Pin Functions

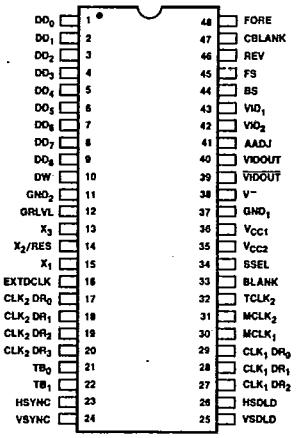
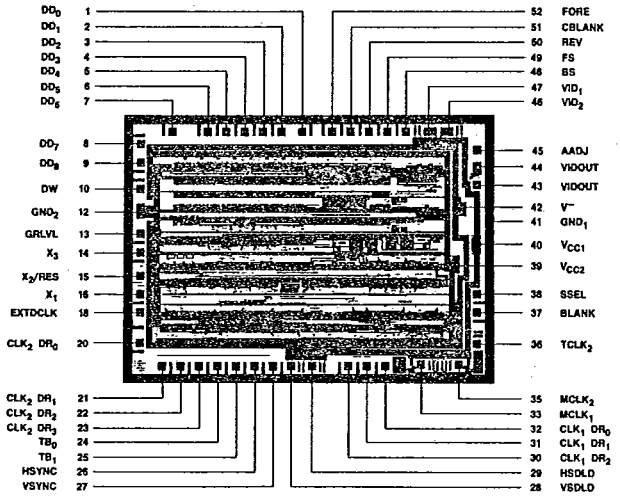


Figure 3. Metallization and Pad Layout



PIN DESCRIPTION

$MCLK_1$ **$CLOCK_1$ (output, non-TTL compatible)**
$MCLK_1$ is a system clock. It is intended to drive the Z8052 horizontal and vertical timing circuitry as well as the DMA operations. $MCLK_1$ output is nominally a square wave divided down from the internal dot clock frequency according to the CLK_1 DR (CLK_1 Divide Ratio) input.

CLK_1 DR **CLK_1 DIVIDE RATIO (inputs (3))**
CLK_1 DR are three inputs which control the $MCLK_1$ divide ratio. The three inputs may be programmed to divide the $MCLK_1$ signal by two, four, six, . . . , sixteen.

CLK_1 DR 2	1	0	A(1)	B(1)
L	L	L	1	1
L	L	H	2	2
L	H	L	3	3
L	H	H	4	4
H	L	L	5	5
H	L	H	6	6
H	H	L	7	7
H	H	H	8	8

$MCLK_2$ **$CLOCK_2$ (output, non-TTL compatible)**
$MCLK_2$ is a character display clock. Its function is to control the character code and attribute data output rate from the appropriate Z8052 CRTC's ports.

CLK_2DR **$CLOCK_2$ DIVIDE RATIO (inputs (4))**
CLK_2 DR are four inputs which control an internal divider to divide the dot clock frequency by a value from two to seventeen.

CLK_2 DR 3	2	1	0	C(1)	D(1)
L	L	L	L	1	1
L	L	L	H	1	2
L	L	H	L	2	2
L	L	H	H	2	3
L	H	L	L	3	3
L	H	L	H	3	4
L	H	H	L	4	4
L	H	H	H	4	5
H	L	L	L	5	5
H	L	L	H	5	6
H	L	H	L	6	6
H	L	H	H	6	7
H	H	L	L	7	7
H	H	L	H	7	8
H	H	H	L	8	8
H	H	H	H	8	9

Note 1. A, B, C, and D are measured in EXTDCLK periods.
(See Reset Timing on page 15).

$TCLK_2$ **TTL $CLOCK_2$ (output)**
$TCLK_2$ is a TTL compatible version of $MCLK_2$.

X_1,X_2/RES **X_1, X_2/RESET (inputs, X_2, is non-TTL compatible, reset is TTL compatible)**
X_1, X_2/RES are the external crystal inputs when the on-chip oscillator of the VSC is being used. The external crystal frequency is multiplied by five to produce the on-chip dot clock. If the external dot clock option is used, the X_1 should be tied LOW and X_2/RES may be used as a reset input, to synchronize multiple VSC's. Note that the reset signal should be synchronous to the external dot clock.

X_3 **X_3 (input, non-TTL compatible)**
X_3 is used as an input to the on-chip voltage-controlled oscillator. When the on-chip oscillator of the VSR is being used, X_3 should be connected to ground by an appropriate capacitor. If the external dot clock option is used, X_3 and X_1 should be tied LOW.

VSYNC **VERTICAL SYNC (input)**
VSYNC is an input that must be synchronous to either $MCLK_1$ or $MCLK_2$, dependent on the SSEL input. If SSEL is HIGH, VSYNC must be synchronous to $MCLK_1$.

VSDLD **VERTICAL SYNC DELAYED (output)**
VSDLD is the delayed output of VSYNC, synchronous to $MCLK_1$ or $MCLK_2$, depending on the setting of SSEL.

HSYNC **HORIZONTAL SYNC DELAYED (input)**
HSYNC is an input that must be synchronous to either $MCLK_1$ or $MCLK_2$, dependent upon the SSEL input. If SSEL is LOW, HSYNC must be synchronous to $MCLK_2$; if SSEL is HIGH, HSYNC must be synchronous to $MCLK_1$.

HSDLD **HORIZONTAL SYNC (output)**
HSDLD is the delayed output of HSYNC, synchronous to $MCLK_1$ or $MCLK_2$, depending upon the setting of SSEL.

SSEL **SYNC SELECT (input)**
The SSEL line determines if the VSYNC, HSYNC and BLANK are going to be synchronized to the $MCLK_1$ or $MCLK_2$ signals. A HIGH on SSEL also will resynchronize CLK_2 and CLK_1 during blanking.

BLANK **BLANK (input)**
BLANK is an input normally synchronous to $MCLK_1$, although it may be synchronous to $MCLK_2$ in non-proportional spacing applications. The active pulse width of BLANK will usually overlap the inactive-to-active waveforms of HSYNC and VSYNC, as well as the active-to-inactive portion of VSYNC. While BLANK is active $TCLK_2$/$MCLK_2$ may be forced to synchronize to the $MCLK_1$ clock. When BLANK goes inactive, the rising edges of $MCLK_1$ and $TCLK_2$/$MCLK_2$ must be synchronized in order to prevent "dot walk" in proportional spacing applications. BLANK active also forces the video output level to "blank" regardless of DD, FORE or other inputs.

CBLANK **CHARACTER BLANK (input)**
CBLANK forces video output levels (VID_1, VID_2, VIDOUT and VIDOUT) to switch to the background color level.

FORE **FOREGROUND VIDEO (input)**
The FORE video input is "OR'ed" with the dot data output by the parallel-to-serial shift register to switch to the foreground color level (e.g., to implement underlines).

REV **REVERSE (input)**
The REV input causes the foreground color levels to be transposed with the background color level for the total character period (including any tracking blanks).

FS **FOREGROUND SHIFT (input)**
The FS input causes the shift in the video output levels to produce a highlight effect. See Table 1.

TB_0, TB_1 **TRAILING BLANKS (inputs(2))**
The TB inputs concatenate "blank" video dots to the tail end of the dot data contained in the parallel-to-serial shift register. TB can be specified to concatenate 0, 1, 2 or 3 dots. The TB value is also added to the CLK_2 DR value to obtain the total. The combination of all CLK_2DR inputs being High (17 dots) and both TB inputs being High (3 trailing blanks) is not allowed. The maximum CLK_2 period is 19 dot periods.

$DD_0 - DD_8$ **DOT DATA (inputs (9))**
The DD inputs accept parallel character dot matrix information for serial conversion for video output. DD data is accepted at the $TCLK_2/MCLK_2$ clock rate. DD_0 is shifted out first.

BS **BACKGROUND SELECT (input)**
The BS input specifies the color level of the background video. This input can be overridden by BLANK active.

VIDOUT, $\overline{\text{VIDOUT}}$ **VIDEO OUTPUT (analog outputs (2), non-TTL compatible)**
VIDOUT and $\overline{\text{VIDOUT}}$ outputs in a differential mode the composite blank, and video dot levels to a nominal 75Ω load impedance from switched current sources.

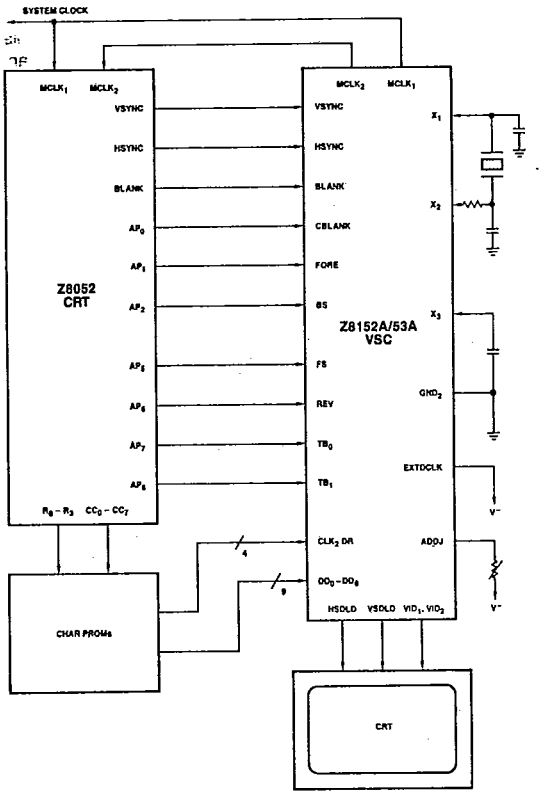
VID_1, VID_2 **VIDEO DIGITAL (outputs (2), (8152A-TTL; 8153A-ECL)**
VID_1 and VID_2 are digitally encoded outputs of the video out. VID_1 is the least significant bit. Encoding is as follows:

	VID_2 (VIDEO)	VID_1 (HIGHLIGHT)
Blank Level	0	0
Black	0	1
Grey	1	0
White	1	1

GRLVL **GREY LEVEL (input)**
The GRLVL input adjusts the current level output, via the VIDOUT and $\overline{\text{VIDOUT}}$ outputs, of the grey video level. There are two pre-selected grey levels; for GRLVL HIGH grey is brighter, for LOW grey is darker.

DW **DOUBLE WIDTH (inputs)**
The DW input, when active HIGH, causes the dot clock supplied to the $TCLK_2/MCLK_2$ clock divide to be divided by two. This function is used to facilitate doubling the width of a character cell matrix in the horizontal direction. The trailing blank information is also widened during a double width character.

Figure 4. Z8152A/53A Application with Z8052 CRT Controller



EXTDCLK **EXTERNAL DOT CLOCK (input, 8152A-TTL; 8153A-ECL)**
EXTDCLK is an external, TTL or ECL compatible dot clock input for use in multiple Z8152A/53A configurations. This signal replaces the internal oscillator function. To enable EXTDCLK both X_1 and X_3 must be grounded.

AADJ **ANALOG OUTPUTS CURRENT ADJUST (input, non – TTL compatible)**
Analog output current adjust is used for setting the analog video output current to 13.3mA. This is done by connecting AADJ to V^- via an applicable 1% resistor.

FUNCTIONAL DESCRIPTION

The Z8152A Video System Controller (VSC) supports both black and white and color video applications for CPUs, CRT controllers, and terminals. The essential functions of the VSC are to support proportional and non-proportional character display, to synchronize and mix character attributes with video, and to output the video in a four level analog or digital format.

PARALLEL PIXEL LOADING

Pixel information that must be serialized for video transmission is loaded into the serial shift register via inputs DD_0-DD_8. Information is loaded on both edges of the $MCLK_2$ character clock, as shown in Figure 3. The information set up on DD (0 : 7) prior to the falling edge of $MCLK_2$ is loaded into positions VID_9-VID_{16}. Note that DD_8 information is ignored. Information set up on DD(0:8) prior to the rising edge of $MCLK_2$ is loaded into positions VID_0-VID_8. Thus, up to 17 bits of pixel information can be loaded into the shift register. Note that if the character width is nine pixels or less the information captured on the falling edge of the $MCLK_2$ is not used. Any trailing blank insertion only occurs after the total number of pixels for the character

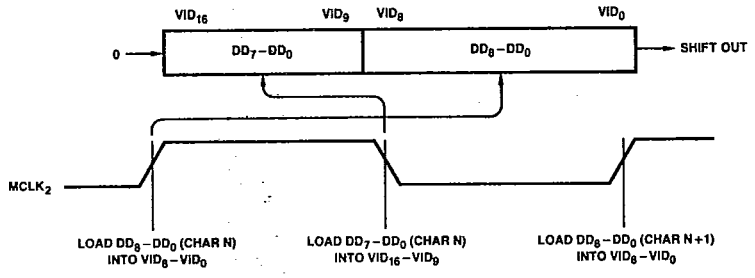
CLK_2DR (0 : 3) and TB (0 : 1) determine the divide ratio for the character clock. The sum of both values specifies the character clock period in dot clocks. During the trailing blank, the VSC shifts out what was loaded into the shift register. Therefore, it is the responsibility of the user to insure that the pixels output during the trailing blank dot period are set to the blank level.

VIDEO OPERATION

Parallel video data is obtained from the character ROM inputs; bits are shifted out serially and mixed with attribute information such as underline, shifted underline, and any other video sources. Video is internally encoded into one of four levels: White, Grey, Black and Blank. White is the highest analog current level, and Blank is the lowest. This information is then output through two ports (see Figure 5/6). One port provides a single current source output into a 75Ω impedance and the second port outputs either encoded TTL or ECL video on two pins.

There are two distinct blank inputs to the Z8152A/53A. BLANK is the CRTC's horizontal and vertical retrace period input which causes a blank output level to the display. CBLANK is an attribute input to selectively blank a character cell by forcing the video information for the particular character cell period to switch to the selected background color level.

Figure 5. Shift Register Loading



VIDEO INPUTS/OUTPUTS

Video information may be input in a number of different ways. Table 1 depicts all the combinations of video outputs achievable with each of the various inputs. The background color is determined by a separate pin input allowing either a black or white background. Using the REVERSE VIDEO (REV) input, a grey background can also be selected. The foreground then becomes black or white according to the signal on the foreground SHIFT line. Foreground and video sums can be modified depending on the combination of background, foreground shift, and reverse inputs. The user may apply any of his video inputs to the foreground to obtain a desired effect.

TABLE 1. Z8152A/53A VIDEO ATTRIBUTES

INPUTS				Z8152A/53A VIDEO ATTRIBUTES
BS	FS	REV	$\overline{CBLANK}$ (DD (0 : 8) + FORE)	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

SYSTEM TIMING

The CPU clock ($MCLK_1$) output is derived from an on-board oscillator by an externally programmable divide by two or three prescaler and a one to eight decoder. The internal oscillator is capable of operating a frequency of up to 100MHz and in a fundamental or third harmonic mode. Figure 4 shows the output waveform of $MCLK_1$ and $MCLK_2$.

The character clock ($MCLK_2$) output to the CRTC is frequency modulated according to the chosen number of dots per character cell. The duty cycle of $MCLK_2$ is 50% (±1 dot clock period) and is derived from an internal crystal driven oscillator whose divide ratio is set by the width of the character ROM plus the number of trailing blanks. A double width input further modifies $MCLK_2$ doubling the character width. During an active BLANK input $MCLK_2$ is internally re-synchronized to $MCLK_1$. This action aligns character cells at the left-end side of the display thereby eliminating "Dot Walk." The Vertical and Horizontal Sync (VSYNC, HSYNC) inputs from the CRT controller are buffered and delayed by a $MCLK_1$ or $MCLK_2$ clock period in order to phase correctly with the character video output.

PROPORTIONAL/VARIABLE SPACING

Proportional spacing is achieved by programming on a character-by-character basis, a number of two to twenty dot clock periods per character. The character ROM pixel information is selectable from two to seventeen per character. Up to three trailing blank pixels can be concatenated to the character ROM input, making it easier to provide a straight right margin for right justification of text.

COLOR APPLICATION

The Z8152A/53A may be used for many high-end color display applications. The foreground video and background information is mixed by the Z8152A/53A, and the encoded TTL video output can be used externally to select a color mix for the particular pixel being displayed. The horizontal and vertical synchronization, and video blank is output by the Z8152A/53A.

Figure 6. $MCLK_1$/$MCLK_2$ Output Waveform

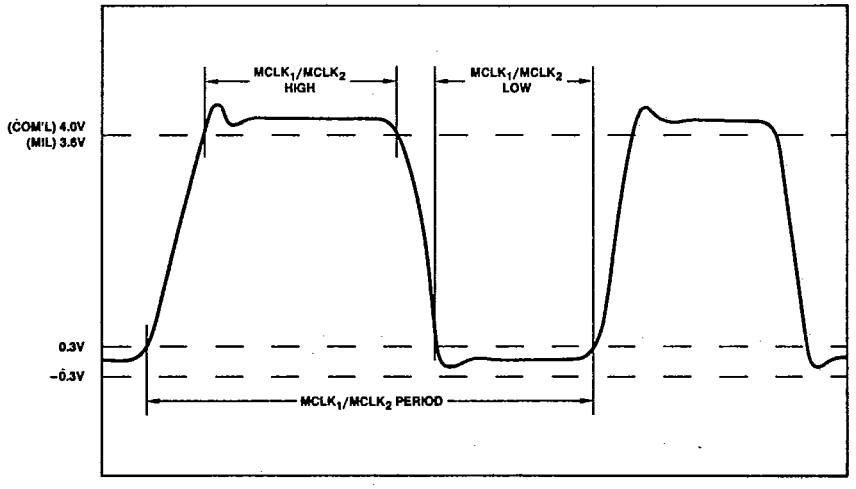
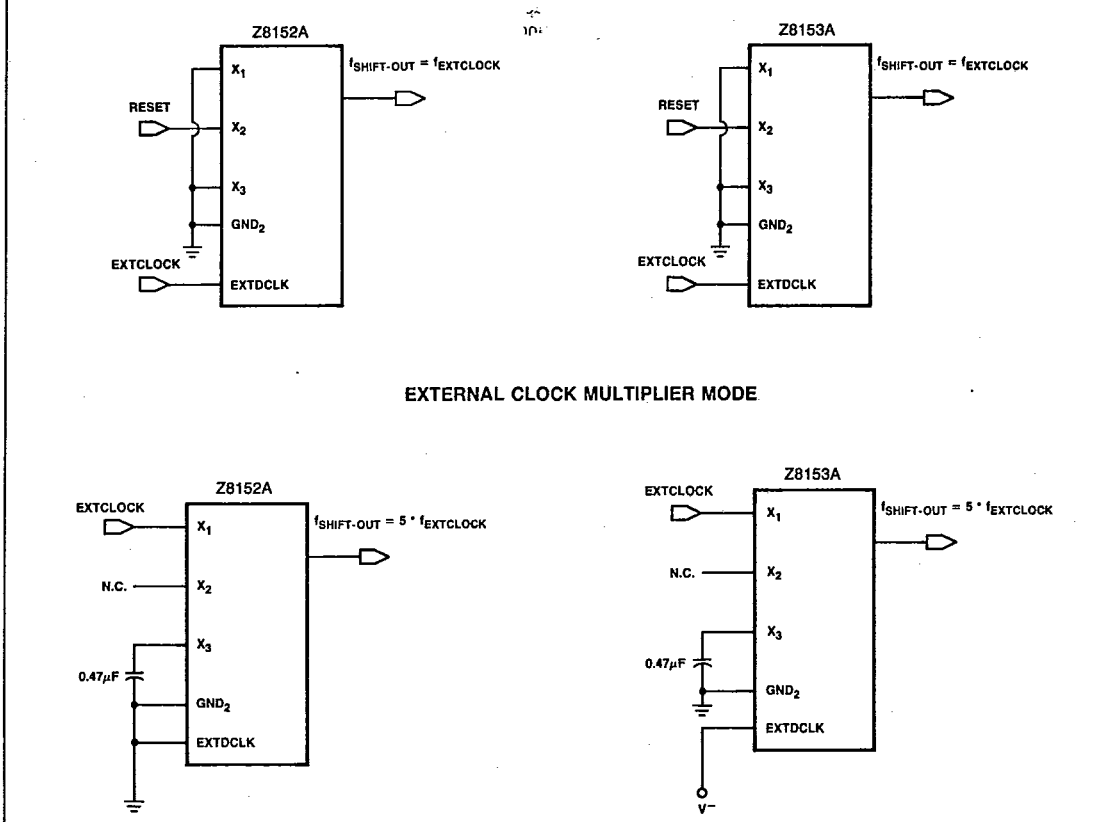


Figure 7. Dotclock Generation Mode



Z8152A

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC}
DC Input Voltage	−0.5 to +5.5V
DC Output Current into Outputs	30mA
DC Input Current	−30 to +5.0mA

Z8152A DC CHARACTERISTICS (See Note 4)

The following conditions apply unless otherwise specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (Min = 4.75V Max = 5.25V) V^- = 0V
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (Min = 4.50V Max = 5.50V) V^- = 0V

Parameters	Description	Test Conditions (Note 1)				Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min	$MCLK_1$ $MCLK_2$	I_{OH} = −0.1mA	MIL	3.6			Volts
					COM'L	4.0			Volts
			TTL Outputs	I_{OH} = −1mA	MIL	2.4	3.4		Volts
				I_{OH} = −2.6mA	COM'L	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min		I_{OL} = 0.1mA $MCLK_{1/2}$				0.3	Volts
				I_{OL} = 16mA TTL Outputs				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA						−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max V_{IN} = 0.4V		All Inputs (Except RES, EXTDCLK)				−0.4	mA
				RES, EXTDCLK				−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = Max V_{IN} = 2.7V		All Inputs (Except RES)				+50	μA
				RES				+600	μA
I_I	Input HIGH Current at Max Input Voltage	V_{CC} = Max V_{IN} = 5.5V						+1.0	mA
I_{SC}	Output Short Current Current (Note 3)	V_{CC} = Max		$MCLK_1$, $MCLK_2$		−50		−250	mA
				Others		−40		−130	mA
I_{CC}	Power Supply Current	V_{CC1} = Max V_{CC2} = Max		Over Operating Range				415	mA
				@ T_A = 70°C				375	mA
				@ T_C = 125°C				350	mA

Notes: 1. For conditions shown as Min or Max use the appropriate value specified under DC Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Except: X_1, X_2, X_3, AADJ, VIDOUT, $\overline{\text{VIDOUT}}$.

Z8153A

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC}
DC Input Voltage	−0.5 to +5.5V
DC Output Current into Outputs	30mA
DC Input Current	−30 to +5.0mA

Z8153A DC CHARACTERISTICS (See Note 4)

The following conditions apply unless otherwise specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (Min = 4.75V Max = 5.25V) V^- = −5.2V ±5% (Min = −4.94V Max = −5.46V)
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (Min = 4.50V Max = 5.50V) V^- = −5.2V ±10% (Min = − 4.68V Max = −5.72V)

Parameters	Description	Test Conditions (Note 1)				Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min	$MCLK_1$ $MCLK_2$	I_{OH} = −0.1mA	MIL	3.6			Volts
					COM'L	4.0			Volts
			TTL Outputs	I_{OH} = −1mA	MIL	2.4	3.4		Volts
				I_{OH} = −2.6mA	COM'L	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min		I_{OL} = 0.1mA $MCLK_{1/2}$				0.3	Volts
				I_{OL} = 16mA TTL Outputs				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA						−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max V_{IN} = 0.4V		All Inputs (Except RES)				−0.4	mA
				RES				−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = Max V_{IN} = 2.7V		All Inputs (Except RES)				+50	μA
				RES				+600	μA
I_I	Input HIGH Current at Max Input Voltage	V_{CC} = Max V_{IN} = 5.5V						+1.0	mA
I_{SC}	Output Short Current Current (Note 3)	V_{CC} = Max		$MCLK_1$, $MCLK_2$		−50		−250	mA
				Others		−40		−130	mA
I_{CC}	Power Supply Current	V_{CC1} = Max V_{CC2} = Max		Over Operating Range				410	mA
				@ T_A = 70°C				370	mA
				@ T_C = 125°C				345	mA
I^-	Power Supply Current	V^- = Max		Over Operating Range				40	mA
				@ T_A = 70°C				37	mA
				@ T_C = 125°C				35	mA

Notes: 1. For conditions shown as Min or Max use the appropriate value specified under DC Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Except: X_1, X_2, X_3, AADJ, VIDOUT, $\overline{\text{VIDOUT}}$.

Z8152A SWITCHING CHARACTERISTICS

OVER OPERATING RANGE (T_A = 0 to 70°C, V_{CC} = 5.0V ±5%, V^- = 0V)

Number	Description		Min	Max	Units
1	$MCLK_1$ Period		100		ns
2	CLK_2 Period		70		ns
3	$MCLK_1$ HIGH (See Note 5)	4.0V	38		ns
4	$MCLK_1$ LOW (See Notes 3 and 5)	0.3V	38		ns
5	$MCLK_2$ HIGH (See Note 6)	4.0V	23		ns
6	$MCLK_2$ LOW (See Notes 3 and 6)	0.3V	23		ns
7	Data to $MCLK_2$/$TCLK_2$ RE (See Note 1)		20		ns
8	$MCLK_2$/$TCLK_2$ to Data Not Valid		0		ns
9	VSYNC/HSYNC to $MCLK_1$ RE Setup (SSEL = HIGH)		20		ns
10	VSYNC/HSYNC to $MCLK_2$ RE Setup (SSEL = LOW)		20		ns
11	$TCLK_2$ RE to $MCLK_2$ RE Delay			8	ns
12	$TCLK_2$ FE to $MCLK_2$ FE Delay			12	ns
13	$MCLK_1$ to VSLD, HSLD (SSEL = HIGH)			6 + T_D	ns
14	$TCLK_2$ to VSLD, HSLD (SSEL = LOW)			6 + T_D	ns
15	DD(0:7) to $TCLK_2$ FE		20		ns
16	$TCLK_2$ RE to VID_1 VID_2 VAL (See Note 2)			6 + T_D	ns
17	BLANK FE to $MCLK_2$ RE Setup (SSEL = LOW)		20		ns
18	BLANK FE to $MCLK_1$ FE Setup (SSEL = HIGH)		20		ns
19	BLANK RE to $MCLK_1$ RE Setup (SSEL = HIGH)		20		ns
20	BLANK RE to $MCLK_2$ RE Setup (SSEL = LOW)		20		ns
22	VID_1 to VID_2 Skew		−5	+5	ns
24	EXTDCLK to $MCLK_1$			20	ns
25	EXTDCLK to $TCLK_2$			13	ns
26	EXTDCLK to $MCLK_2$			23	ns
27	EXTDCLK to VID_1/VID_2			13	ns
28	EXTDCLK to HSDLD/VSDLD (SSEL HI)			13	ns
29	EXTDCLK to HSDLD/VSDLD (SSEL LO)			13	ns
30	EXTDCLK to Data In Setup		9		ns
31	EXTDCLK to Data Not Valid Hold		11		ns
32	EXTDCLK to H/V SYNC Setup		10		ns
33	EXTDCLK Period		16.6		ns
34	EXTDCLK LOW Cycle		5		ns
35	EXTDCLK HIGH Cycle		5.0		ns
36	Reset Pulse Width (High)		10.0		ns
37	Reset Low to EXTDCLK Setup		8.0		ns

Notes: 1. Data includes CBLANK, FORE, REV, FS, DD_0–DD_8, TB0, TB1, BS, CLK_1DR, CLK_2DR, DW.
2. First Pixel of character. T_D is pixel period as defined by oscillator frequency.
3. Max undershoot on these outputs is guaranteed to be −0.3V.
4. T_D is the dot clock period.
5. Guaranteed to 100ns $MCLK_1$ cycle time.
6. Guaranteed to 70ns $MCLK_2$ cycle time (even divide ratio only).

Z8153A SWITCHING CHARACTERISTICS

OVER OPERATING RANGE (T_A = 0 to 70°C, V_{CC} = 5.0V ±5%, V^- = −5.25V ±5%)

Number	Description		Min	Max	Units
1	$MCLK_1$ Period		100		ns
2	CLK_2 Period		70		ns
3	$MCLK_1$ HIGH (See Note 5)	4.0V	38		ns
4	$MCLK_1$ LOW (See Notes 3 and 5)	0.3V	38		ns
5	$MCLK_2$ HIGH (See Note 6)	4.0V	23		ns
6	$MCLK_2$ LOW (See Notes 3 and 6)	0.3V	23		ns
7	Data to $MCLK_2$/$TCLK_2$ RE (See Note 1)		20 +T_D (See Note 4)		ns
8	$MCLK_2$/$TCLK_2$ to Data Not Valid		0		ns
9	VSYNC/HSYNC to $MCLK_1$ RE Setup (SSEL = HIGH)		20 +T_D		ns
10	VSYNC/HSYNC to $MCLK_2$ RE Setup (SSEL = LOW)		20 +T_D		ns
11	$TCLK_2$ RE to $MCLK_2$ RE Delay			8	ns
12	$TCLK_2$ FE to $MCLK_2$ FE Delay			12	ns
13	$MCLK_1$ to VSLD, HSLD (SSEL = HIGH)			6	ns
14	$TCLK_2$ to VSLD, HSLD (SSEL = LOW)			6	ns
15	DD(0:7) to $TCLK_2$ FE		20 +T_D		ns
16	$TCLK_2$ RE to VID_1 VID_2 VAL (See Note 2)			6	ns
17	BLANK FE to $MCLK_2$ RE Setup (SSEL = LOW)		20 +T_D		ns
18	BLANK FE to $MCLK_1$ FE Setup (SSEL = HIGH)		20 +T_D		ns
19	BLANK RE to $MCLK_1$ RE Setup (SSEL = HIGH)		20 +T_D		ns
20	BLANK RE to $MCLK_2$ RE Setup (SSEL = LOW)		20 +T_D		ns
21	VID_1 to VID_2 Skew		−2	+2	ns
24	EXTDCLK to $MCLK_1$			20	ns
25	EXTDCLK to $TCLK_2$			10	ns
26	EXTDCLK to $MCLK_2$			23	ns
27	EXTDCLK to VID_1/VID_2			8	ns
28	EXTDCLK to HSDLD/VSDLD (SSEL HI)			10	ns
29	EXTDCLK to HSDLD/VSDLD (SSEL LO)			10	ns
30	EXTDCLK to Data in Setup		9		ns
31	EXTDCLK to Data Not Valid Hold		11		ns
32	EXTDCLK to H/V SYNC Setup		10		ns
33	EXTDCLK Period		10		ns
34	EXTDCLK LOW Cycle		5		ns
35	EXTDCLK HIGH Cycle		3.5		ns
36	Reset Pulse Width (High)		10.0		ns
37	Reset Low to EXTDCLK Setup		8.0		ns

Notes: 1. Data includes CBLANK, FORE, REV, FS, DD_0−DD_8, TB0, TB1, BS, CLK_1DR, CLK_2DR, DW.
2. First Pixel of character. T_D is pixel period as defined by oscillator frequency.
3. Max undershoot on these outputs is guaranteed to be −0.3V.
4. T_D is the dot clock period.
5. Guaranteed to 100ns $MCLK_1$ cycle time.
6. Guaranteed to 70ns $MCLK_2$ cycle time (even divide ratio only).

Figure 8. Switching Test Circuits

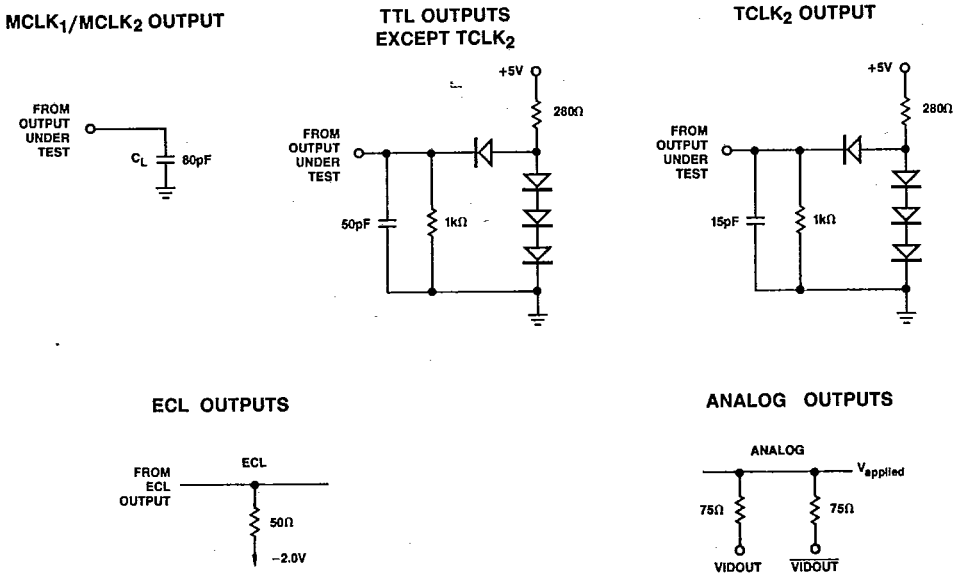


Figure 9. Z8152A/53A Timing
(Parameters Measured with Respect to EXTDCLK)

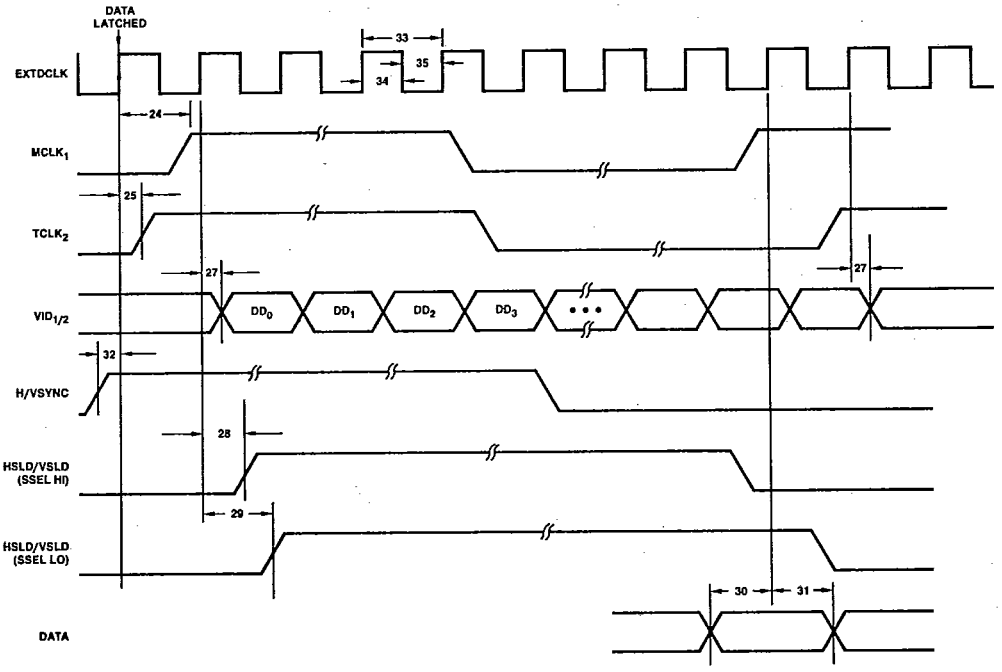


Figure 10. Switching Time Diagram—$MCLK_1/MCLK_2$

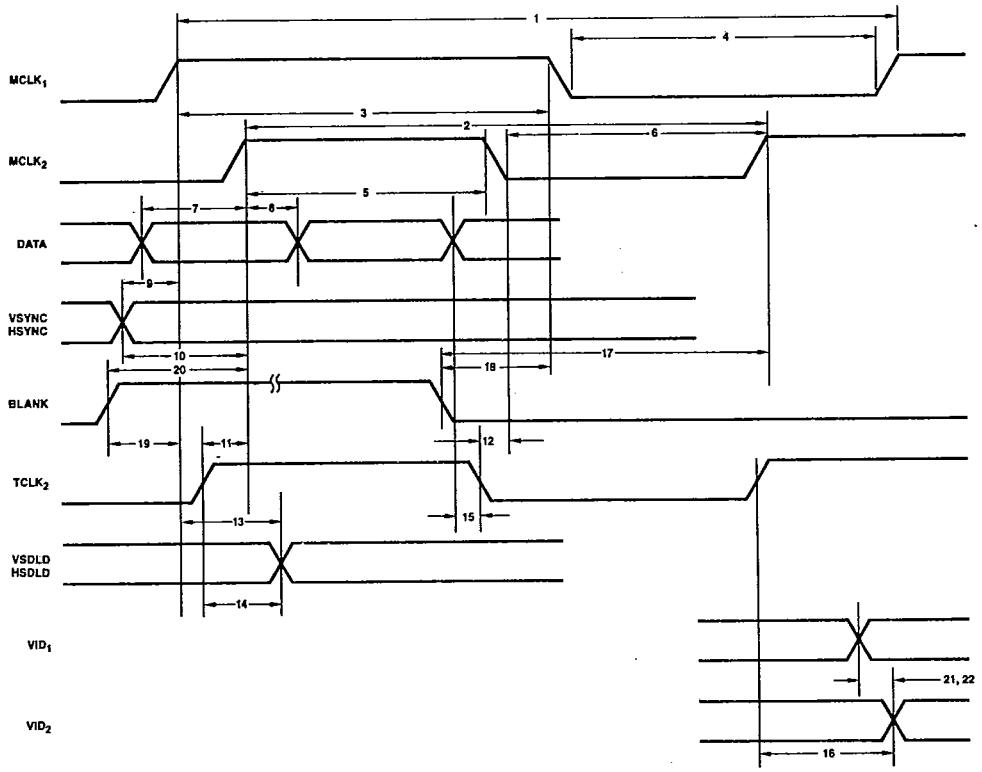


Figure 11. VSC CLK_2 Synchronization (Only Occurs If SSEL Is High)

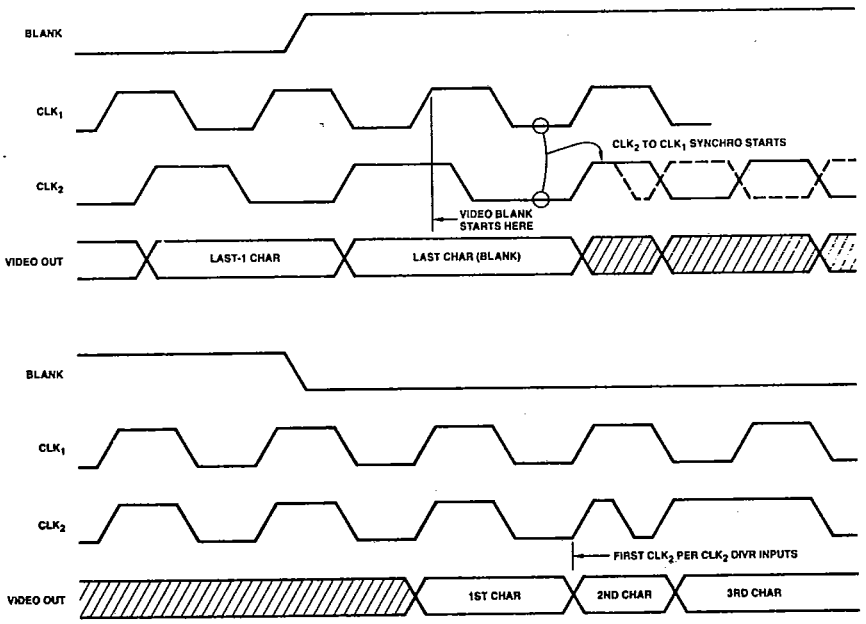


Figure 12. Analog Video Outputs and Digital Video Outputs for Z8152A

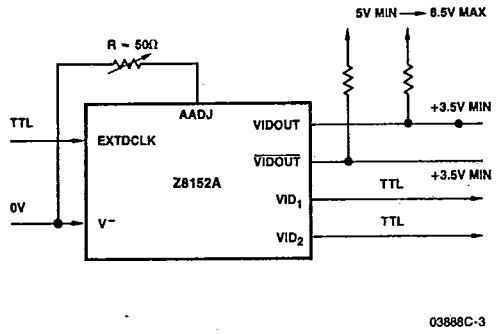
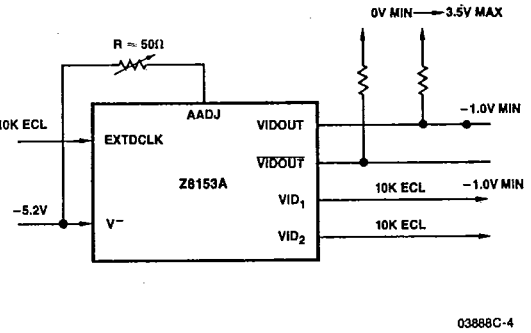


Figure 13. Analog Video Outputs and Digital Video Outputs for Z8153A



ANALOG ELECTRICAL CHARACTERISTICS (see notes)

The following conditions apply unless otherwise specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (Min = 4.75V Max = 5.25V) Am8152A: V^- = 0V Z8153A: V^- = −5.2V ±5%
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (Min = 4.50V Max = 5.50V) V^- = 0V V^- = −5.2V ±10%

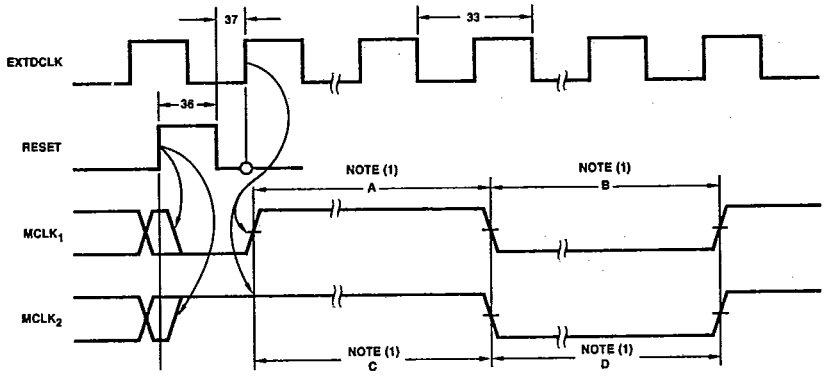
Grey Level	VID_2	VID_1		VIDOUT Min (%)	VIDOUT Max (%)	$\overline{VIDOUT}$ Min (%)	$\overline{VIDOUT}$ Max (%)
X	I	I	I_{White}	0	0	100	100
I	I	O	I_{Grey1}	37	44	56	63
O	I	O	I_{Grey2}	45	53	47	55
X	O	I	I_{Black}	90.5	92.5	7.5	9.5
X	O	O	I_{Blank}	100	100	0	0

DRIFT OVER OPERATING CONDITIONS (For particular part)

Grey Level	VID_2	VID_1		VIDOUT	$\overline{VIDOUT}$
X	I	I	I_{White}	0	0
I	I	O	I_{Grey1}	2% Max	2% Max
O	I	O	I_{Grey2}	2% Max	2% Max
X	O	I	I_{Black}	1% Max	1% Max
X	O	O	I_{Blank}	0	0

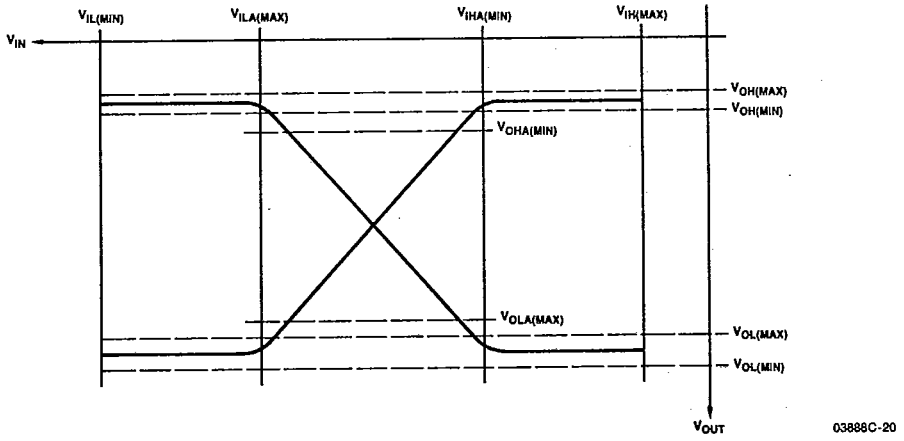
Notes:
1. Test Condition: Normal I_{White} for $\overline{VIDOUT}$ + 13.3mA.
2. Positive current flowing into VIDOUT/$\overline{VIDOUT}$.
3. t_R, t_F = 5ns Max.
4. $\overline{VIDOUT}$ output currents normalized to I_{White}. VIDOUT output currents normalized to I_{Blank}.
5. Min/Max values for VIDOUT and $\overline{VIDOUT}$ account for variation of different devices.
6. Z8152A
   V Pull-Up: 8.5V ≥ V Pull-Up ≥ V_{CC}
   VIDOUT/$\overline{VIDOUT}$: (V Pull-Up) ≥ VIDOUT/$\overline{VIDOUT}$ ≥ (V_{CC} − 1V)
7. Z8153A
   V Pull-Up: 3.5V ≥ V Pull-Up ≥ 0V
   VIDOUT/$\overline{VIDOUT}$: (V Pull-Up) ≥ VIDOUT/$\overline{VIDOUT}$ ≥ −1.0V

RESET TIMING FOR Z8152A/53A



Note 1. See pin description on page 3.

Z8153A 10K ECL SPECIFICATIONS



DC CHARACTERISTICS

COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±5% GND = 0V V^- = −5.2V ±5% (Max = −5.46, Min = −4.94)
MIL T_C = −55 to 125°C V_{CC} = 5.0V ±10% GND = 0V V^- = −5.2V ±10% (Max = −5.72, Min = −4.68)

	Parameters	Test Conditions	−55°C	0°C	25°C	70°C	125°C	Unit
10K ECL Outputs	V_{OH} (Max)	50Ω to −2V	−880	−840	−780	−720	−630	mV
	V_{OH} (Min)		−1080	−1000	−930	−900	−825	mV
	V_{OHA} (Min)		−1100	−1020	−950	−920	−845	mV
VID_1 and VID_2	V_{OLA} (Max)	50Ω to −2V	−1635	−1645	−1600	−1605	−1525	mV
	V_{OL} (Max)		−1655	−1665	−1620	−1625	−1545	mV
	V_{OL} (Min)		−1920	−1870	−1850	−1830	−1820	mV
10K ECL Input	V_{IH} (Max)		−880	−840	−780	−720	−630	mV
	V_{IHA} (Min)		−1255	−1145	−1105	−1045	−1000	mV
EXTDCLK	V_{ILA} (Max)		−1510	−1490	−1475	−1450	−1400	mV
	V_{IL} (Min)		−1920	−1870	−1850	−1830	−1820	mV
	I_{IH}	V^- = Max, $V_{IN} = V_{IH}$ (Max)	200	200	200	200	200	μA
	I_{IL}	V^- = Max, $V_{IN} = V_{IL}$ (Min)	150	150	150	150	150	μA

ORDERING INFORMATION

Z8152A/53A VSC
48-pin DIP
Z8152A CS
Z8153A CS

Codes

First letter is for package; second letter is for temperature.

C = Ceramic DIP
P = Plastic DIP
L = Ceramic LCC
V = Plastic PCC

R = Protopack
T = Low Profile Protopack
DIP = Dual-In-Line Package
LCC = Leadless Chip Carrier
PCC = Plastic Chip Carrier (Leaded)

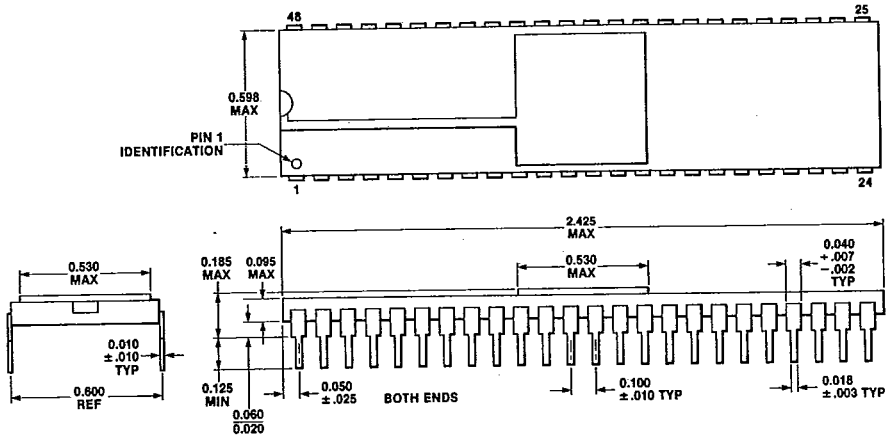
TEMPERATURE
S = 0°C to +70°C
E = −40°C to +85°C
M*= −55°C to +125°C

FLOW
B = 883 Class B

Example: PS is a plastic DIP, 0°C to +70°C.

*For Military Orders, contact your local Zilog Sales Office for Military Electrical Specifications.

PACKAGE INFORMATION



48-Pin Dual-In-Line Package (DIP), Ceramic

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.