T-49-17-07

Z8400 Military Z80® CPU Central Processing Unit

Zilog

Military Electrical Specification

July 1985

FEATURES

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.
- 2.5 MHz and 4 MHz clocks for the Z80 and Z80A CPU result in rapid instruction execution with consequent high data throughput.
- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers, together with indexed and relative addressing, result in the most powerful data handling capabilities in the microcomputer industry.
- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.
- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays.
- There are three modes of high speed interrupt processing: 8080 compatible, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.
- On-chip dynamic memory refresh counter.

GENERAL DESCRIPTION

The Z80 and Z80A CPUs are third-generation single-chip microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5 V power source, all output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers. The internal block diagram (Figure 1) shows the primary functions of the Z80 processors. Subsequent text provides more detail on the Z80 I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

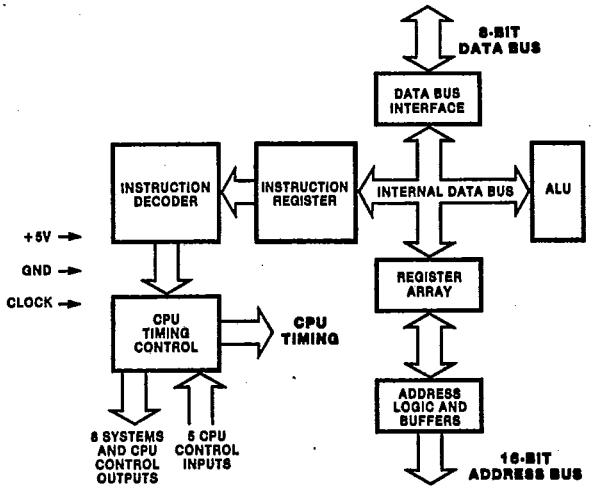


Figure 1. Z80 CPU Block Diagram

CPU TIMING

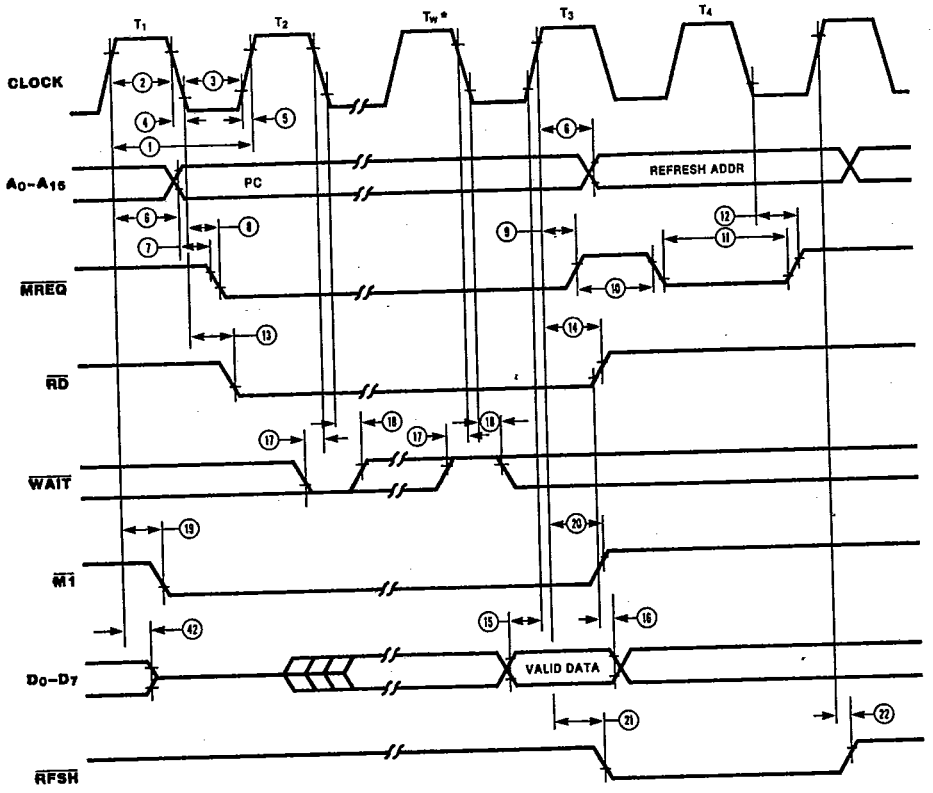
The CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Opcode Fetch. The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 2). Approximately one-half clock cycle later, $\overline{MREQ}$ goes active. When active, $\overline{RD}$ indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the $\overline{WAIT}$ input with the falling edge of clock state T_2. During clock states T_3 and T_4 of an $\overline{M1}$ cycle dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction. When the Refresh Control signal becomes active, refreshing of dynamic memory can take place.



*T_W = Wait cycle added when necessary for slow ancillary devices.

Figure 2. Instruction Opcode Fetch

Memory Read or Write Cycles. Figure 3 shows the timing of memory read or write cycles other than an opcode fetch ($\overline{M1}$) cycle. The $\overline{MREQ}$ and $\overline{RD}$ signals function exactly as in the fetch cycle. In a memory write cycle, $\overline{MREQ}$ also becomes active when the address bus is stable. The $\overline{WR}$ line is active when the data bus is stable, so that it can be used directly as an R/$\overline{W}$ pulse to most semiconductor memories.

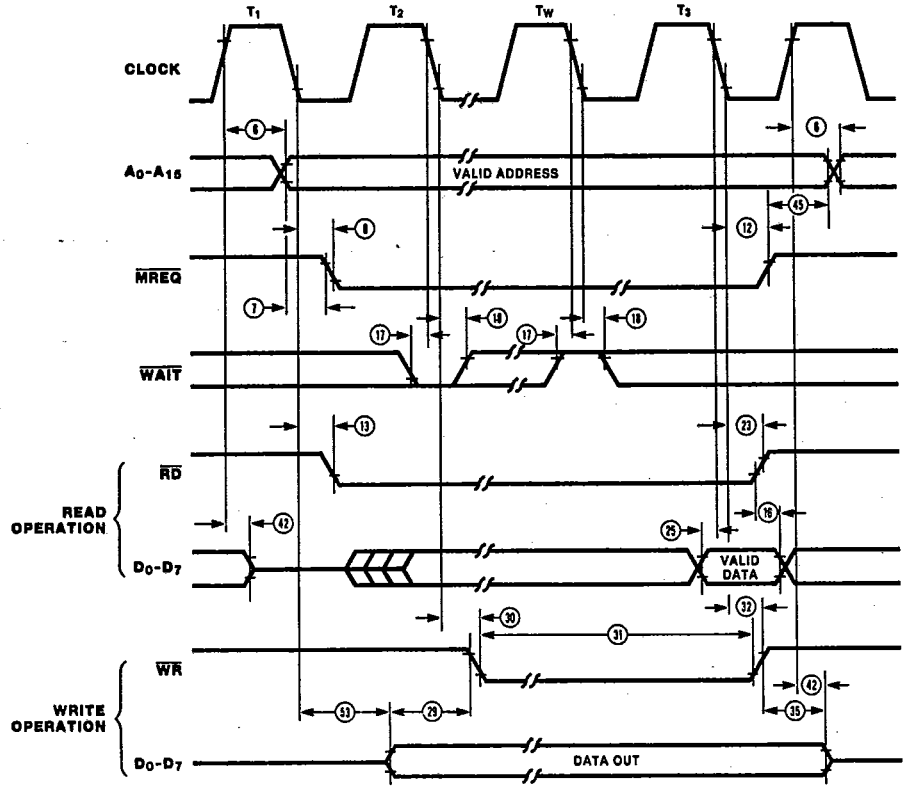
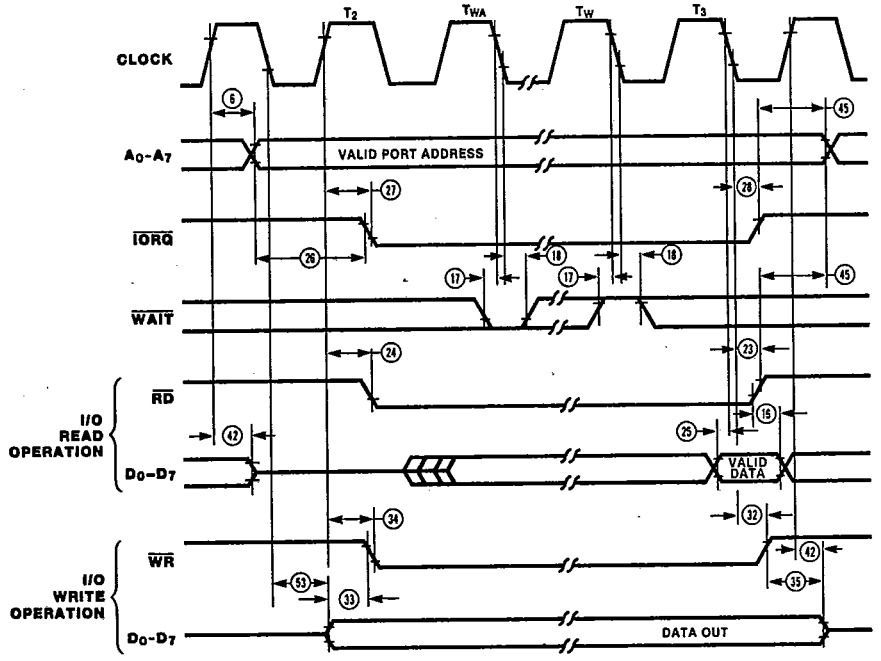


Figure 3. Memory Read or Write Cycles

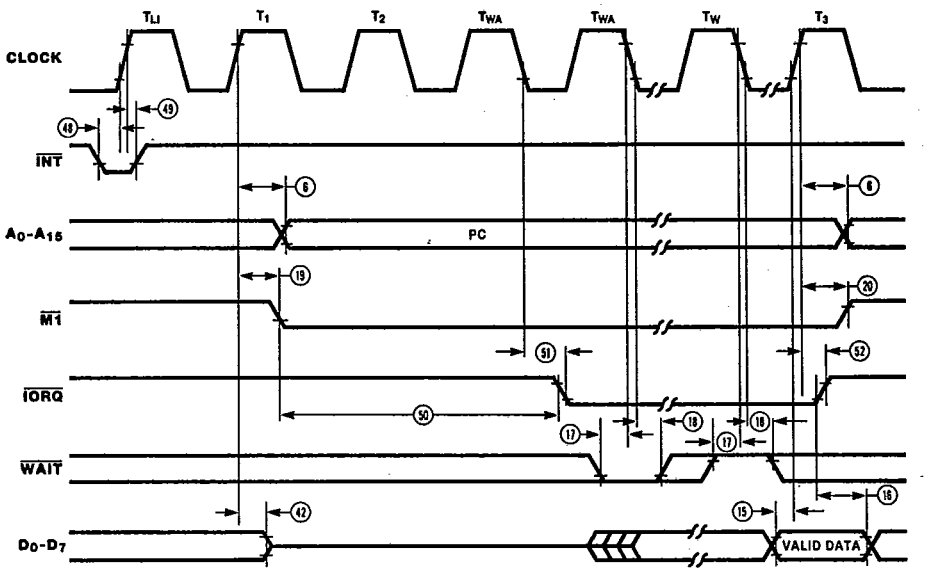
Input or Output Cycles. Figure 4 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_{WA}). This extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.



T_{WA} = One wait cycle automatically inserted by CPU.

Figure 4. Input or Output Cycles

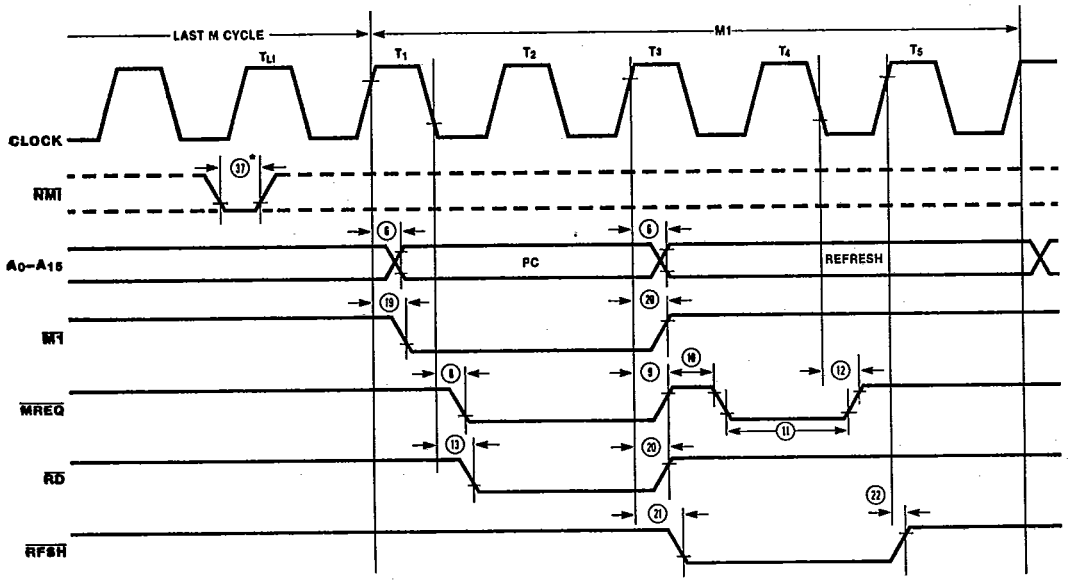
Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 5). When an interrupt is accepted, a special $\overline{M1}$ cycle is generated. During this $\overline{M1}$ cycle, $\overline{IORQ}$ becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.



NOTES: 1) T_{LI} = Last state of any instruction cycle.
2) T_{WA} = Wait cycle automatically inserted by CPU.

Figure 5. Interrupt Request/Acknowledge Cycle

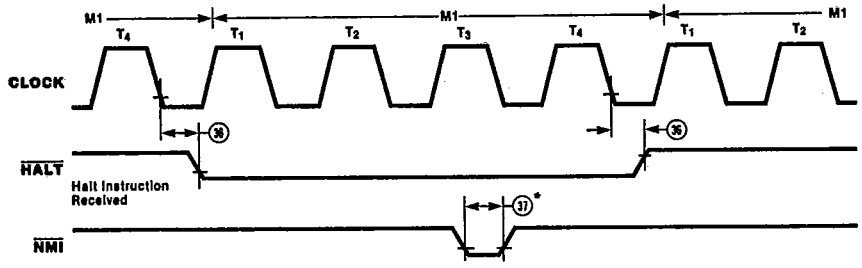
Non-Maskable Interrupt Request Cycle. $\overline{NMI}$ is sampled at the same time as the maskable interrupt input $\overline{INT}$ but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal instruction fetch except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the $\overline{NMI}$ service routine located at address 0066H (Figure 6).



*Although $\overline{NMI}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no late than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 6. Non-Maskable Interrupt Request Operation

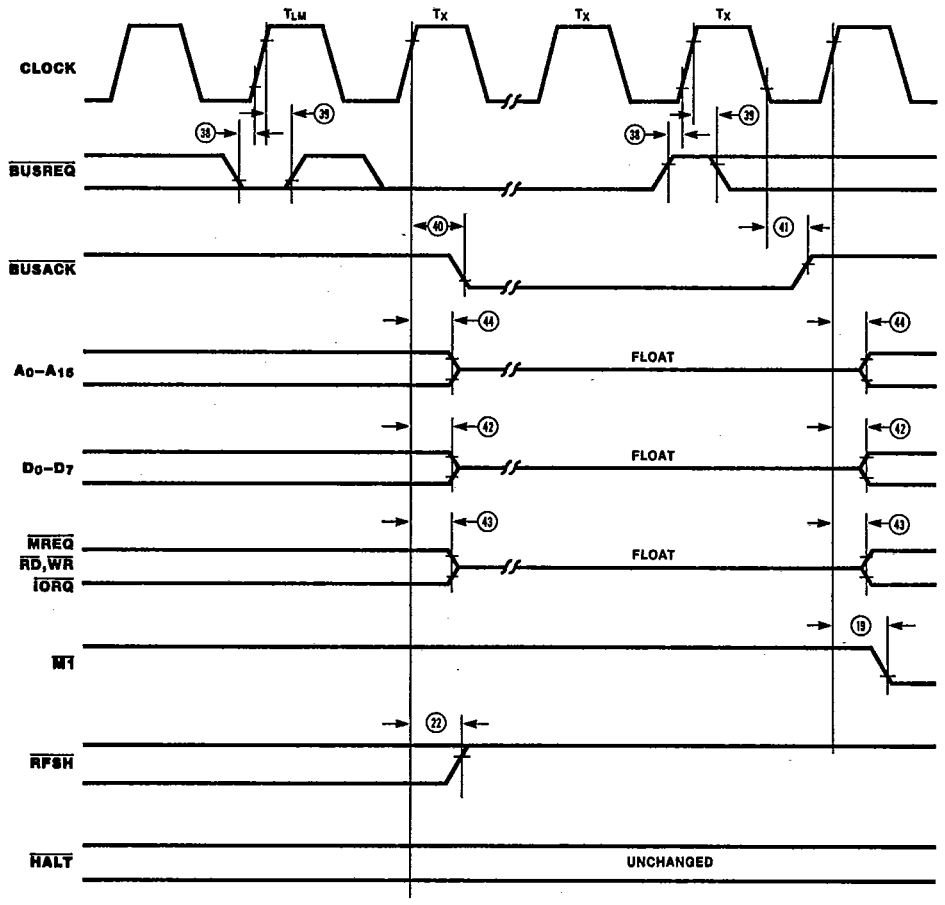
Halt Acknowledge Cycle. When the CPU receives a Halt instruction, it executes NOP states until either an $\overline{INT}$ or $\overline{NMI}$ input is received. When in the Halt state, the $\overline{HALT}$ output is active and remains so until an interrupt is received (Figure 7). INT will also force a Halt exit.



*Although $\overline{NMI}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 7. Halt Acknowledge Cycle

Bus Request/Acknowledge Cycle. The CPU samples $\overline{BUSREQ}$ with the rising edge of the last clock period of any machine cycle (Figure 8). If $\overline{BUSREQ}$ is active, the CPU sets its address, data, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ lines to a high-impedance state with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.



NOTES: 1) T_{LM} = Last state of any M cycle.
2) T_X = An arbitrary clock cycle used by requesting device.

Figure 8. Z-BUS Request/Acknowledge Cycle

Reset Cycle. $\overline{\text{RESET}}$ must be active for at least three clock cycles for the CPU to properly accept it. As long as $\overline{\text{RESET}}$ remains active, the address and data buses float, and the control outputs are inactive. Once $\overline{\text{RESET}}$ goes inactive, three internal T cycles are consumed before the CPU resumes normal processing operation. $\overline{\text{RESET}}$ clears the PC register, so the first opcode fetch will be to location 0000H (Figure 9).

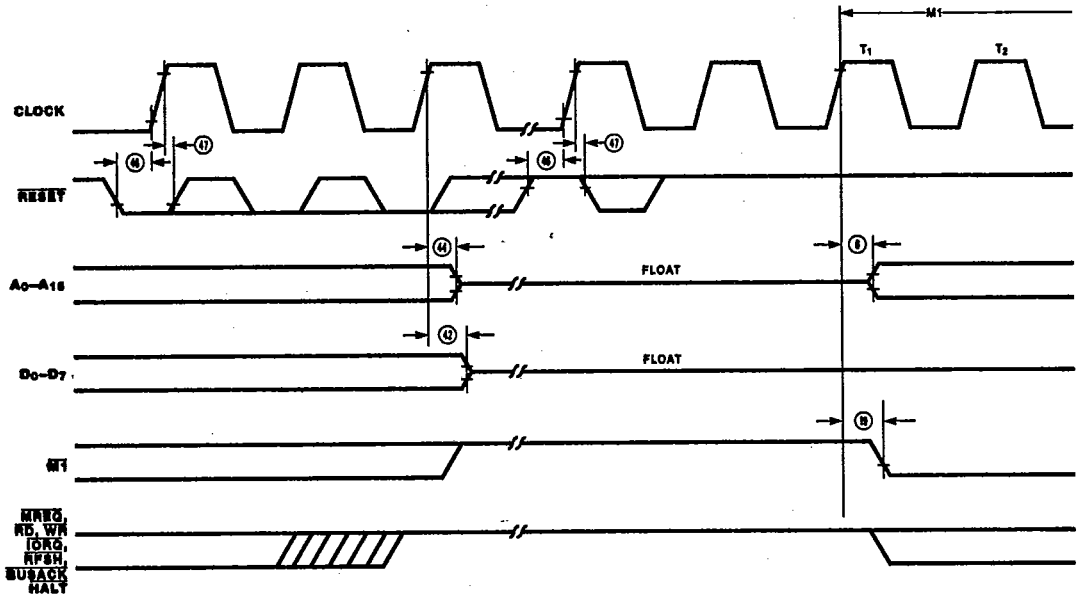


Figure 9. Reset Cycle

ABSOLUTE MAXIMUM RATINGS

Guaranteed by characterization/design.

Voltages on all pins with respect to ground ..... .0.3V to +7V
Operating Case Temperature ..... −55°C to −125°C
Storage Temperature Range ..... −65°C to +150°C
Absolute Maximum Power Dissipation ..... 1.5 W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and Capacitance sections below apply for the following standard test conditions, unless otherwise noted.

Military Operating Temperature Range (T_C)
−55°C to +125°C

Standard Military Test Condition
$+4.5V \leq V_{CC} \leq +5.5V$

All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pf. Add 15 ns delay for each 50 pf increase in load up to a maximum of 200 pf for the data bus. AC timing measurements are referenced to 1.5 volts.

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3[c]	0.45[a]	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−.6[a]	V_{CC}+.3[a]	V	
V_{IL}	Input Low Voltage	−0.3[c]	0.8[a]	V	
V_{IH}	Input High Voltage	2.2[a]	V_{CC}[a]	V	
V_{OL}	Output Low Voltage		0.4[a]	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4[a]		V	I_{OH} = −250 μA
I_{CC}	Power Supply Current		200[a]	mA	Note 2
I_{LI}	Input Leakage Current		10[a]	μA	V_{IN} = 0.4 to V_{CC}
I_{LO}	3-State Output Leakage Current in Float	−10[a]	10[1a]	μA	V_{OUT} = 0.2 to V_{CC}

1. A_{15}-A_0, D_7-D_0, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$.
2. Measurements made with outputs floating.

CAPACITANCE

Symbol	Parameter	Min	Max	Unit
C_{CLOCK}	Clock Capacitance		35[c]	pf
C_{IN}	Input Capacitance		5[c]	pf
C_{OUT}	Output Capacitance		15[c]	pf

NOTES:
T_A = 25°C, f = 1 MHz.
Unmeasured pins returned to ground.

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design

AC CHARACTERISTICS†

Number	Symbol	Parameter	Z80 CPU Min	Z80 CPU Max	Z80A CPU Min	Z80A CPU Max
1	TcC	Clock Cycle Time	400a*		250a*	
2	TwCh	Clock Pulse Width (High)	180a		110a	
3	TwCl	Clock Pulse Width (Low)	180a	1000a	110a	1000a
4	TfC	Clock Fall Time		30c		30c
5	TrC	Clock Rise Time		30c		30c
6	TdCr(A)	Clock ↑ to Address Valid Delay		145a		110a
7	TdA(MREQf)	Address Valid to $\overline{MREQ}$ ↓ Delay	125c*		65c*	
8	TdCf(MREQf)	Clock ↓ to $\overline{MREQ}$ ↓ Delay		100a		85a
9	TdCr(MREQr)	Clock ↑ to $\overline{MREQ}$ ↑ Delay		100a		85a
10	TwMREQh	$\overline{MREQ}$ Pulse Width (High)	170c*		110c*	
11	TwMREQl	$\overline{MREQ}$ Pulse Width (Low)	360c*		220c*	
12	TdCf(MREQr)	Clock ↓ to $\overline{MREQ}$ ↑ Delay		100a		85a
13	TdCf(RDf)	Clock ↓ to $\overline{RD}$ ↓ Delay		130a		95a
14	TdCr(RDr)	Clock ↑ to $\overline{RD}$ ↑ Delay		100a		85a
15	TsD(Cr)	Data Setup Time to Clock ↑	50a		35a	
16	ThD(RDr)	Data Hold Time to $\overline{RD}$ ↑		0c		0c
17	TsWAIT(Cf)	$\overline{WAIT}$ Setup Time to Clock ↓	70a		70a	
18	ThWAIT(Cf)	$\overline{WAIT}$ Hold Time after Clock ↓		0c		0c
19	TdCr(M1f)	Clock ↑ to $\overline{M1}$ ↓ Delay		130a		100a
20	TdCr(M1r)	Clock ↑ to $\overline{M1}$ ↑ Delay		130a		100a
21	TdCr(RFSHf)	Clock ↑ to $\overline{RFSH}$ ↓ Delay		180a		130a
22	TdCr(RFSHr)	Clock ↑ to $\overline{RFSH}$ ↑ Delay		150a		120a
23	TdCf(RDr)	Clock ↓ to $\overline{RD}$ ↑ Delay		110a		85a
24	TdCr(RDf)	Clock ↑ to $\overline{RD}$ ↓ Delay		100a		85a
25	TsD(Cf)	Data Setup to Clock ↓ during M_2, M_3, M_4, or M_5 Cycles	60a		50a	
26	TdA(IORQf)	Address Stable prior to $\overline{IORQ}$ ↓	320c*		180c*	
27	TdCr(IORQf)	Clock ↑ to $\overline{IORQ}$ ↓ Delay		90a		75a
28	TdCf(IORQr)	Clock ↓ to $\overline{IORQ}$ ↑ Delay		110a		85a
29	TdD(WRf)	Data Stable prior to $\overline{WR}$ ↓	190c*		80c*	
30	TdCf(WRf)	Clock ↓ to $\overline{WR}$ ↓ Delay		90a		80a
31	TwWR	$\overline{WR}$ Pulse Width	360c*		220c*	
32	TdCf(WRr)	Clock ↓ to $\overline{WR}$ ↑ Delay		100a		80a
33	TdD(WRf)	Data Stable prior to $\overline{WR}$ ↓	20c*		-10c*	
34	TdCr(WRf)	Clock ↑ to $\overline{WR}$ ↓ Delay		80a		65a
35	TdWRr(D)	Data Stable from $\overline{WR}$ ↑	120c*		60c*	
36	TdCf(HALT)	Clock ↓ to $\overline{HALT}$ ↑ or ↓		300a		300a
37	TwNMI	$\overline{NMI}$ Pulse Width	160c		160c	
38	TsBUSREQ(Cr)	$\overline{BUSREQ}$ Setup Time to Clock ↑	80a		50a	

*For clock periods other than the minimums shown, calculate parameters using the table on the following page. Calculated values above assumed TrC = TfC = 20 ns.

†Units in nanoseconds (ns).

Parameter Test Status:

a Tested

b Guaranteed

c Guaranteed by Characterization/Design

AC CHARACTERISTICS† (Continued)

Number	Symbol	Parameter	Z80 CPU Min	Z80 CPU Max	Z80A CPU Min	Z80A CPU Max
39	ThBUSREQ(Cr)	$\overline{BUSREQ}$ Hold Time after Clock ↑	0[c]		0[c]	
40	TdCr(BUSACKf)	Clock ↑ to $\overline{BUSACK}$ ↓ Delay		120[a]		100[a]
41	TdCf(BUSACKr)	Clock ↓ to $\overline{BUSACK}$ ↑ Delay		110[a]		100[a]
42	TdCr(Dz)	Clock ↑ to Data Float Delay		90[c]		90[c]
43	TdCr(CTz)	Clock ↑ to Control Outputs Float Delay ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$)		110[c]		80[c]
44	TdCr(Az)	Clock ↑ to Address Float Delay		110[c]		90[c]
45	TdCTr(A)	$\overline{MREQ}$ ↑, $\overline{IORQ}$ ↑, $\overline{RD}$ ↑, and $\overline{WR}$ ↑ to Address Hold Time	160[c]*		80[c]*	
46	TsRESET(Cr)	$\overline{RESET}$ to Clock ↑ Setup Time	90[a]		60[a]	
47	ThRESET(Cr)	$\overline{RESET}$ to Clock ↑ Hold Time		0[c]		0[c]
48	TsINTf(Cr)	$\overline{INT}$ to Clock ↑ Setup Time	80[a]		80[a]	
49	ThINTr(Cr)	$\overline{INT}$ to Clock ↑ Hold Time		0[c]		0[c]
50	TdM1f(IORQf)	$\overline{M1}$ ↓ to $\overline{IORQ}$ ↓ Delay	920[c]*		565[c]*	
51	TdCf(IORQf)	Clock ↓ to $\overline{IORQ}$ ↓ Delay		110[a]		85[a]
52	TdCf(IORQr)	Clock ↑ $\overline{IORQ}$ ↑ Delay		100[a]		85[a]
53	TdCf(D)	Clock ↓ to Data Valid Delay		230[a]		150[a]

*For clock periods other than the minimums shown, calculate parameters using the following table. Calculated values above assumed TrC = TfC = 20 ns.
†Units in nanoseconds (ns).

Parameter Test Status:
- a Tested
- b Guaranteed
- c Guaranteed by Characterization/Design

FOOTNOTES TO AC CHARACTERISTICS

Number	Symbol	Z80	Z80A
1	TcC	TwCh + TwCl + TrC + TfC	TwCh + TwCl + TrC + TfC
7	TdA(MREQf)	TwCh + TfC – 75	TwCh + TfC – 65
10	TwMREQh	TwCh + TfC – 30	TwCh + TfC – 20
11	TwMREQl	TcC – 40	TcC – 30
26	TdA(IORQf)	TcC – 80	TcC – 70
29	TdD(WRf)	TcC – 210	TcC – 170
31	TwWR	TcC – 40	TcC – 30
33	TdD(WRf)	TwCl + TrC – 180	TwCl + TrC – 140
35	TdWRr(D)	TwCl + TrC – 80	TwCl + TrC – 70
45	TdCTr(A)	TwCl + TrC – 40	TwCl + TrC – 50
50	TdMIf(IORQf)	2TcC + TwCh + TfC – 80	2TcC + TwCh + TfC – 65

AC Test Conditions:

V_{IH} = 2.2 V	V_{OH} = 1.5 V
V_{IL} = 0.8 V	V_{OL} = 1.5 V
$V_{IHC} = V_{CC} - 0.6$ V	FLOAT = ±0.5 V
V_{ILC} = 0.45 V	

PIN DESCRIPTIONS

A_0-A_{15}. *Address Bus* (output, active High, 3-state). A_0-A_{15} form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

BUSACK. *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals MREQ, IORQ, RD, and WR have entered their high-impedance states. The external circuitry can now control these lines.

BUSREQ. *Bus Request* (input, active Low). Bus Request has a higher priority than NMI and is always recognized at the end of the current machine cycle. BUSREQ forces the CPU address bus, data bus, and control signals MREQ, IORQ, RD, and WR to go to a high-impedance state so that other devices can control these lines. BUSREQ is normally wired-OR and requires an external pullup for these applications. Extended BUSREQ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D_0-D_7. *Data Bus* (input/output, active High, 3-state). D_0-D_7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

Halt. *Halt State* (output, active Low). HALT indicates that the CPU has executed a Halt instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

INT. *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. INT is normally wired-OR and requires an external pullup for these applications.

IORQ. *Input/Output Request* (output, active Low, 3-state). IORQ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. IORQ is also generated concurrently with M1 during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

M1. *Machine Cycle One* (output, active Low). M1, together with MREQ, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. M1, together with IORQ, indicates an interrupt acknowledge cycle.

MREQ. *Memory Request* (output, active Low, 3-state). MREQ indicates that the address bus holds a valid address for a memory read or memory write operation.

NMI. *Non-Maskable Interrupt* (input, negative edge-triggered). NMI has a higher priority than INT. NMI is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

RD. *Read* (output, active Low, 3-state). RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

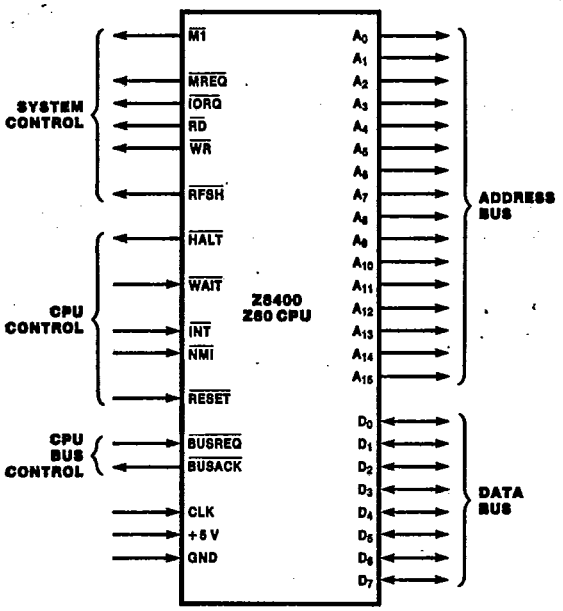
RESET. *Reset* (input, active Low). RESET initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that RESET must be active for a minimum of three full clock cycles before the reset operation is complete.

RFSH. *Refresh* (output, active Low). RFSH, together with MREQ, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

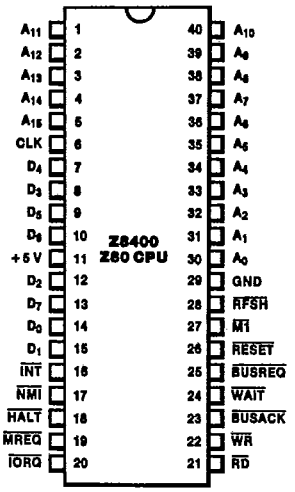
WAIT. *Wait* (input, active Low). WAIT indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended WAIT periods can prevent the CPU from refreshing dynamic memory properly.

WR. *Write* (output, active Low, 3-state). WR indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

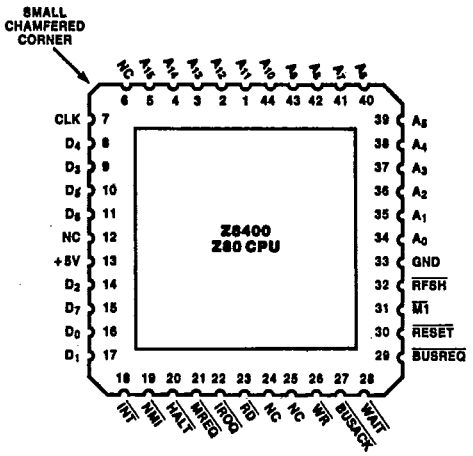
PACKAGE PIN OUTS



DIP and LCC Pin Functions



40-Pin Dual-In-Line Package (DIP), Pin Assignments, Top View



44-Pin Leadless Chip Carrier (LCC), Pin Assignments, Top View

MIL-STD-883 MILITARY PROCESSED PRODUCT

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/ Quality Conformance testing required.

Zilog Military Product Flow

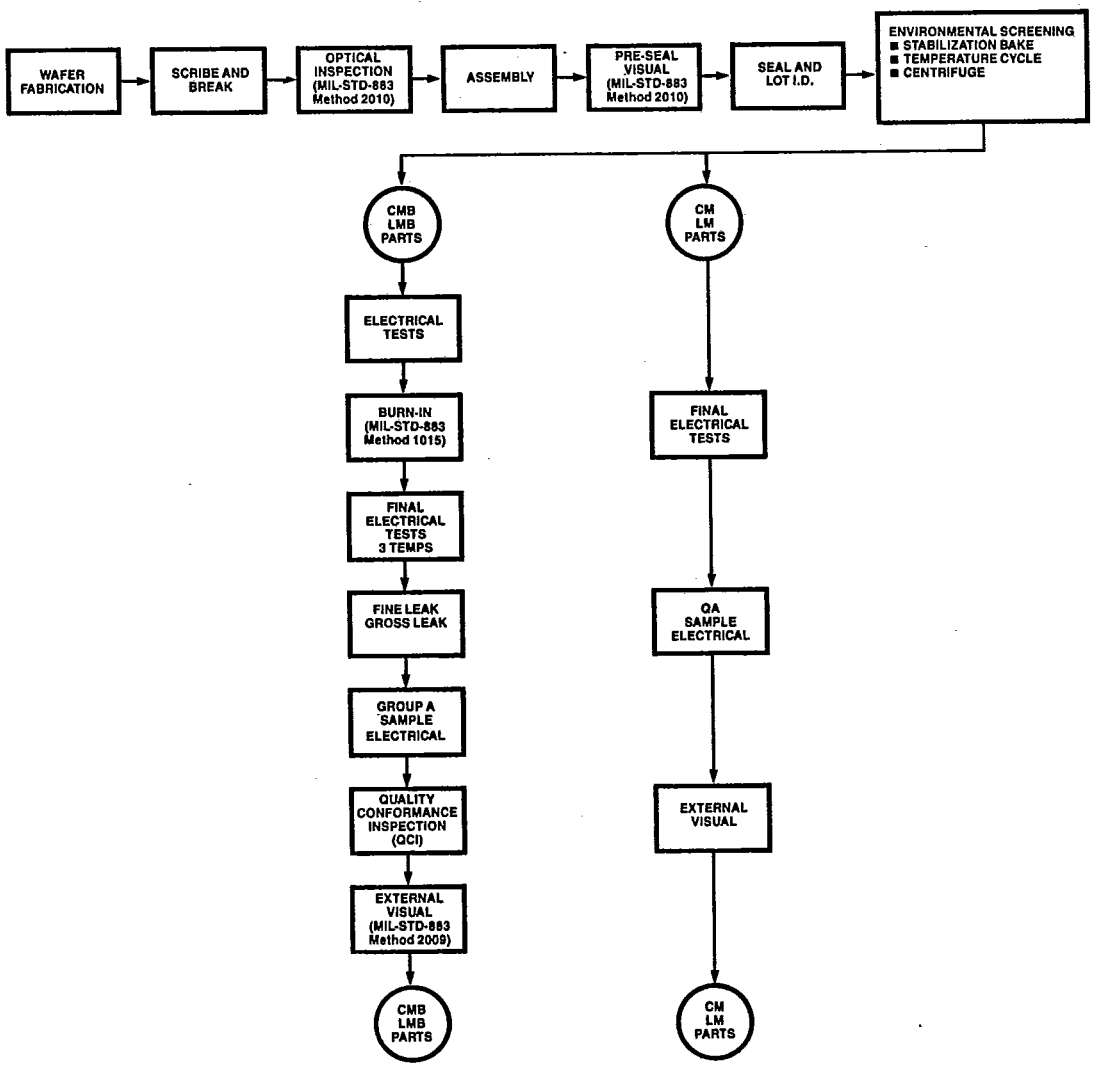


Table I
MIL-STD-883 Class B Screening Requirements
Method 5004

Test	Mil-Std-883 Method	Test Condition	Requirement
Internal Visual	2010	Condition B	100%
Stabilization Bake	1008	Condition C	100%
Temperature Cycle	1010	Condition C	100%
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 1), Y_1 Axis Only	100%
Initial Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
Burn-In	1015	Condition D(Note 2), 160 hours, T_A = +125°C	100%
Interim Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +25°C	100%
PDA Calculation		PDA = 5%	100%
Final Electrical Tests		Zilog Military Electrical Specification Static/DC T_C = +125°C, −55°C Functional, Switching/AC T_C = +25°C	100%
Fine Leak	1014	Condition A_2	100%
Gross Leak	1014	Condition C	100%
Quality Conformance Inspection (QCI)			
Group A Each Inspection Lot	5005	(See Table II)	Sample
Group B Every Week	5005	(See Table III)	Sample
Group C Periodically (Note 3)	5005	(See Table IV)	Sample
Group D Periodically (Note 3)	5005	(See Table V)	Sample
External Visual	2009		100%
QA—Ship			100%

NOTES:
1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).

Table II Group A
Sample Electrical Tests
MIL-STD-883 Method 5005

Subgroup	Tests	Temperature (T_C)	LTPD Max Accept = 2
Subgroup 1	Static/DC	+25°C	2
Subgroup 2	Static/DC	+125°C	3
Subgroup 3	Static/DC	−55°C	5
Subgroup 7	Functional	+25°C	2
Subgroup 8	Functional	−55°C and +125°C	5
Subgroup 9	Switching/AC	+25°C	2
Subgroup 10	Switching/AC	+125°C	3
Subgroup 11	Switching/AC	−55°C	5

NOTES:
- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

Table III Group B

Sample Test Performed Every Week to Test Construction and Insure Integrity of Assembly Process. MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1 Physical Dimensions	2016		2/0
Subgroup 2 Resistance to Solvents	2015		4/0
Subgroup 3 Solderability	2003	Solder Temperature +245°C ± 5°C	15(Note 1)
Subgroup 4 Internal Visual and Mechanical	2014		1/0
Subgroup 5 Bond Strength	2011	C	15(Note 2)
Subgroup 6(Note 3) Internal Water Vapor Content	1018	1000 ppm. maximum at +100°C	3/0 or 5/1
Subgroup 7(Note 4) Seal 7a) Fine Leak 7b) Gross Leak	1014	 7a) A_2 7b) C	5
Subgroup 8(Note 5) Electrostatic Discharge Sensitivity	3015	Zilog Military Electrical Specification Static/DC T_C = +25°C A = 20-2000V B = >2000V Zilog Military Electrical Specification Static/DC T_C = +25°C	15/0

NOTES:
1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

Table IV Group C

Sample Test Performed Periodically to Verify Integrity of the Die.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Steady State Operating Life	1005	Condition D(Note 1), 1000 hours at +125°C	5
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 2			
Temperature Cycle	1010	Condition C	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	
Seal	1014		15
2a) Fine Leak		2a) Condition A_2	
2b) Gross Leak		2b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	

NOTE:
1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.

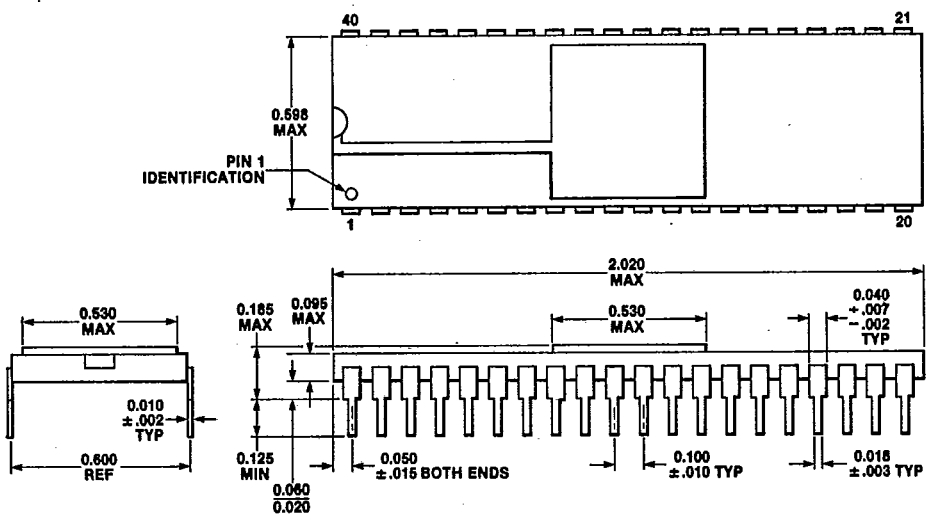
Table V Group D

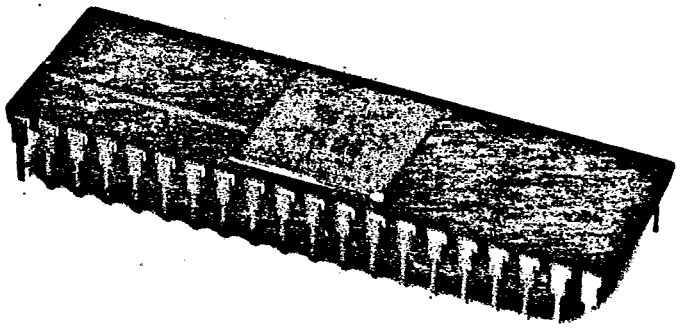
Sample Test Performed Periodically to Insure Integrity of the Package.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Condition B_2 or D(Note 1)	15
Subgroup 3			
Thermal Shock	1011	Condition B minimum, 15 cycles minimum	
Temperature Cycling	1010	Condition C, 100 cycles minimum	15
Moisture Resistance	1004		
Seal	1014		
3a) Fine Leak		3a) Condition A_2	
3b) Gross Leak		3b) Condition C	
Visual Examination	1004 or 1010		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 4			
Mechanical Shock	2002	Condition B minimum	
Vibration Variable Frequency	2007	Condition A minimum	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	15
Seal	1014		
4a) Fine Leak		4a) Condition A_2	
4b) Gross Leak		4b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	
Subgroup 5			
Salt Atmosphere	1009	Condition A minimum	
Seal	1014		15
5a) Fine Leak		5a) Condition A_2	
5b) Gross Leak		5b) Condition C	
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm. maximum water content at +100°C	3/0 or 5/1
Subgroup 7(Note 3)			
Adhesion of Lead Finish	2025		15(Note 4)
Subgroup 8(Note 5)			
Lid Torque	2024		5/0

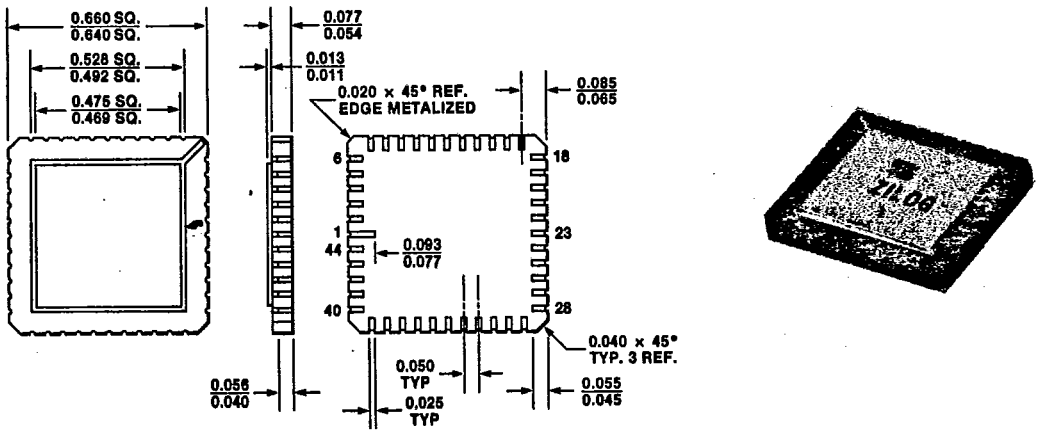
NOTES:
1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

PACKAGE INFORMATION



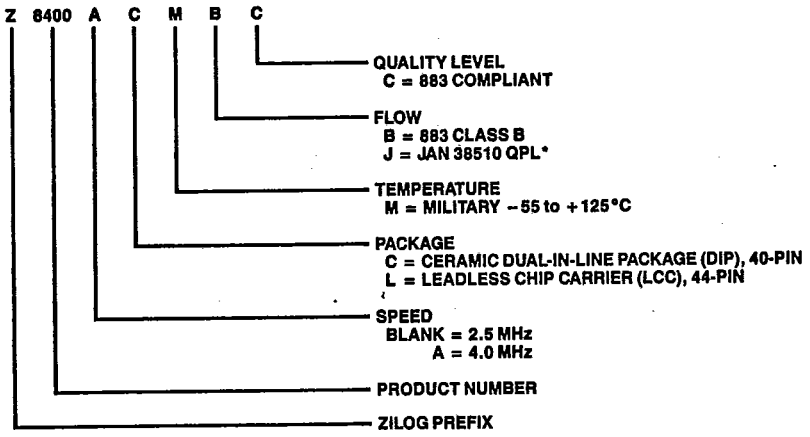


40-Pin Ceramic Dual In-line Package (DIP)



44-Pin Ceramic Leadless Chip Carrier (LCC)

ZILOG ORDERING INFORMATION



*See MIL-M-38510 Slash Sheet 480 for flow and electrical specifications for Z8400CMJ and Z8400ACMJ only.

AVAILABLE MILITARY PRODUCTS

Z80 CPU, 2.5 MHz		Z80A CPU, 4.0 MHz	
40-pin DIP	**44-pin LCC**	**40-pin DIP**	**44-pin LCC**
Z8400 CM	Z8400 LM	Z8400A CM	Z8400A LM
Z8400 CMBC	Z8400 LMBC	Z8400A CMBC	Z8400A LMBC
Z8400 CMJ		Z8400A CMJ	