Z84C30 CMOS Z80®C CTC Counter/Timer Circuit

Zilog NEW 1985

Advance Information AC and DC Characteristics

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ABSOLUTE MAXIMUM RATINGS

Voltages on V_{CC} with respect to V_{SS} . . . . . −0.3V to +7.0V
Voltages on all inputs with respect to V_{SS} . . . . . −0.3V to V_{CC} +0.3V
Storage Temperature . . . . . −65°C to +150°C

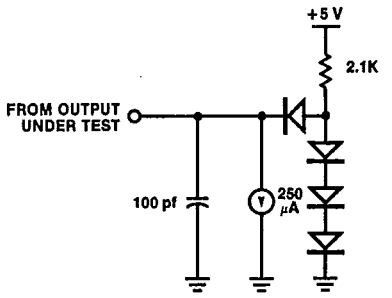
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above these indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin. Available operating temperature range is:

- S = 0°C to +70°C, +4.50V ≤ V_{CC} ≤ +5.50V
- E = −40°C to +85°C, +4.50V ≤ V_{CC} ≤ 5.50V

The Ordering Information section lists package temperature ranges and product numbers. Refer to the Literature List for additional documentation. Package drawings are in the Package Information section.

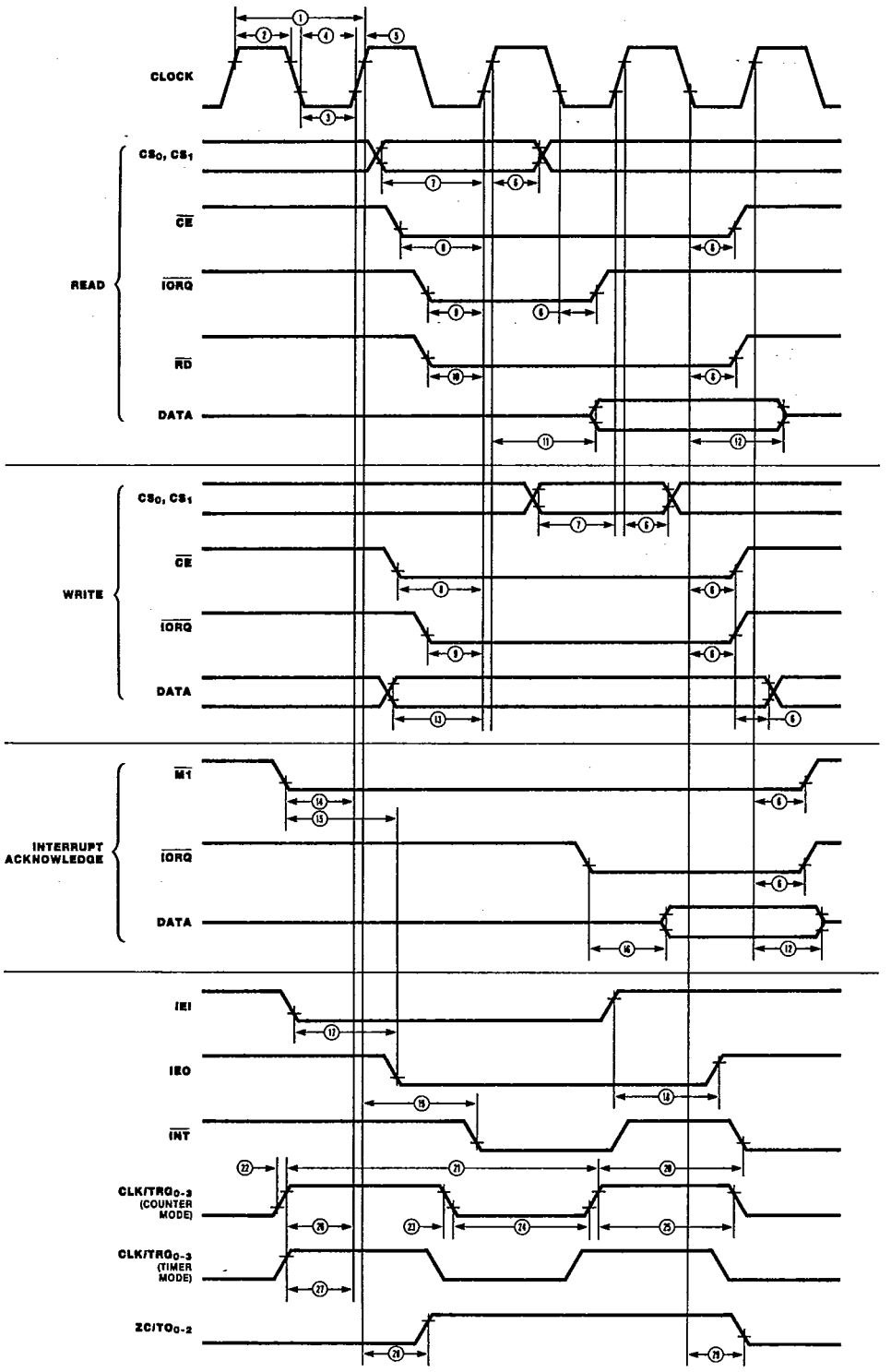


DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Typ	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3	+0.45		V	
V_{IHC}	Clock Input High Voltage	V_{CC} −0.6	V_{CC} +0.3		V	
V_{IL}	Input Low Voltage	−0.3	+0.8		V	
V_{IH}	Input High Voltage	+2.2	V_{CC}		V	
V_{OL}	Output Low Voltage		+0.4		V	I_{OL} = 2.0 mA
V_{OH_1}	Output High Voltage	+2.4			V	I_{OH} = −1.6 mA
V_{OH_2}	Output High Voltage	V_{CC} −0.8			V	I_{OH} = −250 µA
I_{LI}	Input Leakage Current		±10		µA	V_{IN} = 0.4 to V_{CC}
I_{LO}	3-State Output Leakage Current in Float		±10		µA	V_{OUT} = 0.4 to V_{CC}
ICC_1	Power Supply Current		7	3	mA	V_{CC} = 5V CLK = 4MHz V_{IH} = V_{CC} − 0.2V V_{IL} = 0.2V
ICC_2	Standby Supply Current		10	0.5	µA	V_{CC} = 5V CLK = (0) V_{IH} = V_{CC} − 0.2V V_{IL} = 0.2V
I_{OHD}	Darlington Drive Current	−1.5	−5.0		mA	V_{OH} = 1.5V R_{EXT} = 1.1K Ω

Over specified temperature and voltage range.

AC CHARACTERISTICS



AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	Z84C30 Min(ns)	Z84C30 Max(ns)	Z84C30-4 Min(ns)	Z84C30-4 Max(ns)	Notes*
1	TcC	Clock Cycle Time	400	DC [1]	250	DC [1]	
2	TwCh	Clock Pulse Width (High)	170	DC	105	DC	
3	TwCl	Clock Pulse Width (Low)	170	DC	105	DC	
4	TfC	Clock Fall Time		30		30	
5	TrC	Clock Rise Time		30		30	
6	Th	All Hold Times	0		0		
7	TsCS(C)	CS to Clock ↑ Setup Time	250		160		
8	TsCE(C)	$\overline{CE}$ to Clock ↑ Setup Time	200		150		
9	TsIO(C)	$\overline{IORQ}$ ↓ to Clock ↑ Setup Time	250		115		
10	TsRD(C)	$\overline{RD}$ ↓ to Clock ↑ Setup Time	240		115		
11	TdC(DO)	Clock ↑ to Data Out Delay		240		200	[2]
12	TdC(DOz)	Clock ↓ to Data Out Float Delay		230		110	
13	TsDI(C)	Data In to Clock ↑ Setup Time	60		50		
14	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	210		90		
15	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (Interrupt immediately preceding $\overline{M1}$)		300		190	[3]
16	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTA Cycle)		340		160	[2], [6]
17	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		190		130	[3]
18	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED Decode)		220		160	[3]
19	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		(TcC + 200)		(TcC + 140)	[4]
20	TdCLK(INT)	CLK/TRG ↑ to $\overline{INT}$ ↓					
		tsCTR(C) satisfied		(19) + (26)		(19) + (26)	[5]
		tsCTR(C) not satisfied		(1) + (19) + (26)		(1) + (19) + (26)	[5]
21	TcCTR	CLK/TRG Cycle Time	(2TcC)		(2TcC)		[5]
22	TrCTR	CLK/TRG Rise Time		50		50	
23	TfCTR	CLK/TRG Fall Time		50		50	
24	TwCTRl	CLK/TRG Width (Low)	200		200		
25	TwCTRh	CLK/TRG Width (High)	200		200		
26	TsCTR(Cs)	CLK/TRG ↑ to Clock ↑ Setup Time for Immediate Count	300		210		[5]
27	TsCTR(Ct)	CLK/TRG ↑ to Clock ↑ Setup Time for enabling of Prescaler on following clock ↑	300		210		[4]
28	TdC(ZC/TOr)	Clock ↑ to ZC/TO ↑ Delay		260		190	
29	TdC(ZC/TOf)	Clock ↓ to ZC/TO ↓ Delay		190		190	

*$\overline{RESET}$ must be active for a minimum of 3 clock cycles.

NOTES:
[1] TcC = TwCh + TwCl + TrC + TfC.
[2] Increase delay by 10 ns for each 50 pf increase in loading, 200 pf maximum for data lines, and 100 pf for control lines.
[3] Increase delay by 2 ns for each 10 pf increase in loading, 100 pf maximum.
[4] Timer mode.
[5] Counter mode.
[6] 2.5 TcC > (n − 2) TdIEI(IEOf) + TdM1(IEO) + TsIEI(IO) + TTL buffer delay, if any.