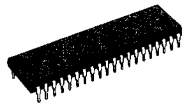
SGS-THOMSON MICROELECTRONICS

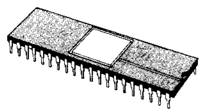
Z8531

ASYNCHRONOUS SERIAL COMMUNICATIONS CONTROLLER

- TWO INDEPENDENT, 0 TO 1M BIT/SECOND, FULL-DUPLEX CHANNELS, EACH WITH A SEPARATE CRYSTAL OSCILLATOR AND BAUD RATE GENERATOR
- PROGRAMMABLE FOR NRZ, NRZI, OR FM DATA ENCODING
- LOCAL LOOPBACK AND AUTO ECHO MODES
- ASYNCHRONOUS COMMUNICATIONS WITH FIVE TO EIGHT BITS PER CHARACTER AND ONE, ONE AND ONE-HALF, OR TWO STOP BITS PER CHARACTER ; PROGRAMMABLE CLOCK FACTOR ; BREAK DETECTION AND GENERATION ; PARITY, OVERRUN, AND FRAMING ERROR DETECTION



PDIP40



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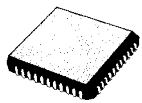


PLCC44

(Ordering Information at the end of the datasheet)

DESCRIPTION

The Z8531 ASCC Asynchronous Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with conventional non-multiplexed buses. The ASCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators and crystal oscillators that dramatically reduce the need for external logic

The ASCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The Z-BUS daisy-chain interrupt hierarchy is also supported–as is standart for Zilog peripheral components.

Figure 1 : Pin Functions.

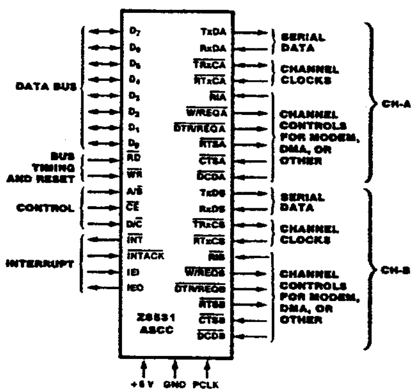


Figure 2a : DIP Pin Connections.

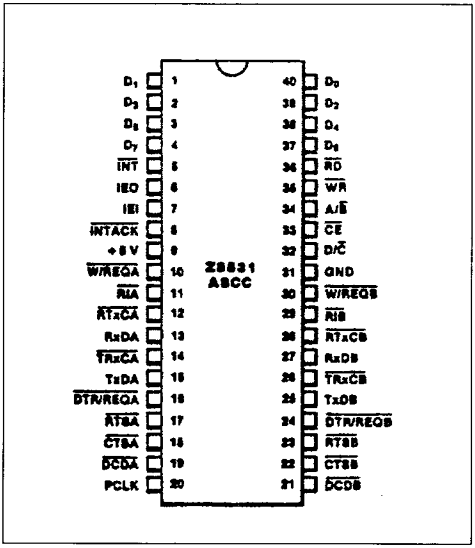
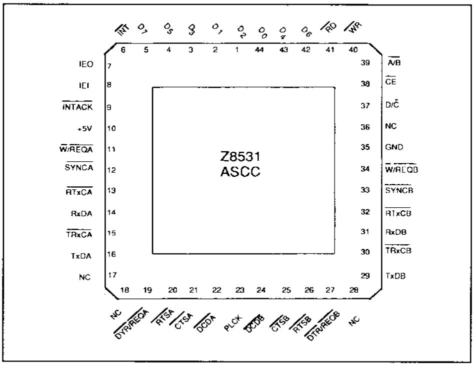


Figure 2b : Chip Carrier Pin Connections.



PIN DESCRIPTION

The following section describes the pin functions of the ASCC. Figures 1 and 2 detail the respective pin functions and pin assignments.

A/B. *Channel A/Channel B Select* (input). This signal selects the channel in which the read or write operation occurs.

CE. *Chip Enable* (input, active Low). This signal selects the ASCC for a read or write operation.

CTSA, CTSB. *Clear To Send* (inputs, active Low). If these pins are programmed as Auto Enables, a Low on the inputs enables the respective transmitters.

If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The ASCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

D/C. *Data/Control Select* (input). This signal defines the type of information transferred to or from the ASCC. A High means data is transferred ; a Low indicates a command.

DCDA, **DCDB**. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if they are programmed for Auto Enables ; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accomodate slow rise-time signals. The ASCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

D_0-D_7. *Data Bus* (bidirectional, 3-state). These lines carry data and commands to and from the ASCC.

DTR/REQA, **DTR/REQB**. *Data Terminal Ready/Request* (outputs, active Low). These outputs follow the state programmed into the DTR bit.They can also be used as general-purpose outputs or as Request lines for a DMA controller.

IEI. *Interrupt Enable In* (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an ASCC interrupt or the ASCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

INT. *Interrupt Request* (output, open-drain, active Low). This signal is activated when the ASCC requests an interrupt.

INTACK. *Interrupt Acknowledge* (input, active Low). This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the ASCC interrupt daisy chain settles. When RD becomes active, the ASCC places an interrupt vector on the data bus (if IEI is High).

INTACK is latched by the rising edge of PCLK.

PIN DESCRIPTION (continued)

PCLK. *Clock* (input). This is the master ASCC clock used to synchronize internal signals ; PCLK is a TTL level signal.

RD. *Read* (input, active Low). This signal indicates a read operation and when the ASCC is selected, enables the ASCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the ASCC is the highest priority device requesting an interrupt.

RxDA, RxDB. *Receive Data* (inputs, active High). These input signals receive serial data at standard TTL levels.

RIA, RIB. *Ring Indicator* (inputs, active Low).These pins can act either as inputs, or part of the crystal oscillator circuit. In normal mode (crystal oscillator option not selected), these pins are inputs similar to CTS and DCD. In this mode, transitions on these lines affect the state of the Ring Indicator status bits in Read Register 0 (Figure 8) but have no other function.

RTxCA, RTxCB. *Receive/Transmit Clocks* (inputs, active Low). These pins can be programmed in several different modes of operation. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective RI pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in Asynchronous modes.

RTSA, RTSB. *Request To Send* (outputs, active Low). When the Request To Send (RTS) bit in Write Register 5 (Figure 9) is set, the RTS signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. With Auto Enable off, the RTS pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

TxDA, TxDB. *Transmit Data* (outputs, active High). These output signals transmit serial data at standard TTL levels.

TRxCA, TRxCB. *Transmit/Receive Clocks* (inputs or outputs, active Low). These pins can be programmed in several different modes of operation. TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

WR. *Write* (input, active Low). When the ASCC is selected, this signal indicates a write operation. The coincidence of RD and WR is interpreted as a reset.

W/REQA, W/REQB. *Wait/Request* (outputs, open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function). These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the ASCC data rate. The reset state is Wait.

FUNCTIONAL DESCRIPTION

The functional capabilities of the ASCC can be described from two different points of view : as a data communications device, it transmits and receives data in a wide variety of data communications protocols ; as a microprocessor peripheral, the ASCC offers valuable features such as vectored interrupts, polling, and simple handshake capability.

Data Communications Capabilities. The ASCC provides two independent full-duplex channels programmable for use in any common Asynchronous data communication protocol. Figure 3 and the following description briefly detail this protocol.

Asynchronous Modes. Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half, or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 1). If the Low does not persist (as in the case of a tran-sient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit : a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The ASCC does not require symmetric transmit and receive clock signals–a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1/16, 1/32, or

FUNCTIONAL DESCRIPTION (continued)

1/64 of the clock rate supplied to the receive and transmit clock inputs.

Baud Rate Generator. Each channel in the ASCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in the High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching 0, the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the Digital Phase-Locked Loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{TRxC}$ pin, the output of the baud rate generator may be echoed out via the $\overline{TRxC}$ pin.

The following formula relates the time constant to the baud rate (the baud rate is in bits/second and the BR clock period is in seconds) :

$$\text{time constant} = \frac{\text{PCLK}}{2\ (\text{clock factor})\ (\text{baud})} - 2$$

Digital Phase-Locked Loop. The ASCC contains a Digital Phase-Locked-Loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the ASCC receive clock, the transmit clock, or both.

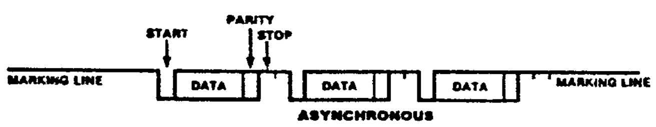
For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the $\overline{RTxC}$ input of the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the ASCC via the $\overline{TRxC}$ pin (if this pin is not being used as an input).

Data Encoding. The ASCC may be programmed to encode and decode the serial data in four different ways (Figure 4). In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encodint, a 1 is represented by no change in level and a 0 is represented by a change in level. In FM1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FMO (bi-phase space), a transi-tion occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the ASCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

Figure 3 : ASCC Protocol.



FUNCTIONAL DESCRIPTION (continued)

Auto Echo and Local Loopback. The ASCC is capable of automatically echoing everything it receives. In Auto Echo mode, RxD is connected to TxD internally. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{\text{CTS}}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and $\overline{\text{WAIT/REQUEST}}$ on transmit.

The ASCC is also capable of local loopback. In this mode TxD is connected to RxD internally, just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works with NRZ, NRZI or FM coding of the data stream.

I/O Interface Capabilities. ASCC offers the choice of Polling, Interrupt (vectored or non vectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

Polling. All interrupts are disabled. Three status registers in the ASCC are automatically updated whenever any function is performed. The idea behing polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read ; depending on its contents, the CPU either writes data, reads data, or continues.

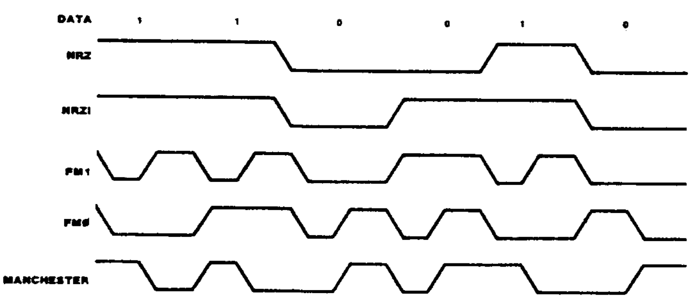
Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

Interrupts. When an ASCC responds to an Interrupt Acknowledge signal ($\overline{\text{INTACK}}$) from the CPU an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 8 and 9).

To speed interrupt response time, the ASCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included ; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the ASCC (Transmit, Receive, and External/ Status interrupts in both channels) has three bits associated with the interrupt source : Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write only.

Figure 4 : Data Encoding Methods.



FUNCTIONAL DESCRIPTION (continued)

The other two bits are related to the interrupt priority chain (Figure 5). As a microprocessor peripheral, the ASCC may request an interrupt only when no higher priority device is requesting one, e.g., when IEI is High. If the device in question requests an interrupt, it pulls down INT. The CPU then res-ponds with INTACK, and the interrupting device places the vector on the data bus.

In the ASCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the INT output is pulled Low, requesting an interrupt. In the ASCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the ASCC and external to the ASCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the ASCC being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts :

Transmit, Receive, and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receiver, Transmit, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the receiver can interrupt the CPU in one ot three ways :

- Interrupt on First Receive Character or Special Receive Condition.
- Interrupt on All Receive Characters or Special Receive Condition.
- Interrupt on Special Receive Condition Only.

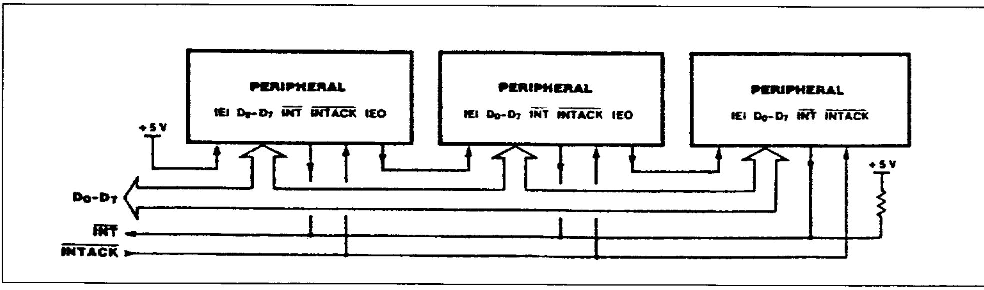
Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is a receiver overrun, and, optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary receive character available interrupt only in the status placed in the vector during the Interrupt Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive Conditions any time after the first receive character interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the CTS, DCD and RI pins ; however, an External/Status interrupt is also caused by a Transmit Underrun condition, or a zero count in the baud rate generator, or by the detection of a Break.

CPU/ DMA Block Transfer. The ASCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the WAIT/ REQUEST output in conjunction with the Wait/Request bits in WR1. The WAIT/ REQUEST output can be defined under software control as a WAIT line in the CPU Block Transfer mode or as a REQUEST line in the DMA Block Transfer mode.

To a DMA controller, the ASCC REQUEST output indicates that the ASCC is ready to tranfer data to or from memory. To the CPU, the WAIT line indicates that the ASCC is not ready to transfer data thereby requesting that the CPU extend the I/O cycle. The DTR/ REQUEST line allows full-duplex operation under DMA control.

Figure 5 : Interrupt Schedule.



ARCHITECTURE

The ASCC internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to a nonmultiplexed bus. Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface to modems of other external devices (Figure 6).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write only Master Interrupt Control register and three read registers : one containing the vector with status information (Channel B only), one containing the vector without status (Channel A only), and one containing the Interrupt Pending bits (Channel A only).

The registers for each channel are designated as follows :

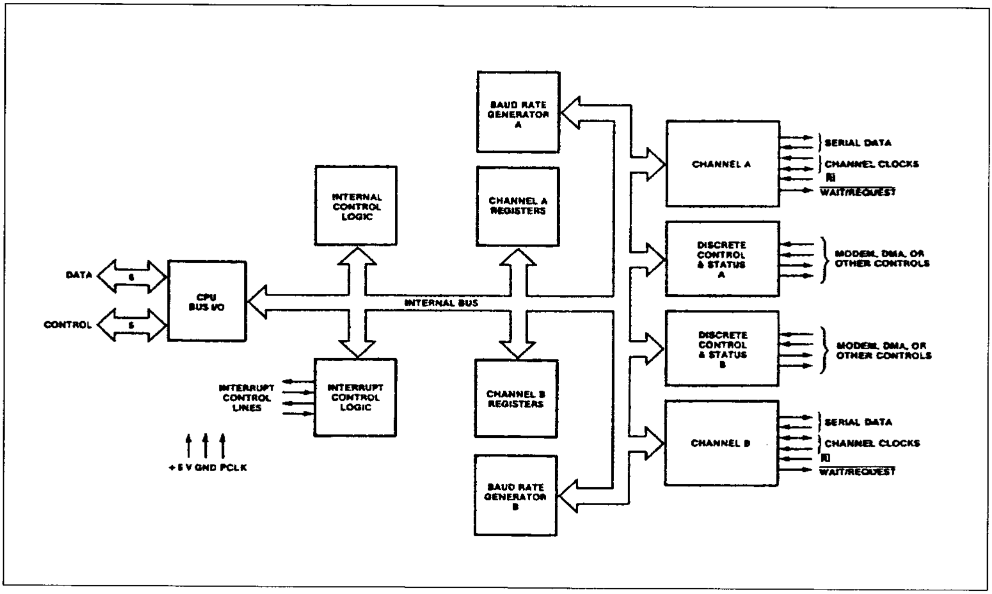
WR0-WR15 - Write Registers 0-5, 8-15.

RR0-RR3, RR10, RR12, RR13, RR15 - Read Registers 0 through 3, 10, 12, 13, 15.

Table 1 lists the functions assigned to each read or write register. The ASCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

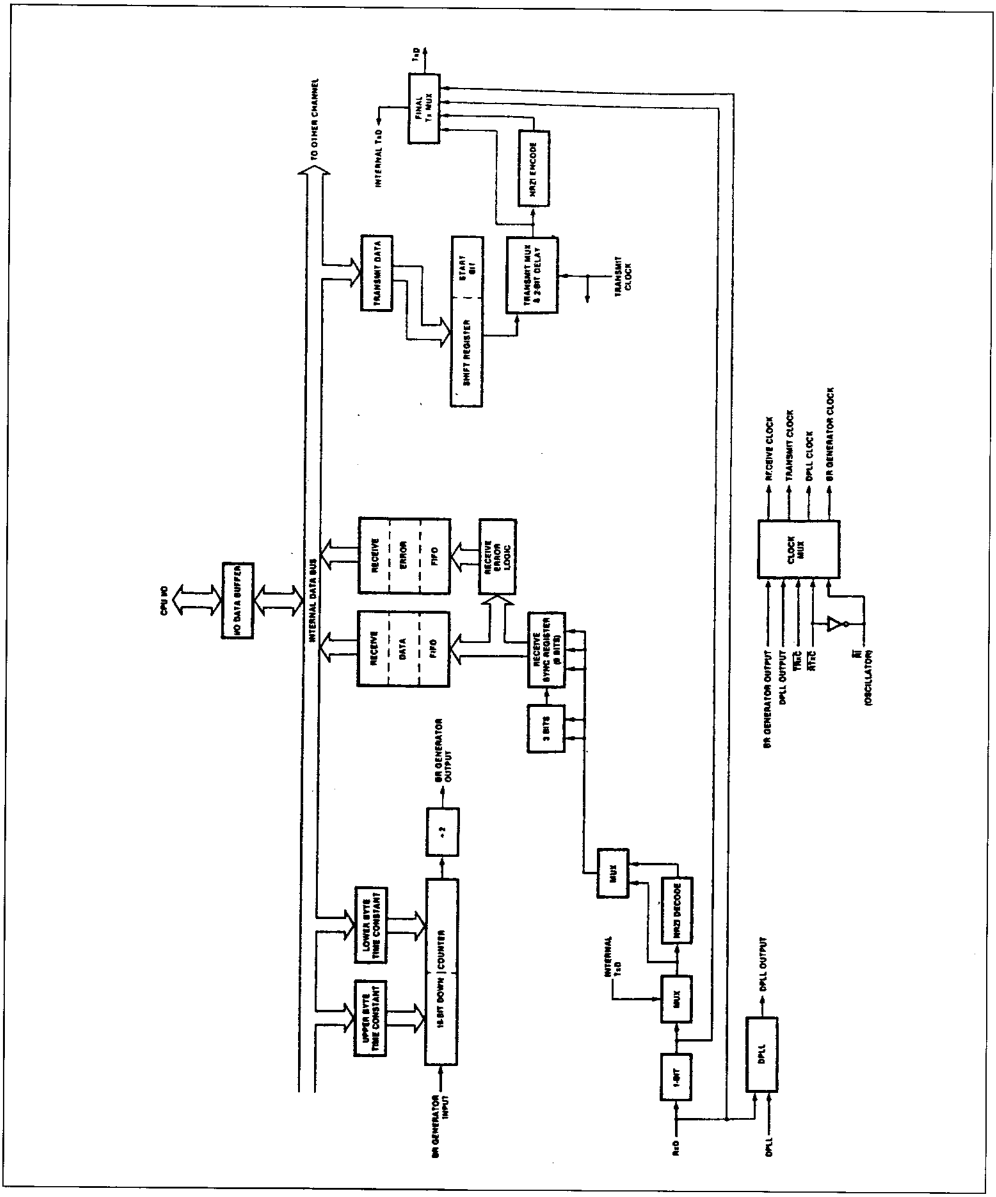
Data path. The transmit and receive data path illustrated in Figure 7 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high speed data. Incoming data is routed through one of several paths depending on the selected mode (the character length also determines the data path).

Figure 6 : Block Diagram of ASCC Architecture.



ARCHITECTURE (continued)

Figure 7 : Data Path.



ARCHITECTURE (continued)

The transmitter has an 8-bit Transmit Data buffer register loaded from the internal data bus and an 11-bit Transmit Shift register that can be loaded from the Transmit Data register.

Table 1. Read and Write Register Functions.

Read Register Functions	
RR0	Transmit/Receive buffer status and External status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Chanel B only) Unmodified interrupt vector (Channel A only)
RR3	Interrupt Pending bits (Channel A only)
RR8	Receive buffer
RR10	Miscellaneous status
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR15	External/Status interrupt information

Write Register Functions	
WR0	CRC initialize, initialization commands for the various modes, Registers Pointers
WR1	Transmit/Receive interrupt and data transfer mode definition
WR2	Interrupt vector (accessed through either channel)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR8	Transmit buffer
WR9	Master it interrupt control and reset (accessed through either channel)
WR10	Miscellaneous transmitter/receiver control bits
WR11	Clock mode control
WR12	Lower byte of baud rate generator time constant
WR13	Upper byte of baud rate generator time constant
WR14	Miscellaneous control bits
WR15	External/Status interrupt control

PROGRAMMING

The ASCC contains 11 write registers in each channel that are programmed by the system separately to configure the functional personality of the channels.

In the ASCC, register addressing is direct for the data registers only, which are selected by a High on the D/$\overline{C}$ pin. In all other cases (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected register, and if the second operation is read, the selected read register is accessed. All of the registers in the ASCC, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

The system program first issues a series of commands to initialize the basic mode of operation. For example, the character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set, and finally, receiver or transmitter enable.

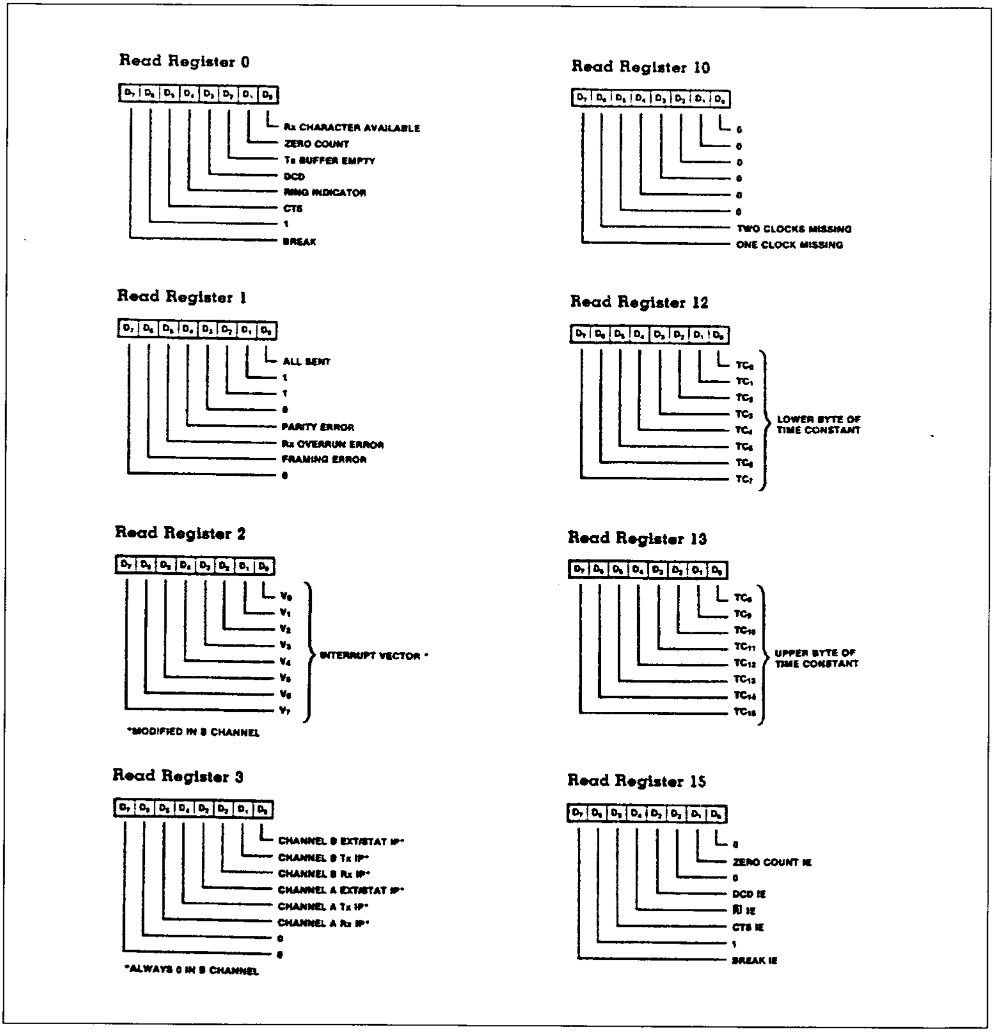
Read Registers. The ASCC contains eight read registers (actually nine, counting the receive buffer (RR8) in each channel). Four of these may be read ot obtain status information (RRO, RR1, RR10, and RR15). Two registers baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). Figure 8 shows the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicated a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

Write Registers. The ASCC contains 11 write registers (12 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 9 shows the format of each write register.

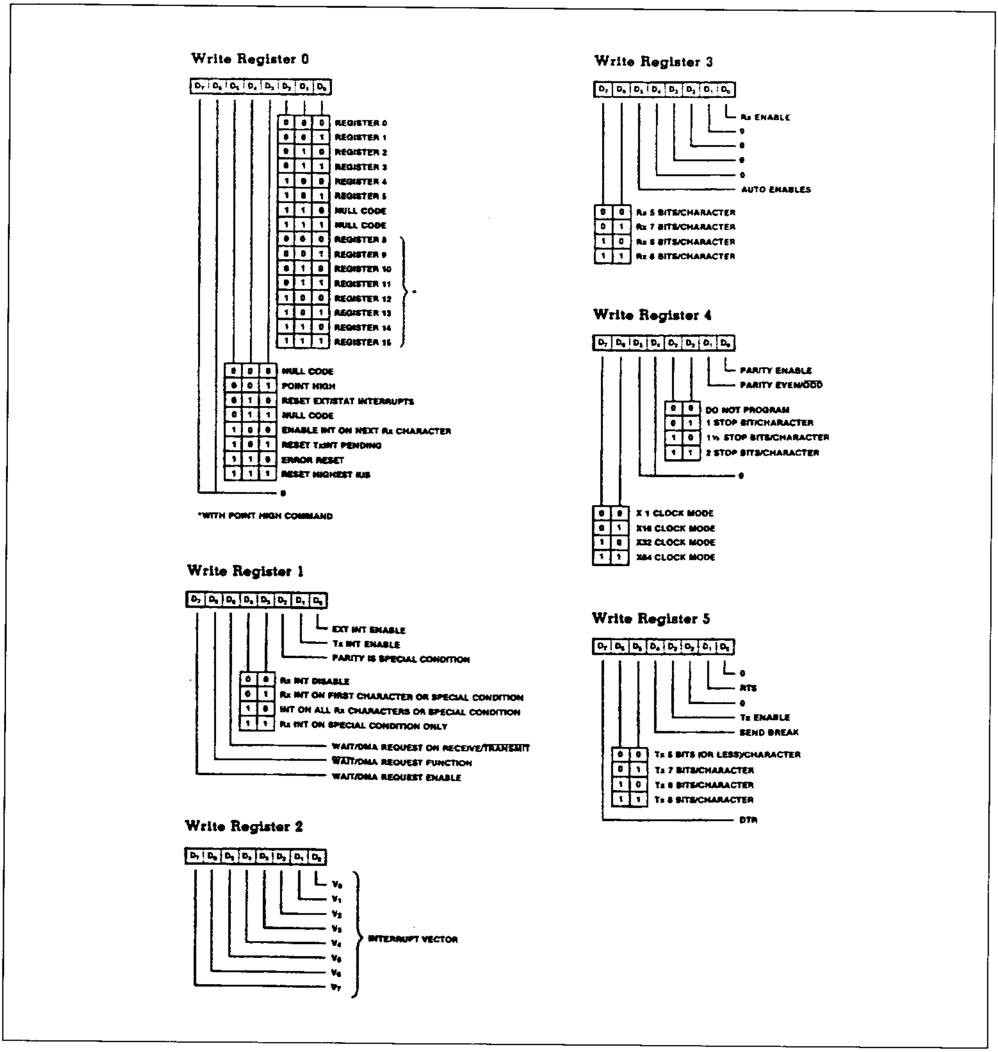
PROGRAMMING (continued)

Figure 8 : Read Register Bit Functions.



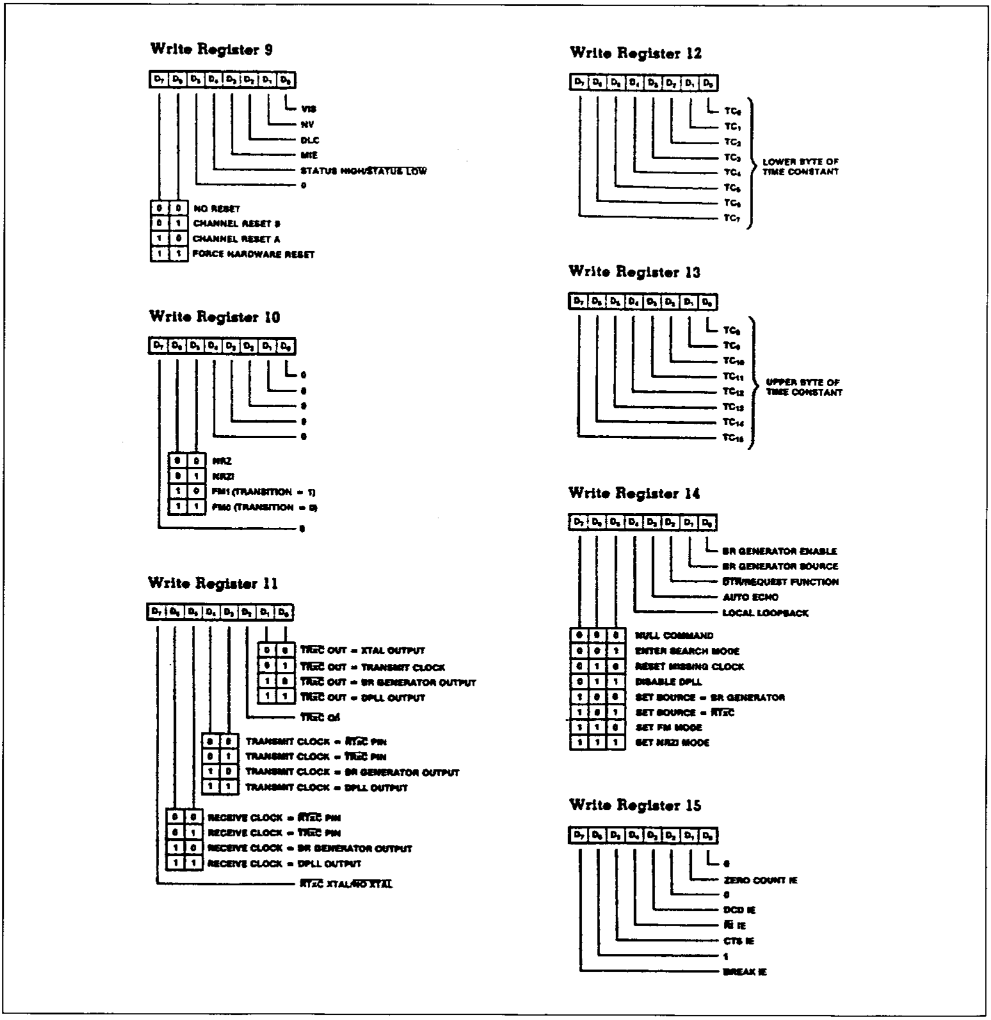
PROGRAMMING (continued)

Figure 9 : Write Register Bit Functions.



PROGRAMMING (continued)

Figure 9 : Write Register Bit Functions (continued).



TIMING

The ASCC generates internal control signals from $\overline{\text{WR}}$ and $\overline{\text{RD}}$ that are related to PCLK. Since PLCK has no phase relationship with $\overline{\text{WR}}$ and $\overline{\text{RD}}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the ASCC. The recovery time required for proper operation is specified from the rising edge of $\overline{\text{WR}}$ or $\overline{\text{RD}}$ in the first transaction involving the ASCC to the falling edge of $\overline{\text{WR}}$ or $\overline{\text{RD}}$ in the second transaction involving the ASCC. This time must be at least 6 PLCK cycles plus 200 ns.

Read Cycle Timing. Figure 10 illustrates read cycle timing. Addresses on A/$\overline{\text{B}}$ and D/$\overline{\text{C}}$ and the status on $\overline{\text{INTACK}}$ must remain stable throughout the cycle. If $\overline{\text{CE}}$ falls after $\overline{\text{RD}}$ falls, or rises before $\overline{\text{RD}}$ rises, the effective $\overline{\text{RD}}$ is shortened.

Write Cycle Timing. Figure 11 illustrates write cycle timing. Addresses on A/$\overline{\text{B}}$ and D/$\overline{\text{C}}$ and the status on $\overline{\text{INTACK}}$ must remain stable throughout the cycle. If $\overline{\text{CE}}$ falls after $\overline{\text{WR}}$ falls or rises before $\overline{\text{WR}}$ rises, the effective $\overline{\text{WR}}$ is shortened.

Interrupt Acknowledge Cycle Timing. Figure 12 illustrates interrupt acknowledge cycle timing. Between the time $\overline{\text{INTACK}}$ goes low and the falling edge of $\overline{\text{RD}}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending the ASCC and IEI is High when $\overline{\text{RD}}$ falls, the acknowledge cycle was intended for the ASCC. In this case, the ASCC may be programmed to respond to $\overline{\text{RD}}$ Low by placing its interrupt vector on D_0-D_7 and sets the appropriate Interrupt-Under-Service latch internally.

Figure 10 : Read Cycle Timing.

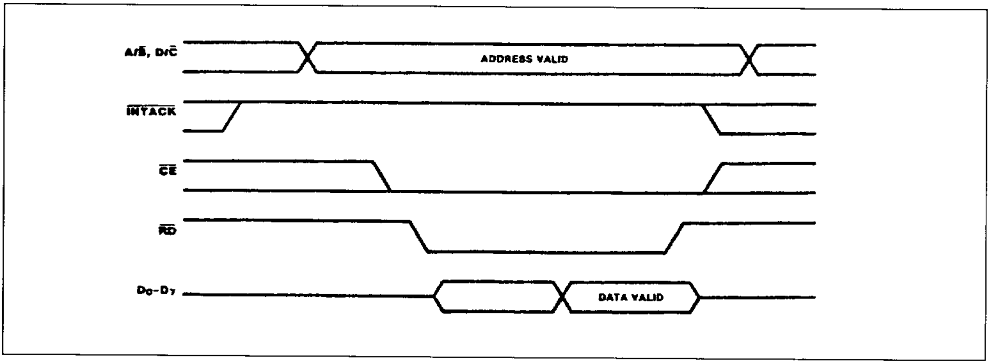
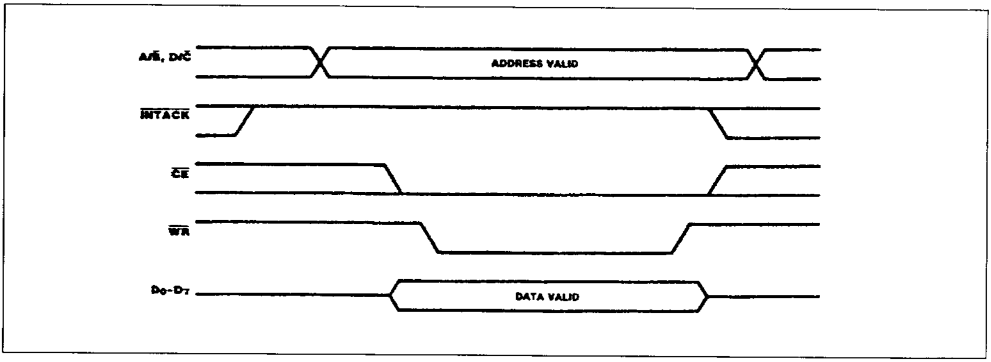
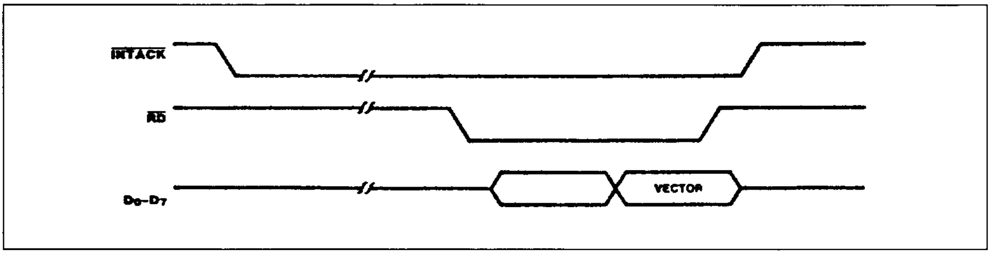


Figure 11 : Write Cycle Timing.



TIMING (continued)

Figure 12 : Interrupt Acknowledge Cycle Timing.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltages on all Pins with Respect to GND	– 0.3 to + 7.0	V
T_A	Operating Ambient Temperature	0 to + 70 – 40 to + 85 – 55 to + 125	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only ; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDART TEST CONDITIONS

The DC characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows :

- $+ 4.75V \leq V_{CC} \leq + 5.25V$
- GND = 0V
- T_A as specified in Order Codes

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section in this book. Refer to the Literature List for additional documentation.

All ac parameters assume a load capacitance of 50 pf max.

Figure 13 : Standart Test Load.

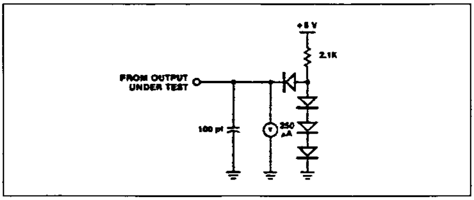
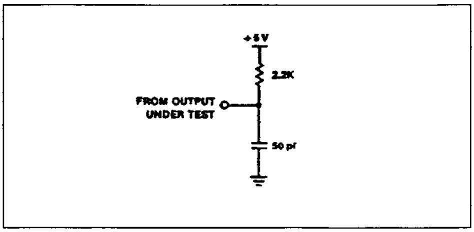


Figure 14 : Open-Drain Test Load.



DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IH}	Input High Voltage	–	2.0	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–	– 0.3	0.8	V
V_{OH}	Output High Voltage	I_{OH} = – 250 µA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL} = + 2 mA	–	0.4	V
I_{IL}	Input Leakage	$0.4 \leq V_{IN} \leq +2.4$ V	–	± 10	µA
I_{OL}	Output Leakage	$0.4 \leq V_{OUT} \leq +2.4$ V	–	± 10	µA
I_{CC}	V_{CC} Supply Current	–	–	250	mA

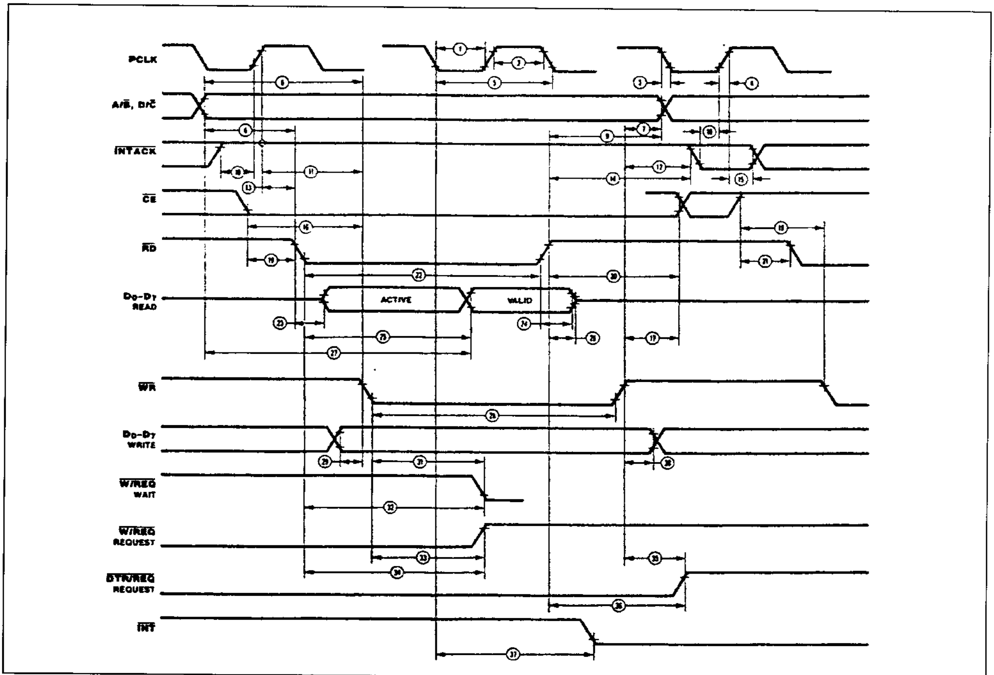
V_{CC} = 5 V ± 5% unless otherwise specified, over specified temperature range.

CAPACITANCE

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	–	–	10	pf
C_{OUT}	Output Capacitance	–	–	15	pf
$C_{I/O}$	Bidirectional Capacitance	–	–	20	pf

f : 1 MHz, over specified temperature range.
Unmeasured pins returned to ground.

READ AND WRITE TIMING

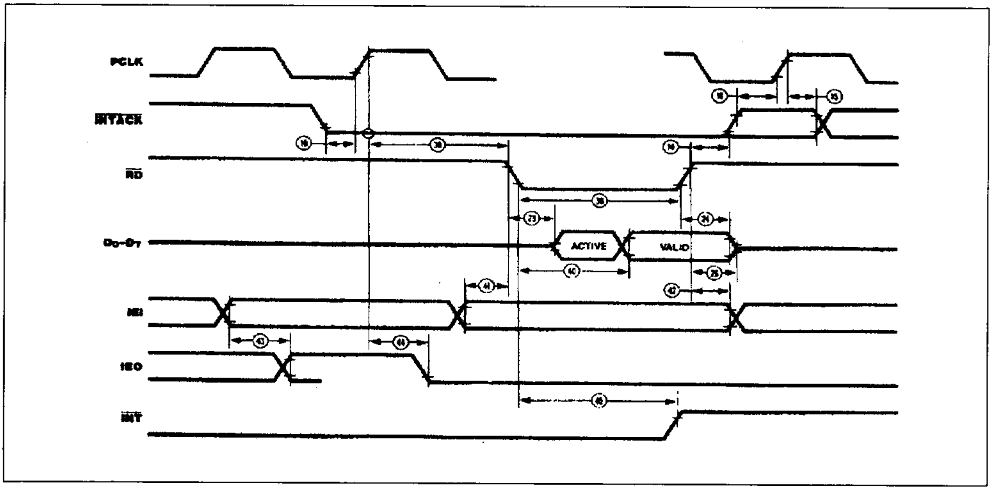


READ AND WRITE TIMING (continued)

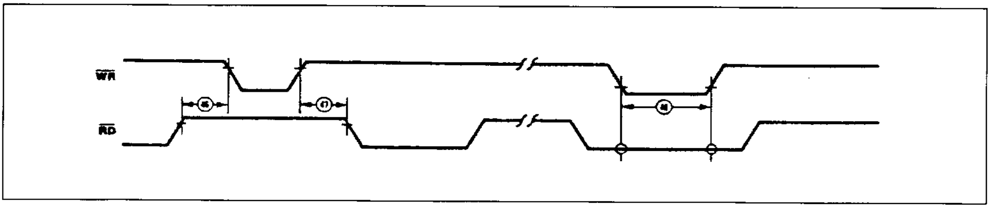
N°	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes *
			Min.	Max.	Min.	Max.	Min.	Max.	†
1	TwPCl	PCLK Low Width	105	2000	70	1000	50	1000	–
2	TwPCh	PCLK High Width	105	2000	70	1000	50	1000	–
3	TfPC	PCLK Fall Time	–	– 20	–	10	–	10	–
4	TrPC	PCLK Rise Time	–	– 20	–	15	–	10	–
5	TcPC	PCLK Cycle Time	250	4000	165	2000	125	2000	–
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	80	–	80	–	70	–	–
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0	–	0	–	0	–	–
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	80	–	80	–	70	–	–
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0	–	0	–	0	–	–
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	10	–	10	–	10	–	–
11	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time	200	–	160	–	145	–	1
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0	–	0	–	0	–	–
13	TsIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time	200	–	160	–	145	–	1
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0	–	0	–	0	–	–
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	100	–	100	–	85	–	–
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0	–	0	–	0	–	–
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0	–	0	–	0	–	–
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	100	–	70	–	60	–	–
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time	0	–	0	–	0	–	1
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time	0	–	0	–	0	–	1
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time	100	–	70	–	60	–	1
22	TwRDl	$\overline{RD}$ Low Width	240	–	200	–	150	–	1
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0	–	0	–	0	–	–
24	TdRDr(DR)	$\overline{RD}$ ↑ To Read Data Not Valid Delay	0	–	0	–	0	–	–
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay	–	250	–	180	–	140	–
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay	–	70	–	45	–	40	2

Notes : 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ± 0.5 V change in the output with a maximum dc load and minimum ac load.
* Timings are preliminary and subject to change.
† Units in nanoseconds (ns).

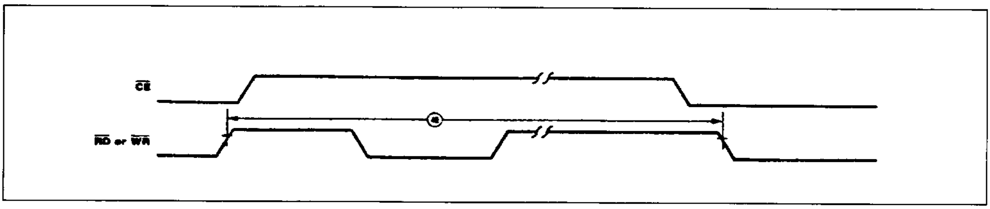
INTERRUPT ACKNOWLEDGE TIMING



RESET TIMING



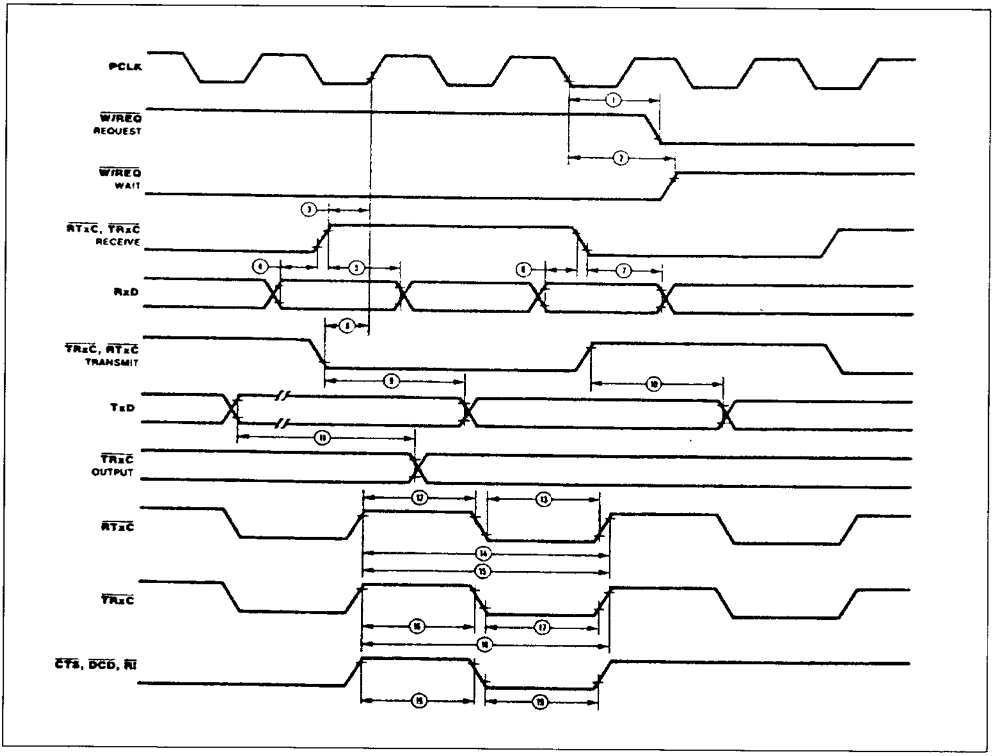
CYCLE TIMING



N°	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes * †
			Min.	Max.	Min.	Max.	Min.	Max.	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay	–	300	–	280	–	220	–
28	TwWRl	$\overline{WR}$ Low Width	240	–	200	–	150	–	–
29	TsDW(WR)	Write Data to $\overline{WR}$ ↓ Setup Time	10	–	10	–	10	–	–
30	ThDW(WR)	Write Data $\overline{WR}$ ↑ Hold time	0	–	0	–	–	–	–
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay	–	240	–	200	–	170	4
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay	–	240	–	200	–	170	4
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay	–	240	–	200	–	170	–
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay	–	240	–	200	–	170	–
35	TdWRr(REQ)	$\overline{WR}$ ↑ to $\overline{DTR/REQ}$ not Valid Delay	–	4TcPC	–	4TcPC	–	4TcPC	–
36	TdRD(REQ)	RD ↑ $\overline{DTR/REQ}$ Not Valid Delay	–	4TcPC	–	4TcPC	–	4TcPC	–
37	TdPC(INT)	PLCK ↓ To $\overline{INT}$ Valid Delay	–	500	–	500	–	500	4
38	TdA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (acknowledge) Delay	250	–	200	–	150	–	5
39	TwRDA	$\overline{RD}$ (acknowledge) Width	250	–	200	–	150	–	–
40	TdRDA(DR)	$\overline{RD}$ ↓ (acknowledge) to Read Data Valid Delay	–	250	–	180	–	140	–
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (acknowledge) Setup Time	120	–	100	–	95	–	–
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (acknowledge) Hold Time	0	–	0	–	0	–	–
43	TdIEI(IEO)	IEI to IEO Delay Time	–	120	–	100	–	95	–
44	TdPC(IEO)	PLCK ↑ IEO Delay	–	250	–	250	–	200	–
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay	–	500	–	500	–	450	4
46	TdRD(WRQ)	$\overline{RD}$ ↑ $\overline{WR}$ ↓ Delay for no Reset	30	–	15	–	15	–	–
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for no Reset	30	–	30	–	20	–	–
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	250	–	200	–	150	–	–
49	Trc	Valid Access Recovery Time	4TcPC	–	4TcPC	–	4TcPC	–	3

Notes : 3. Parameter applies only between transactions involving the ASCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any ASCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC (IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the ASCC, and TdIEI(IEO) for each device separating them in the daisy chain.
* Timing are preliminary and subject to change.
† Units in nanoseconds (ns).

GENERAL TIMING

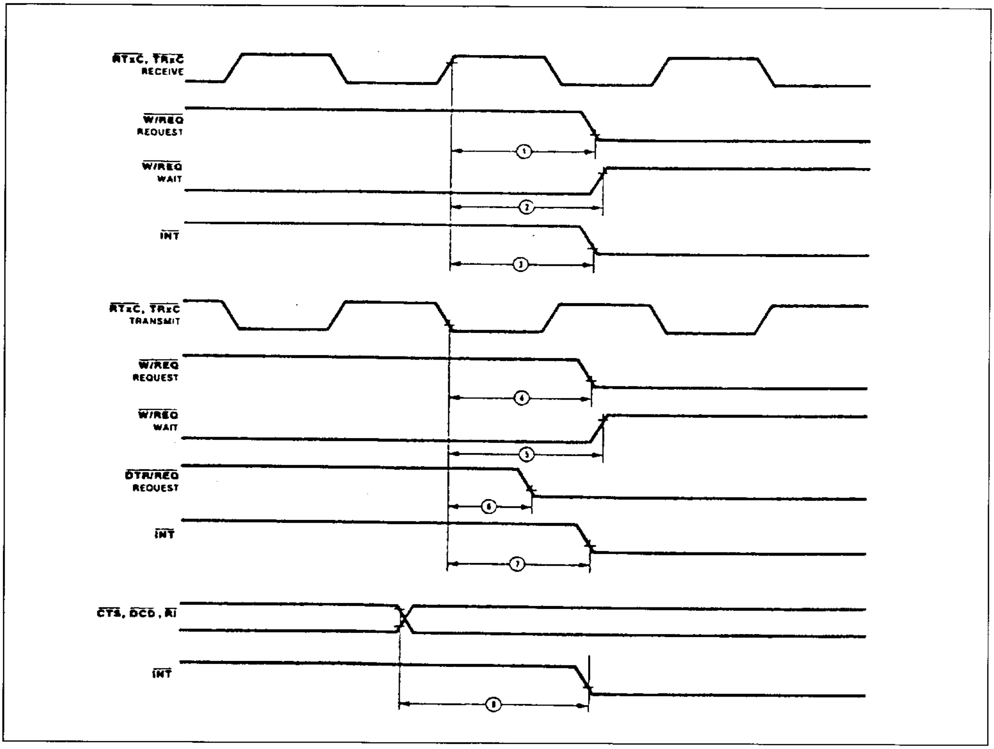


GENERAL TIMING (continued)

N°	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes *
			Min.	Max.	Min.	Max.	Min.	Max.	†
1	TdPC(REQ)	PCLK ↓ to W/REQ Valid Delay	–	250	–	250	–	250	–
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay	–	350	–	350	–	350	–
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time (PCLK + 4 case only)	80	TwPCl	70	TwPCl	60	TwPCl	1.4
4	TsRXD(RXCr)	RxD to RXC ↑ Setup Time (XI mode)	0	–	0	–	0	–	1
5	ThRXD(RXCr)	RxD to RxC ↑ Hold Time (XI mode)	150	–	150	–	150	–	1
6	TsRXD(RXCf)	RxD to RxC ↓ Setup Time (X1 mode)	0	–	0	–	0	–	1.5
7	ThRXD(RXCf)	RxD to RxC ↓ Hold Time (X1 Mode)	150	–	150	–	150	–	1.5
8	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time	0	–	0	–	0	–	2.4
9	TdTXCf(TXD)	TxC ↓ to TxD Delay (X1 Mode)	–	300	–	230	–	200	2
10	TdTXCr(TXD)	TxC ↑ to TxD Delay (X1 mode)	–	300	–	230	–	200	2.5
11	TdTXD(TRX)	TxD to TRxC Delay (send clock echo)	–	200	–	200	–	200	–
12	TwRTXh	RTxC High Width	180	–	180	–	150	–	6
13	TwRTXl	RTxC Low Width	180	–	180	–	150	–	6
14	TcRTX	RTxC Cycle Time	1000	–	640	–	500	–	6
15	TcRTXX	Crystal Oscillator Period	250	1000	165	1000	125	1000	3
16	TwTRXh	TRxC High Width	180	–	180	–	150	–	6
17	TwTRXl	TRxC Low Width	180	–	180	–	150	–	6
18	TcTRX	TRxC Cycle Time	1000	–	640	–	500	–	6.7
19	TwEXT	DCD or CTS or RI Pulse Width	200	–	200	–	200	–	–

Notes : 1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and R1 have 30 pF capacitors ot ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
7. The maximum receive or transmit data is 1/4 PLCK.
* Timings are preliminary and subject to change.
† Units in nanoseconds (ns).

SYSTEM TIMING



N°	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes * †
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TdRXC(REQ)	RxC ↑ to W/REQ Valid Delay	8	12	8	12	8	12	2
2	TdRXC(W)	RxC ↑ to Wait Inactive Delay	8	14	8	14	8	14	1, 2
3	TdRXC(INT)	RxC ↑ to INT Valid Delay	10	16	10	16	10	16	1, 2
4	TdTXC(REQ)	TxC ↓ to W/REQ Valid Delay	5	8	5	8	5	8	3
5	TdTXC(W)	TxC ↓ to Wait Inactive Delay	5	11	5	11	5	11	1, 3
6	TdTXC(DRQ)	TxC ↓ to DRT/REQ Valid Delay	4	7	4	7	4	7	1, 3
7	tdTXC(INT)	TxC ↓ to INT Valid Delay	6	10	6	10	6	10	1, 3
8	TdEXT(INT)	DCD or CTS Transition to INT Valid Delay	2	6	2	6	2	6	1

Notes : 1. Open-drain output, measured with open-drain test load.
2. RxC is RTxC or TRxC, whichever is supplying the receive clock.
3. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
* Timings are preliminary and subject to change.
† Units equal to TcPC.

ORDERING INFORMATION

Sales Type	Frequency	Temp. Range	Package
Z8531B1V	4MHz	0 to + 70°C	PDIP-40
Z8531AB1V	6MHz	0 to + 70°C	PDIP-40
Z8531BB1V	8MHz	0 to + 70°C	PDIP-40
Z8531B6V	4MHz	– 40 to + 85°C	PDIP-40
Z8531AB6V	6MHz	– 40 to + 85°C	PDIP-40
Z8531BB6V	8MHz	– 40 to + 85°C	PDIP-40
Z8531C1V	4MHz	0 to + 70°C	PLCC44
Z8531AC1V	6MHz	0 to + 70°C	PLCC44
Z8531BC1V	8MHz	0 to + 70°C	PLCC44
Z8531C6V	4MHz	– 40 to + 85°C	PLCC44
Z8531AC6V	6MHz	– 40 to + 85°C	PLCC44
Z8531BC6V	8MHz	– 40 to + 85°C	PLCC44
Z8531D1N	4MHz	0 to + 70°C	CDIP-40
Z8531AD1N	6MHz	0 to + 70°C	CDIP-40
Z8531BD1N	8MHz	0 to + 70°C	CDIP-40
Z8531D6N	4MHz	– 40 to + 85°C	CDIP-40
Z8531AD6N	6MHz	– 40 to + 85°C	CDIP-40
Z8531BD6N	8MHz	– 40 to + 85°C	CDIP-40
Z8531D2N	4MHz	– 55 to + 125°C	CDIP-40
Z8531AD2N	6MHz	– 55 to + 125°C	CDIP-40

Note : PDIP = Plastic DIP ; CDIP = Ceramic Multilayer DIP ; PLCC = Plastic Leaded Chip Carrier.