Universal Peripheral Controller

Z8590 UPC

Features

- Complete slave microcomputer, for distributed processing use.
- Unmatched power of Z8 architecture and instruction set.
- Three programmable I/O ports, two with optional 2-Wire Handshake.
- Six levels of priority interrupts from eight sources: six from external sources and two from internal sources.
- Two programmable 8-bit counter/timers each with a 6-bit prescaler. Counter/Timer T0 is driven by an internal source, and Counter/Timer T1 can be driven by internal or external sources. Both counter/timers are independent of program execution.
- 256-byte register file, accessible by both the master CPU and UPC, as allocated in the UPC program.
- 2K bytes of on-chip ROM for efficiency and versatility.

General Description

The Z8590 Universal Peripheral Controller (UPC) is an intelligent peripheral controller for distributed processing applications (Figure 3). The UPC unburdens the host processor by assuming tasks traditionally done by the host (or by added hardware), such as performing arithmetic, translating or formatting data, and controlling I/O devices. Based on the Z8 microcomputer architecture and instruction set, the UPC contains 2K bytes of internal program ROM, a 256-byte register file, three 8-bit I/O ports, and two counter/timers.

The UPC offers fast execution time, an effective use of memory, and sophisticated interrupt, I/O, and bit manipulation. Using a powerful and extensive instruction set combined with an efficient internal addressing scheme, the UPC speeds program execution and efficiently packs program code into the on-chip ROM.

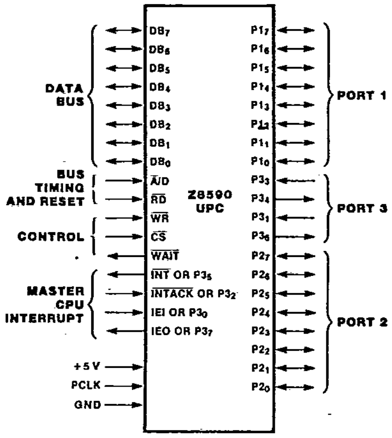

Figure 1. Z8590 UPC Logic Functions

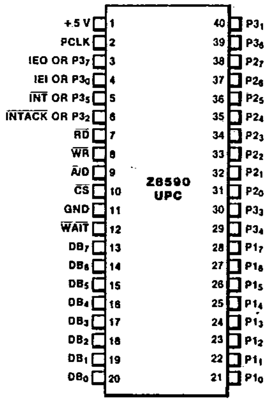

Figure 2. Z8590 UPC Pin Configuration

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General Description (Continued)

An important feature of the UPC is an internal register file containing I/O port and control registers accessed both by the UPC program and indirectly by its associated master CPU. This architecture results in both byte and programming efficiency, because UPC instructions can operate directly on I/O data without moving it to and from an accumulator. Such a structure allows the user to allocate as many general purpose registers as the application requires for data buffers between the CPU and peripheral devices. All general-purpose registers can be used as address pointers, index registers, data buffers, or stack space.

The register file is logically divided into 16 groups, each consisting of 16 working registers. A Register Pointer is used in conjunction with short format instructions, resulting in tight, fast code and easy task switching.

Communication between the master CPU and the register file takes place via one group of 19 interface registers addressed directly by both the master CPU and the UPC, or via a block transfer mechanism. Access by the master CPU is controlled by the UPC to allow independence between the master CPU and UPC software.

The UPC has 24 pins that can be dedicated to I/O functions. Grouped logically into three 8-line ports, they can be programmed in many combinations of input or output lines, with or without handshake, and with push-pull or open-drain outputs. Ports 1 and 2 are bit-programmable; Port 3 has four fixed inputs and four outputs.

To relieve software from coping with real-time counting and timing problems, the UPC has two 8-bit hardware counter/timers, each with a fixed divide-by-four, and a 6-bit programmable prescaler. Various counting modes may be selected.

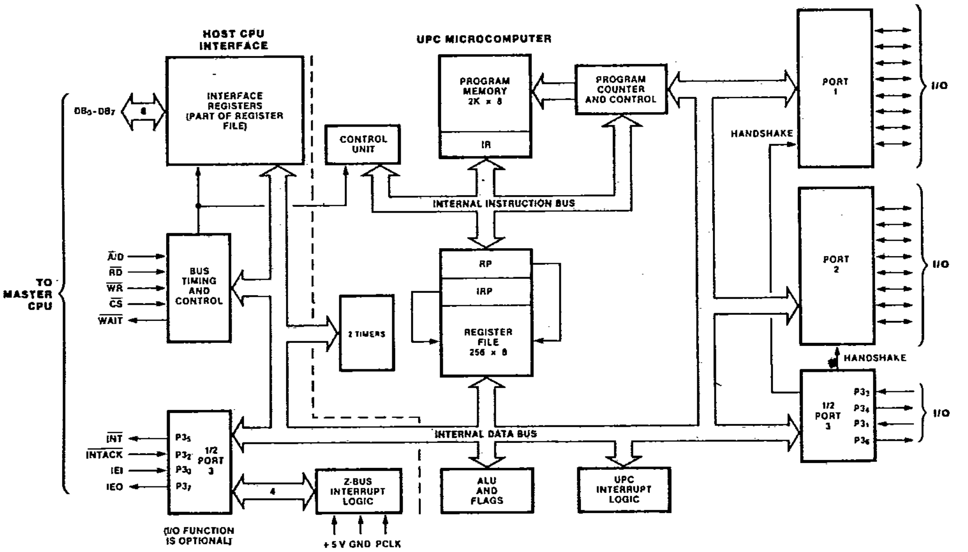

Figure 3. Functional Block Diagram

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General Description (Continued)

In addition to the 40-pin standard configuration, the UPC is available in four special configurations:

- A 64-pin RAM development version with external interface for up to 4K bytes of RAM and 36 bytes of internal ROM permitting down-loading from the master CPU.
- A Protopack RAM version with a socket for up to 2K bytes of RAM, with 36 bytes of internal ROM permitting down-loading from the master CPU.
- A 64-pin ROM development version with external interface for up to 4K bytes of ROM and no internal ROM.
- A Protopack ROM version with a socket for 2K bytes of ROM and no internal ROM.

This range of versions and configurations makes the UPC compatible with most system peripheral device control considerations.

Pin Description

$\overline{\text{A}}$/D. *Address/Data* (input). A Low on this pin defines information on the data bus as an address. A High defines the information as data.

$\overline{\text{CS}}$. *Chip Select* (input, active Low). A Low enables the UPC to accept address or data information from the master CPU during a write cycle or to transmit data to the master CPU during a read cycle. This line is usually generated from higher bits of the address lines.

DB$_0$-DB$_7$. *Data Bus* (bidirectional). This bus is used to transfer address and data information between the master CPU and the UPC.

P1$_0$-P1$_7$, P2$_0$-P2$_7$, P3$_0$-P3$_7$. *I/O Port Lines* (bidirectional, TTL compatible). These 24 lines are divided into three 8-bit I/O ports and may be configured in the following ways under program control:

P1$_0$-P1$_7$. *Port 1* (input/output—as output it can be push-pull or open-drain). Bit-programmable Parallel I/O.

P2$_0$-P2$_7$. *Port 2* (input/output—as output, it can be push-pull or open-drain). Bit-programmable Parallel I/O.

P3$_0$-P3$_7$. *Port 3* (four inputs, four outputs). Parallel I/O, handshake control, timer I/O, or interrupt control.

PCLK. *Clock* (input). TTL-compatible clock input, 4 MHz maximum. This signal does not need to be related to the master CPU clock.

$\overline{\text{RD}}$. *Read* (input, active Low). A Low enables the master CPU to read information from the UPC. Raising the voltage on this pin above V$_{DD}$ will force the UPC into test mode.

$\overline{\text{WAIT}}$. *Wait* (output, active Low, open-drain). When the CPU accesses the UPC register file, this signal requests the master CPU to wait until the UPC can complete its part of the transaction.

$\overline{\text{WR}}$. *Write* (input, active Low). A Low on this pin enables the master CPU to write information to the UPC. A simultaneous Low on $\overline{\text{RD}}$ and $\overline{\text{WR}}$ resets the UPC. It is held in reset as long as $\overline{\text{WR}}$ is Low.

Functional Description

Address Space. On the 40-pin UPC, all address space is committed to on-chip memory. There are 2048 bytes of mask-programmed ROM and 256 bytes of register file. I/O is memory-mapped to three registers in the register file. Only the Protopack and 64-pin versions of the UPC can access external program memory. See the section entitled

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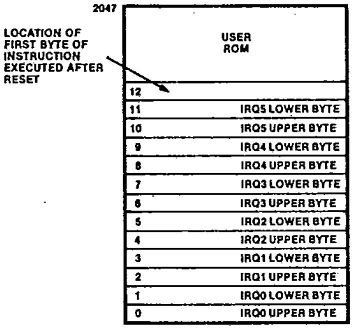
Functional Description (Continued)

"Special Configurations" for complete descriptions of the Protopack and 64-pin versions.

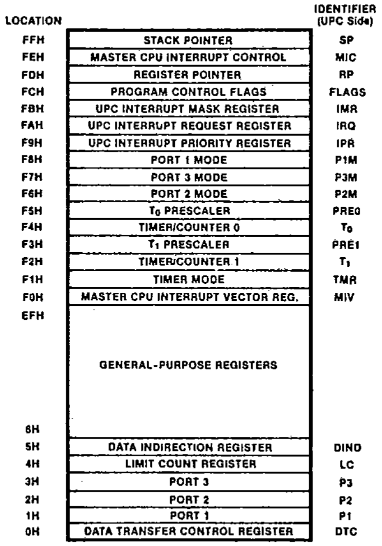
Program Memory. Figure 4 is a map of the 2K on-chip program ROM. Even though the architecture allows addresses from 0 to 4K, behavior of the device above program address 2047 (7FFH) is not defined. The first 12 bytes of program memory are reserved for the UPC interrupt vectors. For the Protopack and 64-pin versions, the address space is extended to 4096 bytes. In the RAM versions, addresses 0CH through 2FH are reserved for on-chip ROM.



LOCATION OF FIRST BYTE OF INSTRUCTION EXECUTED AFTER RESET

2047	USER ROM
12	
11	IRQ5 LOWER BYTE
10	IRQ5 UPPER BYTE
9	IRQ4 LOWER BYTE
8	IRQ4 UPPER BYTE
7	IRQ3 LOWER BYTE
6	IRQ3 UPPER BYTE
5	IRQ2 LOWER BYTE
4	IRQ2 UPPER BYTE
3	IRQ1 LOWER BYTE
2	IRQ1 UPPER BYTE
1	IRQ0 LOWER BYTE
0	IRQ0 UPPER BYTE

Figure 4. Program Memory Map



LOCATION		IDENTIFIER (UPC Side)
FFH	STACK POINTER	SP
FEH	MASTER CPU INTERRUPT CONTROL	MIC
FDH	REGISTER POINTER	RP
FCH	PROGRAM CONTROL FLAGS	FLAGS
FBH	UPC INTERRUPT MASK REGISTER	IMR
FAH	UPC INTERRUPT REQUEST REGISTER	IRQ
F9H	UPC INTERRUPT PRIORITY REGISTER	IPR
F8H	PORT 1 MODE	P1M
F7H	PORT 3 MODE	P3M
F6H	PORT 2 MODE	P2M
F5H	T_0 PRESCALER	PRE0
F4H	TIMER/COUNTER 0	T_0
F3H	T_1 PRESCALER	PRE1
F2H	TIMER/COUNTER 1	T_1
F1H	TIMER MODE	TMR
F0H	MASTER CPU INTERRUPT VECTOR REG.	MIV
EFH	GENERAL-PURPOSE REGISTERS	
6H		
5H	DATA INDIRECTION REGISTER	DIND
4H	LIMIT COUNT REGISTER	LC
3H	PORT 3	P3
2H	PORT 2	P2
1H	PORT 1	P1
0H	DATA TRANSFER CONTROL REGISTER	DTC

Figure 5. Register File Organization

Register File. This 256-byte file includes three I/O port registers (1-3H), 234 general-purpose registers (6-EEH), and 19 control, status and special I/O registers (0H, 4H, 5H, and F0-FFH). The functions and mnemonics assigned to these register address locations are shown in Figure 5. Of the 256 UPC registers, 19 can be directly accessed by the master CPU; the others are accessed indirectly via the block transfer mechanism.

The I/O port and control registers are included in the register file without differentiation. This allows any UPC instruction to process I/O or control information, thereby eliminating the need for special I/O and control instructions. All general-purpose registers can function as accumulators, address pointers, or index registers. In instruction execution, the registers are read when they are defined as sources and written when defined as destinations.

UPC instructions may access registers directly or indirectly using an 8-bit address mode or a 4-bit address mode and a Register Pointer. For the 4-bit addressing mode, the file is divided into 16 working register groups, each occupying 16 contiguous locations (Figure 6). The Register Pointer (RP) addresses the starting point of the active working-register group, and the 4-bit register designator supplied by the instruction specifies the register within the group. Any instruction altering the contents of the register file can also alter the Register Pointer. The UPC instruction set has a special Set Register Pointer (SRP) instruction for initializing or altering the pointer contents.

Stacks. An 8-bit Stack Pointer (SP), register R255, is used for addressing the stack, residing within the 234 general-purpose

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Functional Description (Continued)

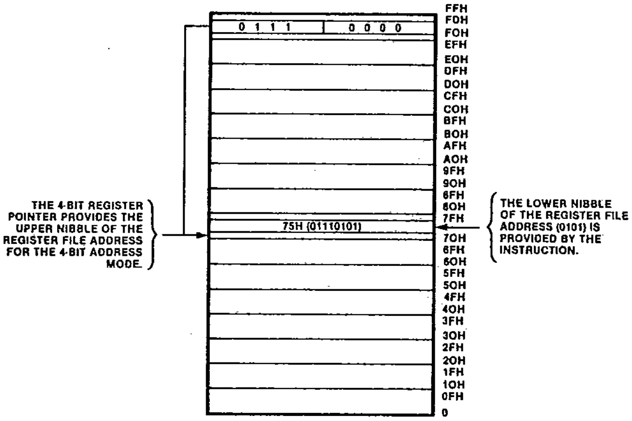
FFH
F0H
0 1 1 1
0 0 0 0
F0H
EFH
E0H
DFH
D0H
CFH
C0H
BFH
B0H
AFH
A0H
9FH
90H
8FH
80H
7FH
75H (01110101)
70H
6FH
60H
5FH
50H
4FH
40H
3FH
30H
2FH
20H
1FH
10H
0FH
0
THE 4-BIT REGISTER POINTER PROVIDES THE UPPER NIBBLE OF THE REGISTER FILE ADDRESS FOR THE 4-BIT ADDRESS MODE.
THE LOWER NIBBLE OF THE REGISTER FILE ADDRESS (0101) IS PROVIDED BY THE INSTRUCTION.

Figure 6. Register Pointer Mechanism

registers, address location 6H through EFH. PUSH and POP instructions can save and restore any register in the register file on the stack. During CALL instructions, the Program Counter is automatically saved on the stack. During UPC interrupt cycles, the Program Counter and the Flag register are automatically saved on the stack. The RET and IRET instructions pop the saved values of the Program Counter and Flag register.

Ports. The UPC has 24 lines dedicated to input and output. These are grouped into three ports of eight lines each and can be configured under software control as inputs, outputs, or special control signals. They can be programmed to provide Parallel I/O with or without handshake and timing signals. All outputs can have active pullups and pulldowns, compatible with TTL loads. In addition, they may be configured as open-drain outputs.

Port 1. Individual bits of Port 1 can be configured as input or output by programming Port 1 Mode register (P1M) F8H. This port is accessed by the UPC program as general register 1H. It is written by specifying address 1H as the destination of any instruction used to store data in the output register. The port is read by specifying address 1H as the source of an instruction.

Port 1 may be placed under handshake control by programming Port 3 Mode register (P3M) F7H. This configures Port 3 pins $P3_3$ and $P3_4$ as handshake control lines $\overline{DAV}_1$ and RDY_1 for input handshake, or RDY_1 and $\overline{DAV}_1$ for output handshake, as determined by the direction (input or output) assigned to bit 7 of Port 1. The Port 3 Mode register also has a bit that programs Port 1 for open-drain output.

Port 2. Individual bits of Port 2 can be configured as inputs or outputs by programming Port 2 Mode register (P2M) F6H. This port is accessed by the UPC program as general register 2H, and its functions and methods of programming are the same as those of Port 1.

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Functional Description (Continued)

Port 3 pins P3$_1$ and P3$_6$ are the handshake lines $\overline{DAV}_2$ and RDY$_2$, with the direction (input or output) determined by the state of bit 7 of the port. The Port 3 Mode register also has a bit used to program Port 2 for open-drain output.

Port 3. This port can be configured as I/O or control lines by programming the Port 3 Mode register. Port 3 is accessed as general register 3H. The directions of the eight data lines are fixed. Four lines, P3$_0$ through P3$_3$, are inputs, and the other four, P3$_4$ through P3$_7$, are outputs. The control functions performed by Port 3 are listed in Table 1.

Counter/Timers. The UPC contains two 8-bit programmable counter/timers, each driven by an internal 6-bit programmable prescaler.

The T1 prescaler can be driven by internal or external clock sources. The T0 prescaler is driven by an internal clock source. Both counter/timers operate independently of the processor instruction sequence to relieve the program from time-critical operations like event counting or elapsed-time calculation. T0 Prescaler register (PRE0) F5H and T1 Prescaler register (PRE1) F3H can be programmed to divide the input frequency of the source being counted by any number from 1 to 64. A counter register (F2H or F4H) is loaded with a number from 1 to 256. The corresponding counter is decremented from this number each time the prescaler reaches end-of-count. When the count is complete, the counter issues a timer interrupt request; IRQ$_4$ for T0 or IRQ$_5$ for T1. Loading either counter with a number (n) results in the interruption of the UPC at the nth count.

Function	Line	Direction	Signal
Handshake	P3$_1$	In	$\overline{DAV}_2$/RDY$_2$
	P3$_3$	In	$\overline{DAV}_1$/RDY$_1$
	P3$_4$	Out	RDY$_1$/$\overline{DAV}_1$
	P3$_6$	Out	RDY$_2$/$\overline{DAV}_2$
UPC Interrupt Request*	P3$_0$	In	IRQ$_3$
	P3$_1$	In	IRQ$_2$
	P3$_3$	In	IRQ$_1$
Counter/Timer	P3$_1$	In	T$_{7N}$
	P3$_6$	Out	T$_{OUT}$
Master CPU	P3$_5$	Out	$\overline{INT}$
	P3$_2$	In	$\overline{INTACK}$
	P3$_0$	In	IEI
	P3$_7$	Out	IEO
Test Mode	P3$_5$	Out	$\overline{A}$/D

*P3$_0$, P3$_1$, and P3$_3$ can always be used as UPC interrupt request inputs, regardless of the configuration programmed.

Table 1. Port 3 Control Functions

The counters can be started, stopped, restarted to continue, or restarted from the initial value. They can be programmed to stop upon reaching end-of-count (Single-Pass mode) or to automatically reload the initial value and continue counting (Modulo-n Continuous mode). The counters and prescalers can be read at any time without disturbing their values or changing their counts. The clock sources for both timers can be defined as any one of the following:

- UPC internal clock (4 MHz maximum) divided by four.
- External clock input to Counter/Timer T1 via P3$_1$ (1 MHz maximum).
- Retriggerable trigger input for the UPC internal clock divided by four.
- Nonretriggerable trigger input for the UPC internal clock divided by four.
- External gate input for the UPC internal clock divided by four.

Interrupts. The UPC allows six interrupts from eight different sources as follows:

- Port 3 lines P3$_0$, P3$_2$, and P3$_3$.
- The master CPU(3).
- The two counter/timers.

These interrupts can be masked and globally enabled or disabled using Interrupt Mask Register (IMR) FBH. Interrupt Priority Register (IPR) F9H specifies the order of their priority. All UPC interrupts are vectored.

Table 2 lists the UPC's interrupt sources, their types, and their vector locations in program ROM. Interrupt Request IRQ$_6$ is dedicated to master CPU communications.

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Functional Description (Continued)

Name	Source	Vector Location	Comments
IRQ_0	EOM, XERR, LERR	0,1	Internal (R0 Bits 0, 1, 2)
IRQ_1	$\overline{DAV}_1$, IRQ_1	2,3	External ($P3_3$) ↓ Edge Triggered
IRQ_2	$\overline{DAV}_2$, IRQ_2, T_{IN}	4,5	External ($P3_1$) ↓ Edge Triggered
IRQ_3	IRQ_3, IEI	6,7	External ($P3_0$) ↓ Edge Triggered
IRQ_4	T0	8,9	Internal
IRQ_5	T1	10,11	Internal

Table 2. Interrupt Types, Sources, and Vector Locations

Interrupt Requests IRQ_1, IRQ_2, and IRQ_3 are generated on the falling transitions of external inputs $P3_3$, $P3_1$, and $P3_0$. Interrupt Requests IRQ_4 and IRQ_5 are generated upon the timeout of the UPC's two counter/timers. When an interrupt request is granted, the UPC enters an interrupt machine cycle. This cycle disables all subsequent interrupts, saves the Program Counter and Status Flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

The UPC also supports polled systems. To accommodate a polled structure, any or all of the interrupt inputs can be masked and the Interrupt Request register polled to determine which of the interrupt requests needs service.

Following any hardware reset operation, an EI instruction must be executed to enable the setting of any interrupt request bit in the IRQ register. Interrupts must be disabled prior to changing the content of either the IPR (F9H) or the IMR (FBH). DI is the only instruction that should be used to globally disable interrupts.

Master CPU Register File Access. There are two ways in which the master CPU can access the UPC register file: direct access and block access.

Direct Access. Three UPC registers—the Data Transfer Control (0H), the Master Interrupt Vector (F0H), and the Master Interrupt Control (FEH)—are mapped directly into the master CPU address space. The master CPU accesses these registers via the addresses shown in Table 3.

UPC Address		Identifier	Address
Decimal	Hex		
0	0H	DTC	xxx11000
5	5H	DIND	
@5**	@5H**		xxx11111
240	FOH	MIV	xxx10000
254	FEH	MIC	xxx11110
*n		DSC0	xxx00000
n+1		DSC1	xxx00001
n+2		DSC2	xxx00010
n+3		DSC3	xxx00011
n+4		DSC4	xxx00100
n+5		DSC5	xxx00101
n+6		DSC6	xxx00110
n+7		DSC7	xxx00111
n+8		DSC8	xxx01000
n+9		DSC9	xxx01001
n+10		DSCA	xxx01010
n+11		DSCB	xxx01011
n+12		DSCC	xxx01100
n+13		DSCD	xxx01101
n+14		DSCE	xxx01110
n+15		DSCF	xxx01111

x = don't care
*n is the value in the IRP x 16
**Master CPU accesses the register address in Register 5.

Table 3. Master CPU/UPC Register Map

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Functional Description (Continued)

The master CPU also has direct access to 16 registers known as the DSC (Data, Status, Command) registers. The DSC registers are numbered 0 through F (DSC0-DSCF). These registers can be any 16 contiguous register file registers beginning on a 16-byte boundary. The base address of the DSC register group is designated by the IRP (I/O Register Pointer), which is bits D_4-D_7 of the Data Transfer Control register (0H). Figure 7 shows how the register address is made up of the 4-bit IRP field, concatenated with the low order 4-bits of the address from the master CPU.

Block Access. The master CPU may transmit or receive blocks of data via address xxx11111. When the master CPU accesses this address, the UPC register pointed to by the Data Indirection register is read or written. The Data Indirection register is incremented, and the Limit Count register is decremented, for example, when the master CPU issues a read or write to address xxx11111 while the Data Indirection register contains the value 33H. The operation causes register 33H to be read or written and the Data Indirection register to be incremented to 34H. This scheme is well suited to Block I/O Instructions and allows the master CPU to efficiently read or write a block of data to or from the UPC.

The Limit Count register (04H) is decremented and is used to control the number of bytes to be transferred by master CPU block accesses. If the master CPU attempts a read or write to the UPC after the Limit Count register reaches 0, the access is not completed, the LERR bit (D_2) of the Data Transfer Control register is set (indicating a limit error), and the LERR error causes an IRQ_0 interrupt request.

The IRP field of the Data Transfer Control register, the Data Indirection register, and the Limit Count register are not directly accessible to the master CPU and therefore must be set by the UPC. This allows the UPC to protect itself from master CPU errors and frees the master CPU from tracking the UPC's internal data layout.

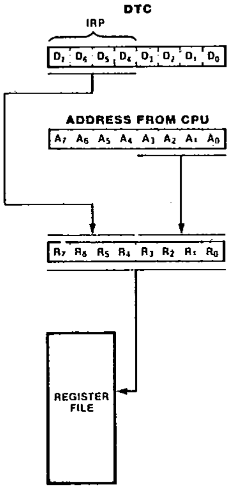

Figure 7. DSC Register Addressing Scheme

Special Configurations

There are two Protopack and two 64-pin versions of the UPC. These versions are identical to the 40-pin UPC with the following exceptions:

- Internal ROM is totally omitted from the 64-pin development (Z8591) and piggyback ROM (Z8593) versions.
- All but 36 bytes of internal ROM are omitted from the 64-pin RAM (Z8592) and piggyback (RAM) (Z8594) versions.
- The memory address and data lines are buffered and brought out to external pins or to the socket on the Protopack.
- Control lines for the external memory are also provided.

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Special Configurations (Continued)

The 64-pin version of the UPC allows the user to prototype the system in hardware with an actual UPC device and to develop the code intended to be mask programmed into the on-chip ROM of the 40-pin UPC for the production system. The 64-pin or piggyback RAM versions of the UPC are extremely versatile parts. Memory space can be extended to 4K bytes on the 64-pin version by using external RAM/ROM for all but 36 bytes of the UPC's memory space. This memory can then be down-loaded from the master CPU using a bootstrap program stored in the 36 bytes (C–2F). Figure 8 is a memory map for the 64-pin RAM version.

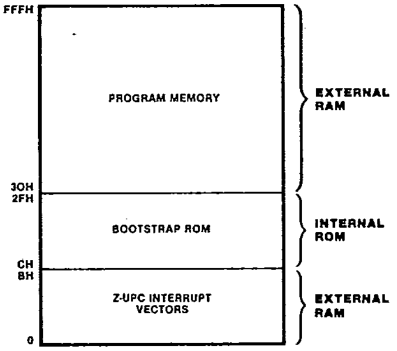

Figure 8. UPC RAM Version Memory Map

64-Pin and Protopack Pin Functions. Forty of the pins on the 64-pin and Protopack versions have functions identical to those of the 40-pin version. The remaining 24 pins have additional functions described below. (Figures 9 through 11 show the 64-pin and Protopack versions' pin functions and pin assignments.)

A_0-A_{11}. *Program Memory Address Lines* (output). These lines are identical in all 64-pin and RAM versions in the Protopack. They are used to address 4K bytes of external UPC memory.

D_0-D_7. *Program Data* (input). Data is read in from the external memory on these lines. The RAM version also writes external memory through this bus.

IACK. *Interrupt Acknowledge* (output, active High). This signal is active whenever an internal UPC interrupt cycle is in process.

$\overline{\text{MAS}}$. *Memory Address Strobe* (output, active Low). This address strobe is pulsed once for each memory fetch to interface with quasi-static RAM.

$\overline{\text{MDS}}$. *Memory Data Strobe* (output, active Low). This signal is Low during an instruction fetch or memory write.

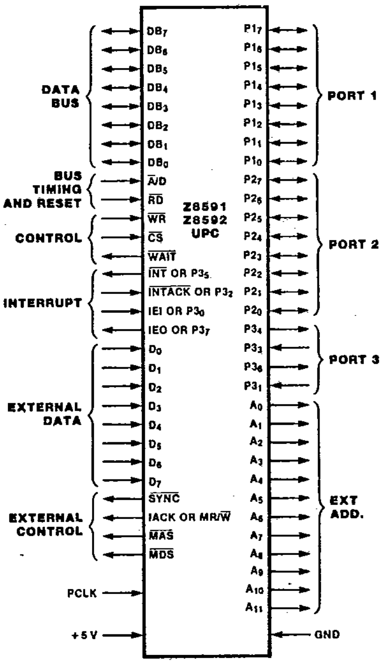

Figure 9. Z8591/Z8592 UPC Logic Functions

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Special Configurations (Continued)

MR/$\overline{\textbf{W}}$. *Memory Read/Write* (output RAM versions only). This signal is High when the UPC is fetching an instruction and Low when it is loading external memory.

$\overline{\textbf{SYNC}}$. *Instruction Sync* (output, active Low). This signal is Low during the clock cycle just preceding an opcode fetch.

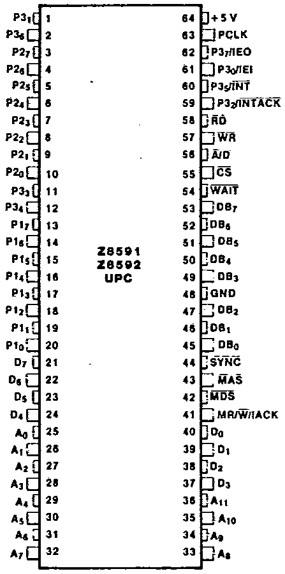

Figure 10. Z8591/Z8592 UPC Pin Configuration

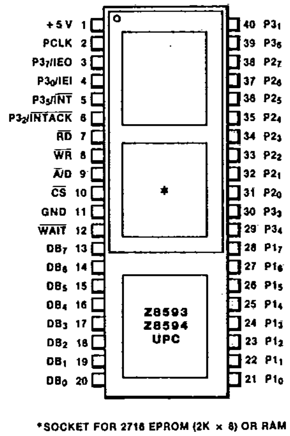

Figure 11. Z8593/Z8594 UPC Piggyback EPROM/RAM Pin Configuration

Addressing Modes

The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working-register pair address
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate

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Additional Symbols

dst	Destination location or contents
src	Source location or contents
cc	Condition code (see list)
@	Indirect address prefix
SP	Stack Pointer (control register FFH)
PC	Program Counter
FLAGS	Flag register (control register FCH)
RP	Register Pointer (control register FDH)
IMR	Interrupt Mask register (control register FBH)

Assignment of a value is indicated by the symbol "←". For example,

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr(n)" is used to refer to bit "n" of a given location. For example,

dst (7)

refers to bit 7 of the destination operand.

Flags

Control Register FCH contains the following six flags:

C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Cleared to zero
1	Set to one
*****	Set or cleared according to operation
–	Unaffected
X	Undefined

Condition Codes

Value	Mnemonic	Meaning	Flags Set
1000		Always true	—
0111	C	Carry	C = 1
1111	NC	No carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000		Never true	—

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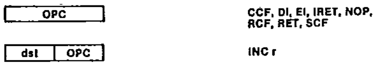
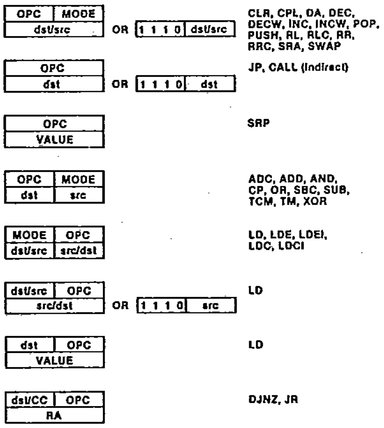
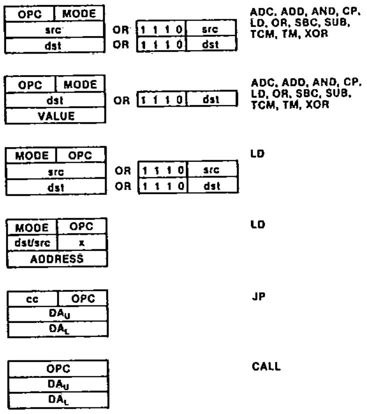
Instruction Formats



One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

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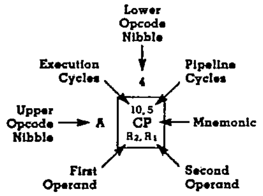
Opcode Map

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6,5 DEC R_1	6,5 DEC IR_1	6,5 ADD r_1, r_2	6,5 ADD r_1, Ir_2	10,5 ADD R_2, R_1	10,5 ADD IR_2, R_1	10,5 ADD R_1, IM	10,5 ADD IR_1, IM	6,5 LD r_1, R_2	6,5 LD r_2, R_1	12-10,5 DJNZ r_1, RA	12/10,0 JR cc, RA	6,5 LD r_1, IM	12/10,0 JP cc, DA	6,5 INC r_1	
1	6,5 RLC R_1	6,5 RLC IR_1	6,5 ADC r_1, r_2	6,5 ADC r_1, Ir_2	10,5 ADC R_2, R_1	10,5 ADC IR_2, R_1	10,5 ADC R_1, IM	10,5 ADC IR_1, IM	│	│	│	│	│	│	│	
2	6,5 INC R_1	6,5 INC IR_1	6,5 SUB r_1, r_2	6,5 SUB r_1, Ir_2	10,5 SUB R_2, R_1	10,5 SUB IR_2, R_1	10,5 SUB R_1, IM	10,5 SUB IR_1, IM	│	│	│	│	│	│	│	
3	8,0 JP IRR_1	6,1 SRP IM	6,5 SBC r_1, r_2	6,5 SBC r_1, Ir_2	10,5 SBC R_2, R_1	10,5 SBC IR_2, R_1	10,5 SBC R_1, IM	10,5 SBC IR_1, IM	│	│	│	│	│	│	│	
4	8,5 DA R_1	8,5 DA IR_1	6,5 OR r_1, r_2	6,5 OR r_1, Ir_2	10,5 OR R_2, R_1	10,5 OR IR_2, R_1	10,5 OR R_1, IM	10,5 OR IR_1, IM	│	│	│	│	│	│	│	
5	10,5 POP R_1	10,5 POP IR_1	6,5 AND r_1, r_2	6,5 AND r_1, Ir_2	10,5 AND R_2, R_1	10,5 AND IR_2, R_1	10,5 AND R_1, IM	10,5 AND IR_1, IM	│	│	│	│	│	│	│	
6	6,5 COM R_1	6,5 COM IR_1	6,5 TCM r_1, r_2	6,5 TCM r_1, Ir_2	10,5 TCM R_2, R_1	10,5 TCM IR_2, R_1	10,5 TCM R_1, IM	10,5 TCM IR_1, IM	│	│	│	│	│	│	│	
7	10/12,1 PUSH R_2	12/14,1 PUSH IR_2	6,5 TM r_1, r_2	6,5 TM r_1, Ir_2	10,5 TM R_2, R_1	10,5 TM IR_2, R_1	10,5 TM R_1, IM	10,5 TM IR_1, IM	│	│	│	│	│	│	│	
8	10,5 DECW RR_1	10,5 DECW IR_1	12,0 LDE r_1, Irr_2	18,0 LDEI Ir_1, Irr_2					│	│	│	│	│	│	│	6,1 DI
9	6,5 RL R_1	6,5 RL IR_1	12,0 LDE r_2, Irr_1	18,0 LDEI Ir_2, Irr_1					│	│	│	│	│	│	│	6,1 EI
A	10,5 INCW RR_1	10,5 INCW IR_1	6,5 CP r_1, r_2	6,5 CP r_1, Ir_2	10,5 CP R_2, R_1	10,5 CP IR_2, R_1	10,5 CP R_1, IM	10,5 CP IR_1, IM	│	│	│	│	│	│	│	14,0 RET
B	6,5 CLR R_1	6,5 CLR IR_1	6,5 XOR r_1, r_2	6,5 XOR r_1, Ir_2	10,5 XOR R_2, R_1	10,5 XOR IR_2, R_1	10,5 XOR R_1, IM	10,5 XOR IR_1, IM	│	│	│	│	│	│	│	16,0 IRET
C	6,5 RRC R_1	6,5 RRC IR_1	12,0 LDC r_1, Irr_2	18,0 LDCI Ir_1, Irr_2				10,5 LD r_1, x, R_2	│	│	│	│	│	│	│	6,5 RCF
D	6,5 SRA R_1	6,5 SRA IR_1	12,0 LDC r_2, Irr_1	18,0 LDCI Ir_2, Irr_1	20,0 CALL* IRR_1		20,0 CALL DA	10,5 LD r_2, x, R_1	│	│	│	│	│	│	│	6,5 SCF
E	6,5 RR R_1	6,5 RR IR_1		6,5 LD r_1, Ir_2	10,5 LD R_2, R_1	10,5 LD IR_2, R_1	10,5 LD R_1, IM	10,5 LD IR_1, IM	│	│	│	│	│	│	│	6,5 CCF
F	6,7 SWAP R_1	6,7 SWAP IR_1		6,5 LD Ir_1, r_2		10,5 LD R_2, IR_1			↓	↓	↓	↓	↓	↓	↓	6,0 NOP
Bytes per Instruction	2				3				2					3	1	



Legend:
R = 8-Bit Address
r = 4-Bit Address
R_1 or r_1 = Dst Address
R_2 or r_2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank areas are not defined.

*2-byte instruction; fetch cycle appears as a 3-byte instruction.

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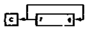
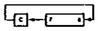
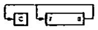
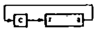
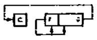
SGS Z8590 UPC

Instruction Summary

Instruction and Operation	Addr Mode		Opcode Byte (Hex)	Flags Affected					
	dst	src		C	Z	S	V	D	H
ADC dst,src dst ← dst + src + C	(Note 1)		1□	*	*	*	*	0	*
ADD dst,src dst ← dst + src	(Note 1)		0□	*	*	*	*	0	*
AND dst,src dst ← dst AND src	(Note 1)		5□	-	*	*	0	-	-
CALL dst SP ← SP - 2 @SP ← PC; PC ← dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C ← NOT C			EF	*	-	-	-	-	-
CLR dst dst ← 0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst ← NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst,src dst - src	(Note 1)		A□	*	*	*	*	-	-
DA dst dst ← DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst ← dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst ← dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR (7) ← 0			8F	-	-	-	-	-	-
DJNZ r,dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA		rA r=0-F	-	-	-	-	-	-
EI IMR (7) ← 1			9F	-	-	-	-	-	-
INC dst dst ← dst + 1	r R IR		rE r=0-F 20 21	-	*	*	*	-	-
INCW dst dst ← dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR (7) ← 1			BF	*	*	*	*	*	*
JP cc,dst if cc is true PC ← dst	DA IRR		cD c=0-F 30	-	-	-	-	-	-
JR cc,dst if cc is true, PC ← PC + dst Range: +127, -128	RA		cB c=0-F	-	-	-	-	-	-
LD dst,src dst ← src	r r R r X r Ir R R R IR IR	IM R r X r Ir r R IR IM IM R	rC r8 r9 r=0-F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst,src dst ← src	r Irr	Irr r	C2 D2	-	-	-	-	-	-
LDCI dst,src dst ← src r ← r + 1; rr ← rr + 1	Ir Irr	Irr Ir	C3 D3	-	-	-	-	-	-
LDE dst,src dst ← src	r Irr	Irr r	82 92	-	-	-	-	-	-
LDEI dst,src dst ← src r ← r + 1; rr ← rr + 1	Ir Irr	Irr Ir	83 93	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-
OR dst,src dst ← dst OR src	(Note 1)		4□	-	*	*	0	-	-
POP dst dst ← @SP SP ← SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP ← SP - 1; @SP ← src		R IR	70 71	-	-	-	-	-	-
RCF C ← 0			CF	0	-	-	-	-	-
RET PC ← @SP; SP ← SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst,src dst ← dst - src - C	(Note 1)		3□	*	*	*	*	1	*
SCF C ← 1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-

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Instruction Summary (Continued)

Instruction and Operation	Addr Mode		Opcode Byte (Hex)	Flags Affected					
	dst	src		C	Z	S	V	D	H
SRP src RP ← src		Im	31	–	–	–	–	–	–
SUB dst,src dst ← dst – src	(Note 1)		2□	*	*	*	*	1	*
SWAP dst	R IR		F0 F1	X	*	*	X	–	–
TCM dst,src (NOT dst) AND src	(Note 1)		6□	–	*	*	0	–	–
TM dst,src dst AND src	(Note 1)		7□	–	*	*	0	–	–
XOR dst,src dst ← dst XOR src	(Note 1)		B□	–	*	*	0	–	–

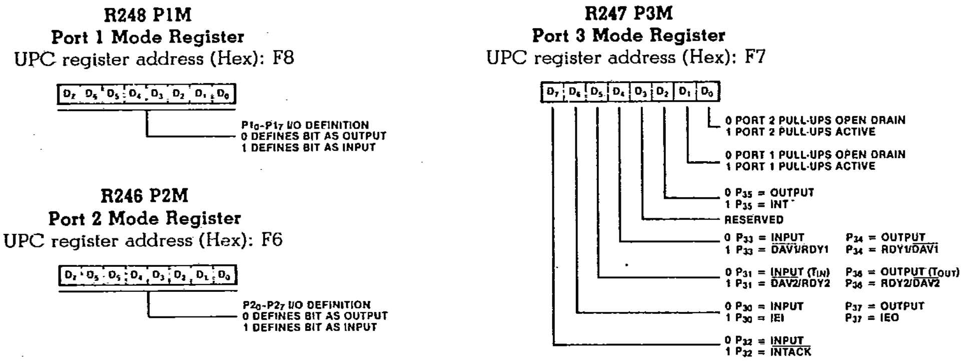
Note 1

These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a □ in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, to determine the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Addr Mode		Lower Opcode Nibble
dst	src	
r	r	2
r	Ir	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

Registers



R248 P1M
Port 1 Mode Register
UPC register address (Hex): F8

R246 P2M
Port 2 Mode Register
UPC register address (Hex): F6

R247 P3M
Port 3 Mode Register
UPC register address (Hex): F7

Figure 12. Port Mode Registers

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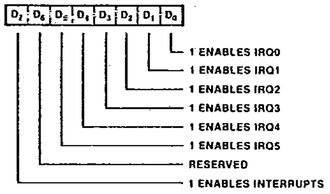
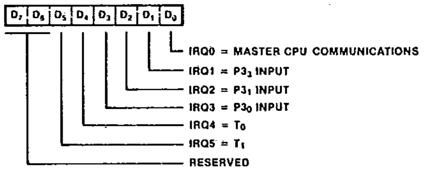
Registers (Continued)

R251 IMR
Interrupt Mask Register
UPC register address (Hex): FB



R250 IRQ
Interrupt Request Register
UPC register address (Hex): FA



R249 IPR
Interrupt Priority Register
UPC register address (Hex): F9 (Write Only)

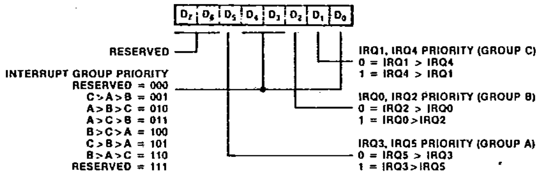
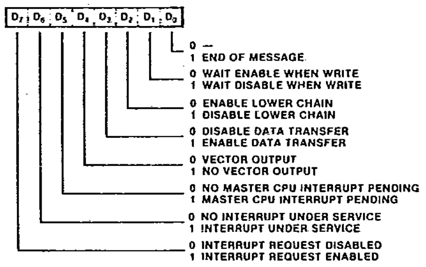


Figure 13. Interrupt Control Registers

R254 MIC
Master CPU Interrupt Control Register
UPC register address (Hex): FE


D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0 —
1 END OF MESSAGE
0 WAIT ENABLE WHEN WRITE
1 WAIT DISABLE WHEN WRITE
0 ENABLE LOWER CHAIN
1 DISABLE LOWER CHAIN
0 DISABLE DATA TRANSFER
1 ENABLE DATA TRANSFER
0 VECTOR OUTPUT
1 NO VECTOR OUTPUT
0 NO MASTER CPU INTERRUPT PENDING
1 MASTER CPU INTERRUPT PENDING
0 NO INTERRUPT UNDER SERVICE
1 INTERRUPT UNDER SERVICE
0 INTERRUPT REQUEST DISABLED
1 INTERRUPT REQUEST ENABLED

R240 MIV
Master CPU Interrupt Vector Register
UPC register address (Hex): F0

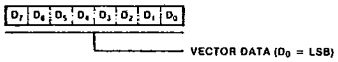

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
VECTOR DATA (D_0 = LSB)

Figure 14. Master CPU Interrupt Registers

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Registers (Continued)

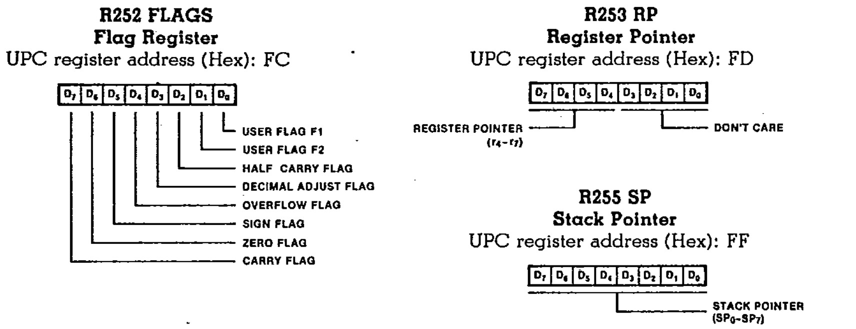

Figure 15. UPC Control Registers

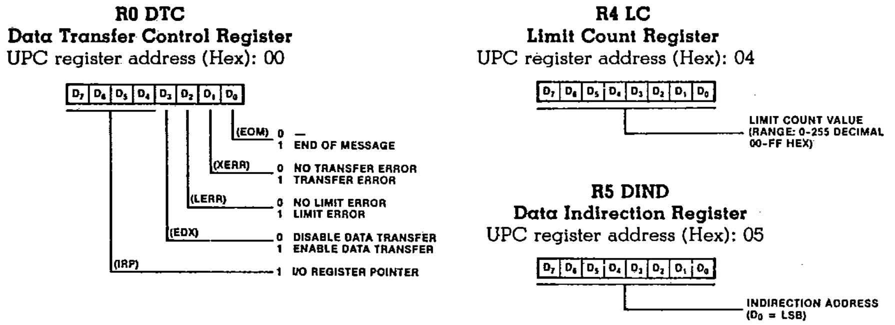
R0 DTC
Data Transfer Control Register
UPC register address (Hex): 00
D7 D6 D5 D4 D3 D2 D1 D0
(EOM) 0 —
1 END OF MESSAGE
(XERR) 0 NO TRANSFER ERROR
1 TRANSFER ERROR
(LERR) 0 NO LIMIT ERROR
1 LIMIT ERROR
(EDX) 0 DISABLE DATA TRANSFER
1 ENABLE DATA TRANSFER
(IRP) 1 I/O REGISTER POINTER
R4 LC
Limit Count Register
UPC register address (Hex): 04
D7 D6 D5 D4 D3 D2 D1 D0
LIMIT COUNT VALUE (RANGE: 0-255 DECIMAL 00-FF HEX)
R5 DIND
Data Indirection Register
UPC register address (Hex): 05
D7 D6 D5 D4 D3 D2 D1 D0
INDIRECTION ADDRESS (D0 = LSB)

Figure 16. Master CPU-UPC Data Transfer Registers

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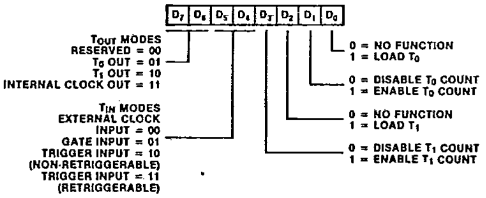
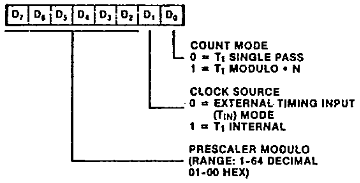
Registers (Continued)

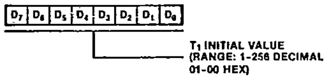
R241 TMR
Timer Mode Register
UPC register address (Hex): F1



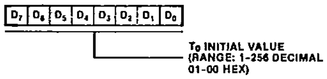
R243 PRE1
Prescaler 1 Register
UPC register address (Hex): F3



R242 T1
Counter/Timer 1 Register
UPC register address (Hex): F2



R244 T0
Counter/Timer 0 Register
UPC register address (Hex): F4



R245 PRE0
Prescaler 0 Register
UPC register address (Hex): F5

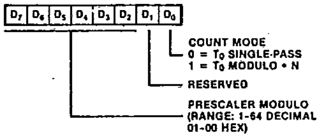


Figure 17. UPC Counter/Timer Registers

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Registers (Continued)

Control Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Comments
00_H Data Transfer Control Register	X	X	X	X	0	0	0	0	Disable data transfer from master CPU
04_H Limit Count Register				Not Defined					
05_H Data Indirection Register				Not Defined					
$F0_H$ Interrupt Vector Register				Not Defined					
$F1_H$ Timer Mode	0	0	0	0	0	0	0	0	Stops T0 and T1
$F2_H$ T0 Register				Not Defined					
$F3_H$ T0 Prescaler	X	X	X	X	X	X	0	0	Single-Pass mode
$F4_H$ T1 Register				Not Defined					
$F5_H$ T1 Prescaler	X	X	X	X	X	X	0	0	Single-Pass mode External clock source
$F6_H$ Port 2 Mode	1	1	1	1	1	1	1	1	Port 2 lines defined as inputs
$F7_H$ Port 3 Mode	0	0	0	0	X	1	0	0	Port 1, 2 open drain; $P3_5$ = INT; $P3_0$, $P3_1$, $P3_2$, $P3_3$ defined as input; $P3_4$, $P3_6$, $P3_7$ defined as output.
$F8_H$ Port 1 Mode	1	1	1	1	1	1	1	1	Port 1 lines defined as inputs
$F9_H$ Interrupt Priority				Not Defined					
FA_H Interrupt Request	X	X	0	0	0	0	0	0	Reset Interrupt Request
FB_H Interrupt Mask	0	X	X	X	X	X	X	X	Interrupts disabled
FC_H Flag Register				Not Defined					
FD_H Register Pointer				Not Defined					
FE_H Master CPU Interrupt Control Register	0	0	0	0	0	0	0	0	Master CPU interrupt disabled; wait enable when write; lower chain enabled
FF_H Stack Pointer				Not Defined					

NOTE: X means not defined.

Table 4. Control Register Reset Conditions

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Absolute Maximum Rating

Voltages on all pins (except V_{BB})
with respect to GND..........-0.5 V to +7.0 V
Operating Ambient
Temperature..................0°C to +70°C
Storage Temperature........-65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

- $+4.75\text{ V} \leq V_{CC} \leq +5.25\text{ V}$
- $V_{SS} = \text{GND} = 0\text{ V}$
- $0°\text{C} \leq T_A \leq +70°\text{C}$

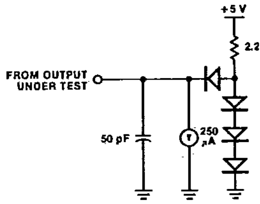

Figure 18. Test Load 1

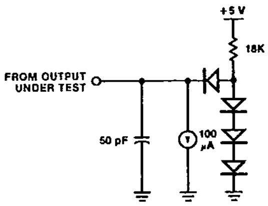

Figure 19. Test Load 2

DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition	Notes
V_{CH}	Clock Input High Voltage	2.4	V_{CC}	V		
V_{CL}	Clock Input Low Voltage	-0.3	0.8	V		
V_{IH}	Input High Voltage	2.0	V_{CC}	V		
V_{IL}	Input Low Voltage	-0.3	0.8	V		
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -250\ \mu A$	1
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = +2.0\text{ mA}$	1
I_{IL}	Input Leakage	-10	10	µA	$0 \leq V_{IN} \leq +5.25\text{ V}$	
I_{OL}	Output Leakage	-10	10	µA	$0 \leq V_{IN} \leq +5.25\text{ V}$	
I_{CC}	V_{CC} Supply Current		180	mA		

[1] For A_0-A_{11} and D_0-D_7, $\overline{\text{MDS}}$, $\overline{\text{SYNC}}$, $\overline{\text{MAS}}$, and MR/$\overline{\text{W}}$/IACK on the 64-pin versions. $I_{OH} = 100\ \mu A$ and $I_{OL} = 1.0\text{ mA}$.

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Master CPU Interface Timing

Number	Symbol	Parameter	Min (ns)	Max (ns)	Notes*
1	TrC	Clock Rise Time		20	
2	TwCh	Clock High Width	105	1855	
3	TfC	Clock Fall Time		20	
4	TwCl	Clock Low Width	105	1855	
5	TpC	Clock Period	250	2000	
6	TsA/D(WR)	$\overline{A}$/D to $\overline{WR}$ ↓ Setup Time	80		
7	TsA/D(RD)	$\overline{A}$/D to $\overline{RD}$ ↓ Setup Time	80		
8	ThA/D(WR)	$\overline{A}$/D to $\overline{WR}$ ↑ Hold Time	30		
9	ThA/D(RD)	$\overline{A}$/D to $\overline{RD}$ ↑ Hold Time	30		
10	TsCSf(WR)	$\overline{CS}$ ↓ to$\overline{WR}$ ↓ SetupTime	0		
11	TsCSf(RD)	$\overline{CS}$ ↓ to $\overline{RD}$ ↓ Setup Time	0		
12	TsCSr(WR)	$\overline{CS}$ ↑ to $\overline{WR}$ ↓ Setup Time	60		
13	TsCSr(RD)	$\overline{CS}$ ↑ to $\overline{RD}$ ↓ Setup Time	60		
14	ThCS(WR)	$\overline{CS}$ to $\overline{WR}$ ↓ Hold Time	0		
15	ThCS(RD)	$\overline{CS}$ to $\overline{RD}$ ↓ Hold Time	0		
16	TsDI(WR)	Data in to $\overline{WR}$ ↓ Setup Time	0		
17	Tw(WR)	$\overline{WR}$ Low Width	390		
18	Tw(RD)	$\overline{RD}$ Low Width	390		
19	ThWR(DI)	Data in to $\overline{WR}$ ↑ Hold Time	0		
20	TdRD(DI)	Data Valid from $\overline{RD}$ ↓ Delay			1
21	ThRD(DI)	Data Valid to $\overline{RD}$ ↑ Hold Time	0		
22	TdRD(DI_Z)	Data Bus Float Delay from $\overline{RD}$ ↑		70	
23	TdRD(DB_A)	$\overline{RD}$ ↓ to Read Data Active Delay	0		
24	TdWR(W)	$\overline{WR}$ ↓ to $\overline{WAIT}$ ↓ Delay		150	
25	TdRD(W)	$\overline{RD}$ ↓ to $\overline{WAIT}$ ↓ Delay		150	
26	TdDI(W)	Data Valid to $\overline{WAIT}$ ↑ Delay	0		

NOTES

1. This parameter is dependent on the state of the UPC at the time of master CPU access.
3. The timing characteristics given reference 2.0 V as High and 0.8 V as Low.
4. All output ac parameters use test load 1.

*Timings are preliminary and subject to change.

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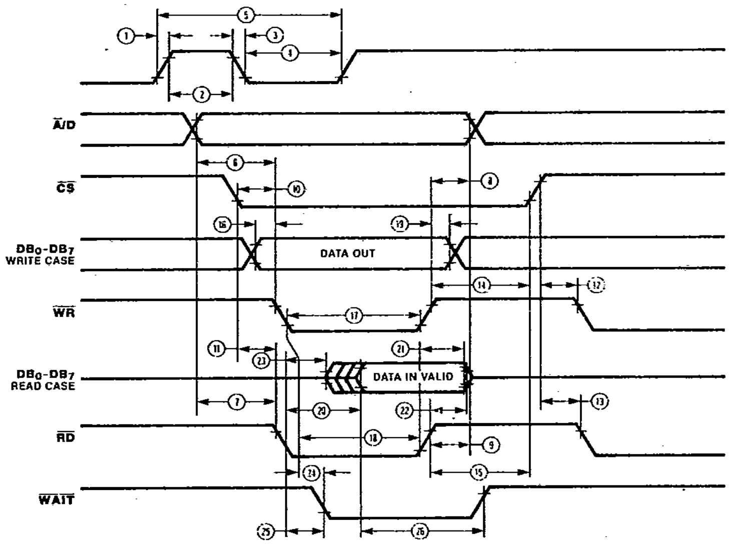
Interrupt Acknowledge Transactions

Number	Symbol	Parameter	Min (ns)	Max (ns)	Notes*
27	TsACK(RD)	$\overline{\text{INTACK}}$ ↓ to $\overline{\text{RD}}$ ↓ Setup Time	90		2
28	TdRD(DI)	$\overline{\text{RD}}$ ↓ to Vector Valid Delay		255	
29	ThRD(ACK)	$\overline{\text{RD}}$ ↑ to $\overline{\text{INTACK}}$ ↑ Hold Time	0		
30	ThIEI(RD)	IEI to $\overline{\text{RD}}$ ↓ Hold Time	100		
~~31~~	~~TwRDl~~	~~$\overline{\text{RD}}$ (Acknowledge) Low Width~~	~~255~~		
32	TdIEI(IEO)	IEI to IEO Delay		120	
33	TsIEI(RD)	IEI to $\overline{\text{RD}}$ ↓ Setup Time	150		
34	$\text{TdACK}_f\text{(IEO)}$	$\overline{\text{INTACK}}$ ↓ to IEO ↓ Delay		250	
35	$\text{TdACK}_r\text{(IEO)}$	$\overline{\text{INTACK}}$ ↑ to IEO ↑ Delay		250	

NOTES:
2. In case where daisy chain is not used.
3. The timing characteristics given reference 2.0 V as High and 0.8 V as Low.
4. All output ac parameters use test load 1.

*Timings are preliminary and subject to change.

Master CPU Interface Timing



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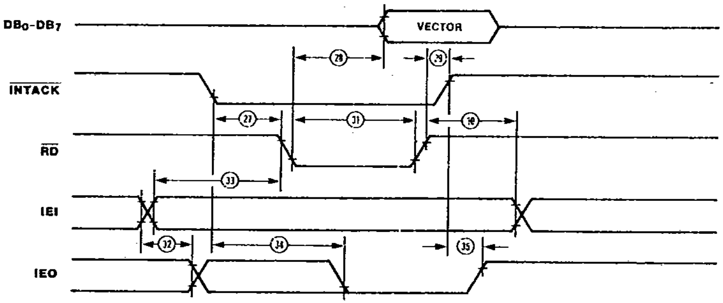
Interrupt Acknowledge Timig



Handshake Timing

Number	Symbol	Parameter	Min (ns)	Max (ns)	Notes*
1	TsDI(DA)	Data In Setup Time	0		
2	ThDA(DI)	Data In Hold Time	230		
3	TwDA	Data Available Width	175		1,2
4	TdDAL(RY)	Data Available Low to Ready Delay Time	20 0	175	1,2 2,3
5	TdDAH(RY)	Data Available High to Ready Delay Time	 0	150	1,2 2,3
6	TdDO(DA)	Data Out to Data Available Delay Time	50		2
7	TdRY(DA)	Ready to Data Available Delay Time	0	205	2

1. Input Handshake.
2. Test Load 1.
3. Output Handshake.

*Timings are preliminary and subject to change.

Reset Timing

Number	Symbol	Parameter	Min (ns)	Max (ns)	Notes*
1	TdRDQ(WR)	Delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↓ for No Reset	40		
2	TdWRQ(RD)	Delay from $\overline{WR}$ ↑ to $\overline{RD}$ ↓ for No Reset	50		
3	TwRES	Minimum Width of $\overline{WR}$ and $\overline{RD}$ both Low for Reset	250		4

4. Internal reset signal is ½ to 2 clock delays from external reset condition.

*Timings are preliminary and subject to change.

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Z8590 UPC

RAM Version Program Memory Timing

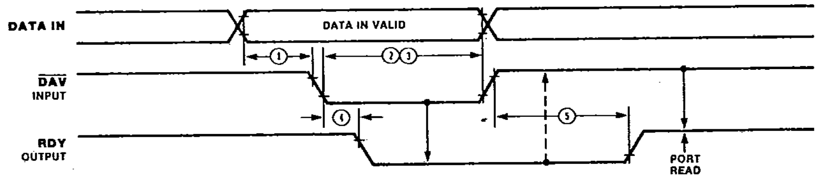
Number	Symbol	Parameter	Min (ns)	Max (ns)	Notes*
1	TwMAS	Memory Address Strobe Width	60		5
2	TdA(MAS)	Address Valid to Memory Address Strobe ↑ Delay	30		5
3	TdMR/W (MAS)	Memory Read/Write to Memory Address Strobe ↑ Delay	30		5
4	TdMDS(A)	Memory Data Strobe ↑ to Address Change Delay	60		
5	TdMDS (MR/W)	Memory Data Strobe ↑ to Memory Read/Write Not Valid Delay	80		
6	Tw(MDS)	Memory Data Strobe Width (Write Case)	160		6
7	TdD0(MDS)	Data Out Valid to Memory Data Strobe ↓ Delay	30		5
8	TdMDS(D0)	Memory Data Strobe ↑ to Data Out Change Delay	30		5
9	Tw(MDS)	Memory Data Strobe Width (Read Case)	230		6
10	TdMDS(DI)	Memory Data Strobe ↓ to Data In Valid Delay		160	7
11	TdMAS(DI)	Memory Address Strobe ↓ to Data In Valid Delay		280	7
12	ThMDS(DI)	Memory Data Strobe ↑ to Data In Hold Time	0		
13	TwSY	Instruction Sync Out Width	160		
14	TdSY(MDS)	Instruction Sync Out to Memory Data Strobe Delay	200		
15	TwI	Interrupt Request via Port 3 Input Width	100		

NOTES:

5. Delay times are specified for an input clock frequency of 4 MHz. When operating at a lower frequency, the increase in input clock period must be added to the specified delay time.
6. Data strobe width is specified for an input clock frequency of 4 MHz. When operating at a lower frequency, the increase in three input clock periods must be added to the specified width. Data strobe width varies according to the instruction being executed.
7. Address strobe and data strobe to data in valid delay times represent memory system access times and are given for a 4 MHz input frequency.
8. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0."
9. All output ac parameters use test load 2.

*Timings are preliminary and subject to change.

Handshake Timing



Input Handshake

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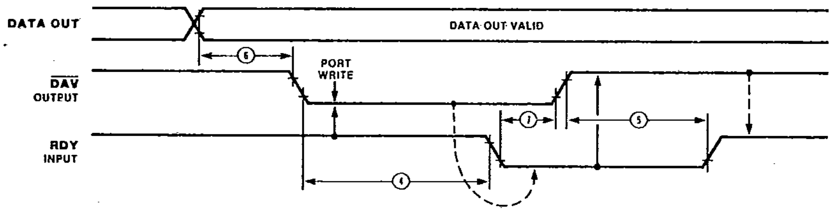
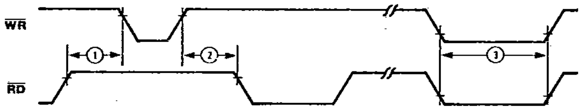
Handshake Timing (Continued)

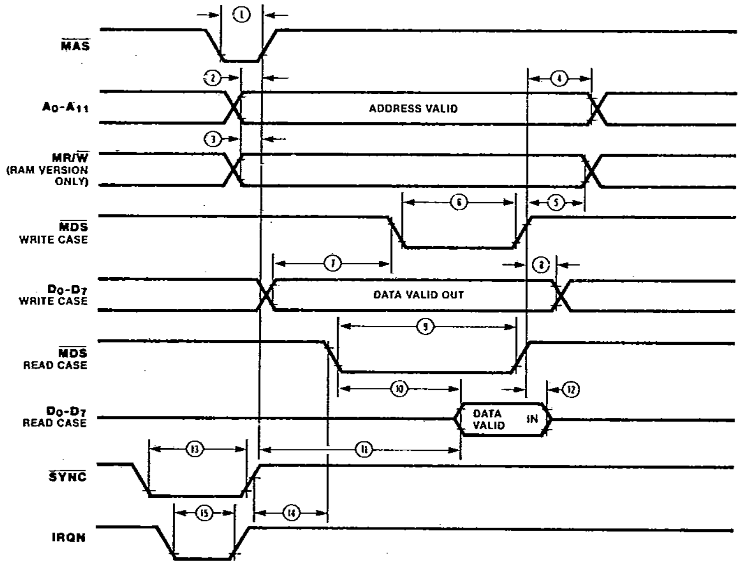


Output Handshake

Reset Timing



RAM Version Program Memory Timing



Ordering Information

Type	Package	Temp	Clock	Description
Z8590 B1	Plastic 40 pin	0/+70°C	4MHz	Z8590 Universal Peripheral
B6	Plastic 40 pin	-40/+85°C		Controller
D1	Ceramic 40 pin	0/+70°C		
D2	Ceramic 40 pin	-55/+125°C		
D6	Ceramic 40 pin	-40/+85°C		
Z8590A B1	Plastic 40 pin	0/+70°C	6MHz	
B6	Plastic 40 pin	-40/+85°C		
D1	Ceramic 40 pin	0/+70°C		
D6	Ceramic 40 pin	-40/+85°C		
Z8591 Q1	QUIP 64	0/+70°C	4MHz	External ROM
Z8591A Q1	QUIP 64	0/+70°C	6MHz	UPC
Z8592 Q1	QUIP 64	0/+70°C	4MHz	External RAM
Z8592A Q1	QUIP 64	0/+70°C	6MHz	UPC
Z8593 R1	PDP	0/+70°C	4MHz	Piggyback EPROM
Z8593A R1	PDP	0/+70°C	6MHz	UPC
Z8594 R1	PDP	0/+70°C	4MHz	Piggyback EPROM
Z8594A R1	PDP	0/+70°C	6MHz	UPC

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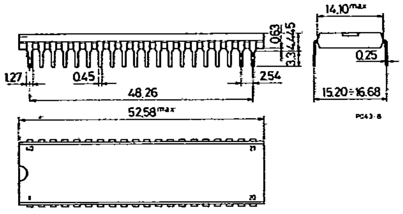
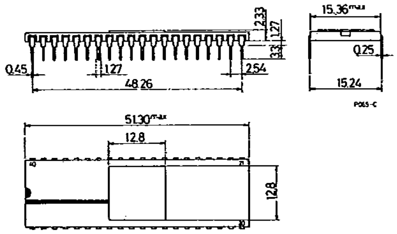
Packages

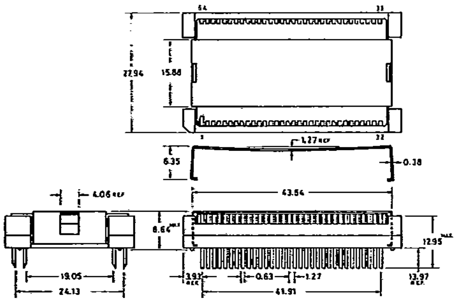
Plastic



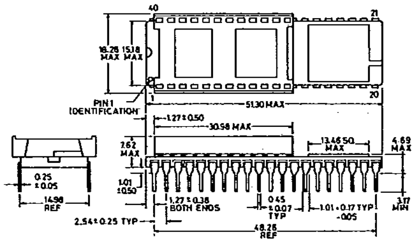
Ceramic



Quip 64



PDP



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