

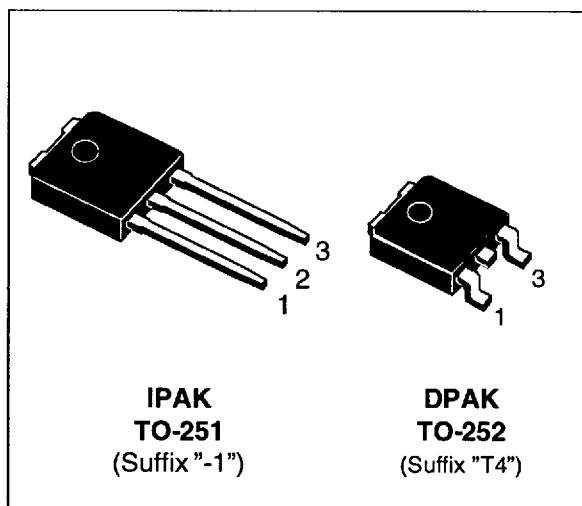
N - CHANNEL ENHANCEMENT MODE "ULTRA HIGH DENSITY" POWER MOS TRANSISTOR

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD20N06	60 V	< 0.03 Ω	20 A (*)

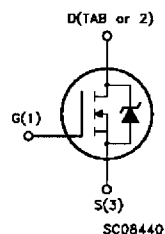
- TYPICAL R_{DS(on)} = 0.026 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- HIGH dV/dt RUGGEDNESS
- APPLICATION ORIENTED CHARACTERIZATION
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- POWER MOTOR CONTROL
- DC-DC & DC-AC CONVERTERS
- SYNCHRONOUS RECTIFICATION



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	60	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 k Ω)	60	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	20	A
I _D	Drain Current (continuous) at T _c = 100 °C	14	A
I _{DM} (*)	Drain Current (pulsed)	80	A
P _{tot}	Total Dissipation at T _c = 25 °C	60	W
	Derating Factor	0.4	W/°C
dV/dt(1)	Peak Diode Recovery voltage slope	7	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(*) Pulse width limited by safe operating area

STD20N06

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	2.5	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	100	$^{\circ}C/W$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	1.5	$^{\circ}C/W$
T_l	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}C$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	20	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}C$, $I_D = I_{AR}$, $V_{DD} = 25 V$)	80	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	20	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100^{\circ}C$, pulse width limited by T_j max, $\delta < 1\%$)	14	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	60			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^{\circ}C$			250 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$ $I_D = 10 A$ $V_{GS} = 10V$ $I_D = 10 A$ $T_c = 100^{\circ}C$		0.026	0.03 0.06	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	20			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 10 A$	11	16		S
C_{iss}	Input Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		2000	2800	pF
C_{oss}	Output Capacitance			350	450	pF
C_{rss}	Reverse Transfer Capacitance			80	120	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	$V_{DD} = 30\text{ V}$ $I_D = 10\text{ A}$ $R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		45 280	65 380	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 48\text{ V}$ $I_D = 20\text{ A}$ $R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		240		A/ μ s
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 40\text{ V}$ $I_D = 20\text{ A}$ $V_{GS} = 10\text{ V}$		60 10 20	80	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 48\text{ V}$ $I_D = 38\text{ A}$ $R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		55 125 200	75 170 270	ns ns ns

SOURCE DRAIN DIODE

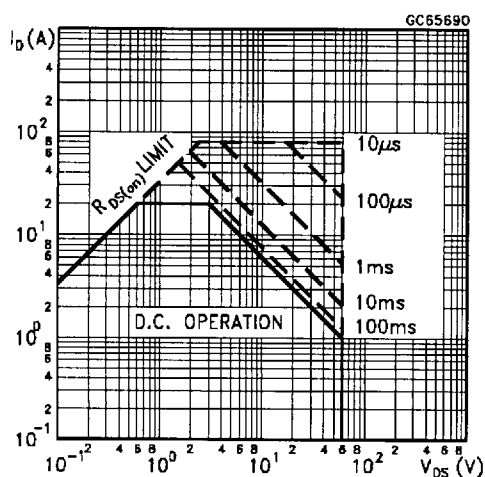
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				9 36	A A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 20\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		80 0.3 7		ns μC A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

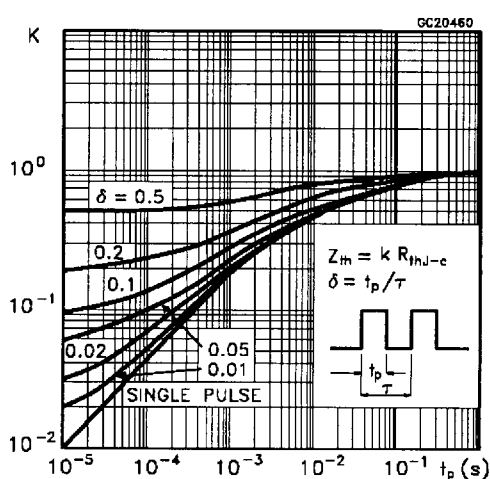
(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 20\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

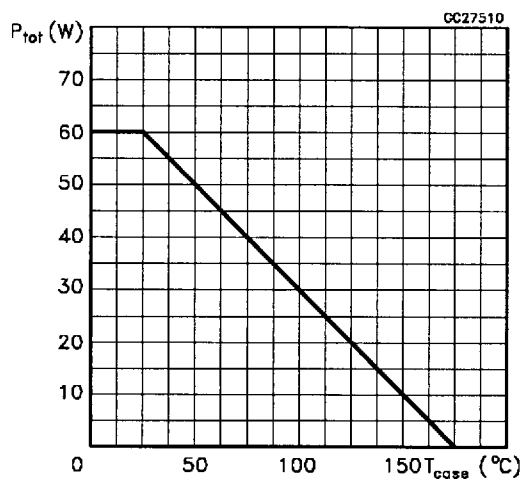
Safe Operating Area



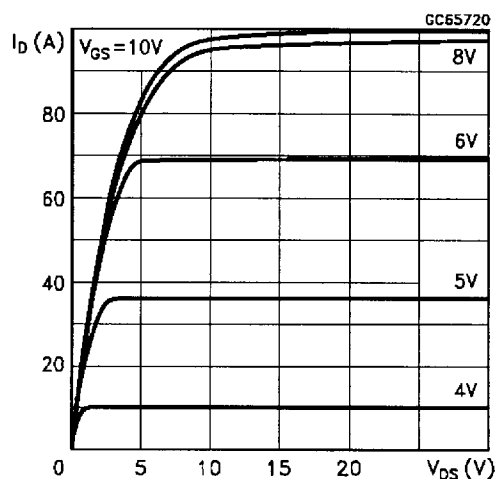
Thermal Impedance



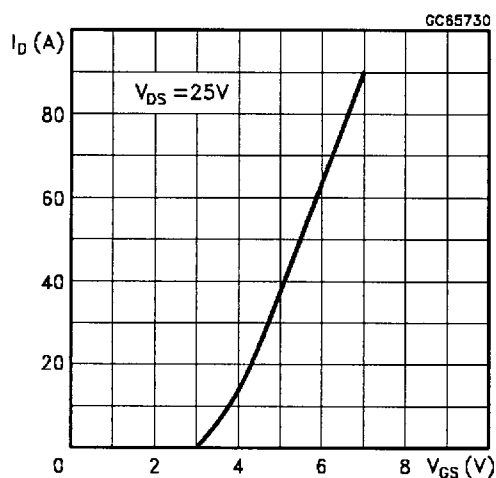
Derating Curve



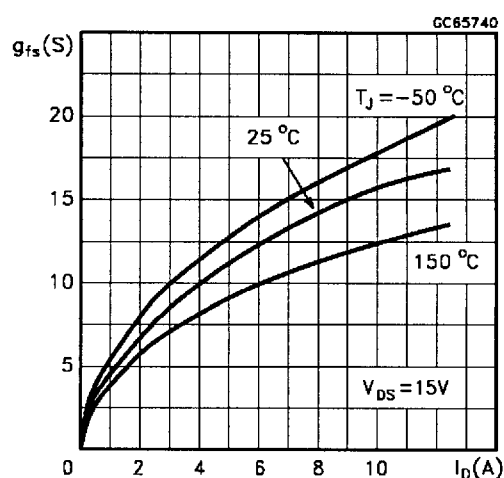
Output Characteristics



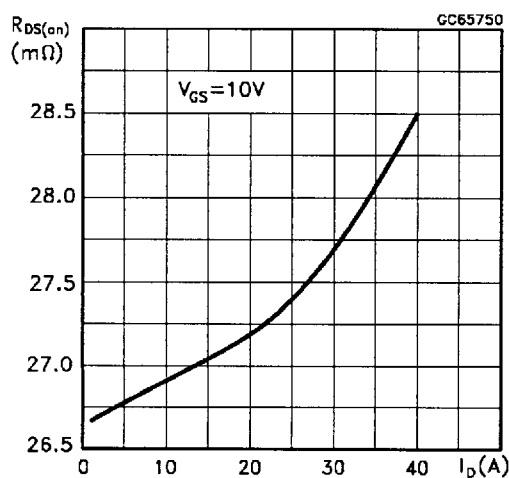
Transfer Characteristics



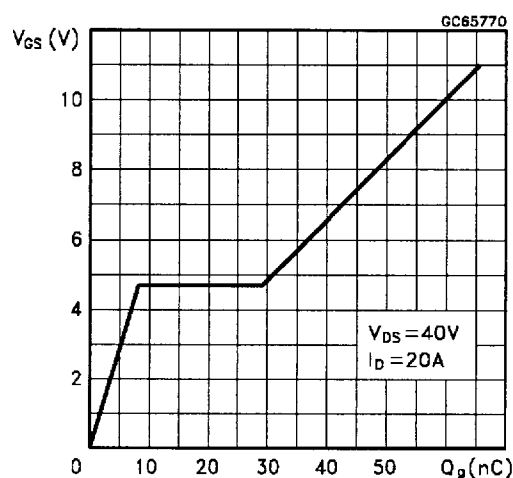
Transconductance



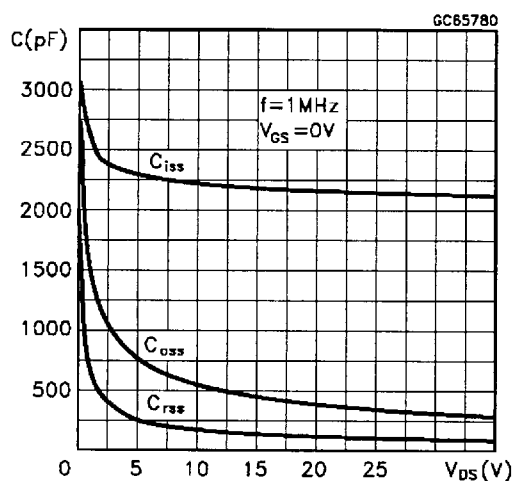
Static Drain-source On Resistance



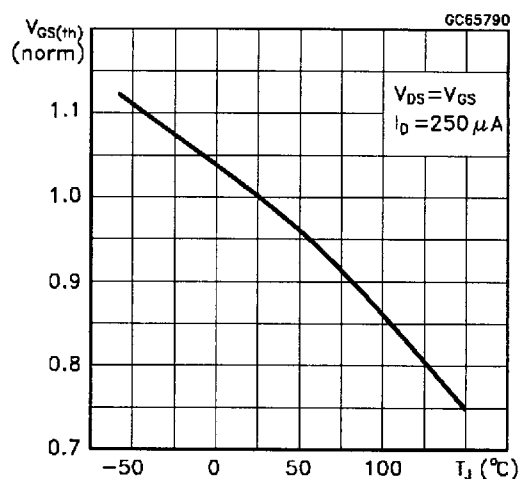
Gate Charge vs Gate-source Voltage



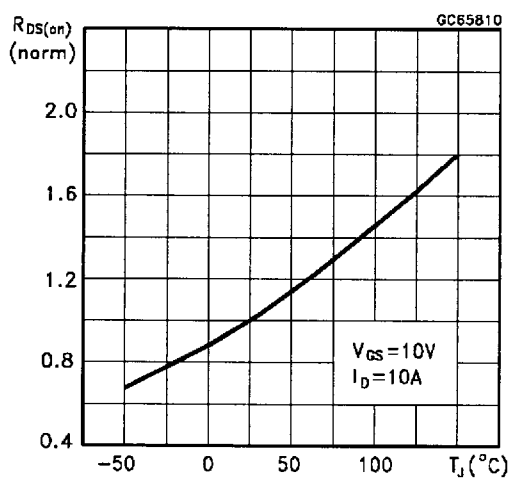
Capacitance Variations



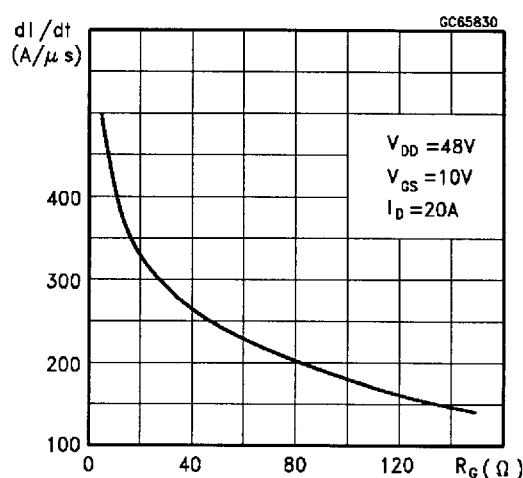
Normalized Gate Threshold Voltage vs Temperature



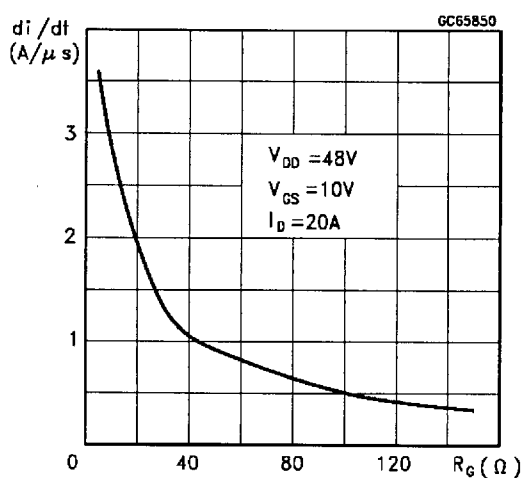
Normalized On Resistance vs Temperature



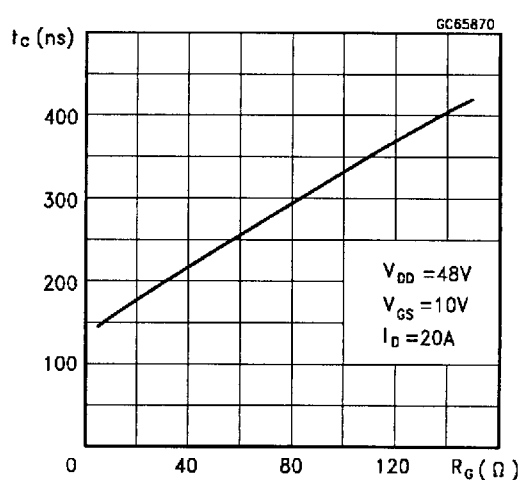
Turn-on Current Slope



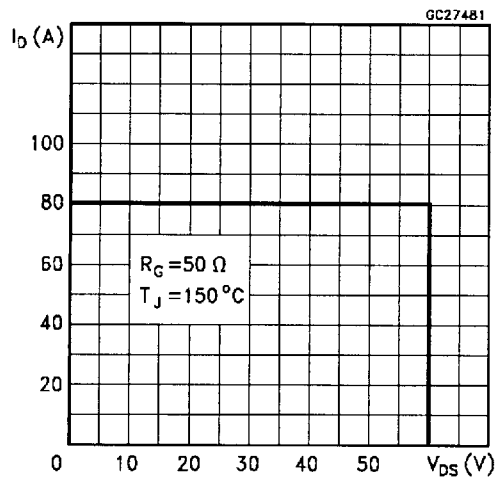
Turn-off Drain-source Voltage Slope



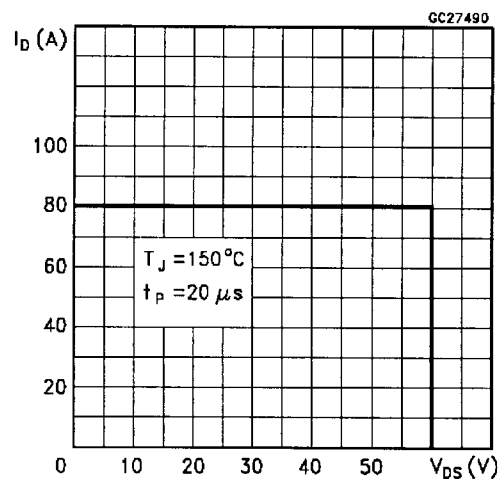
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

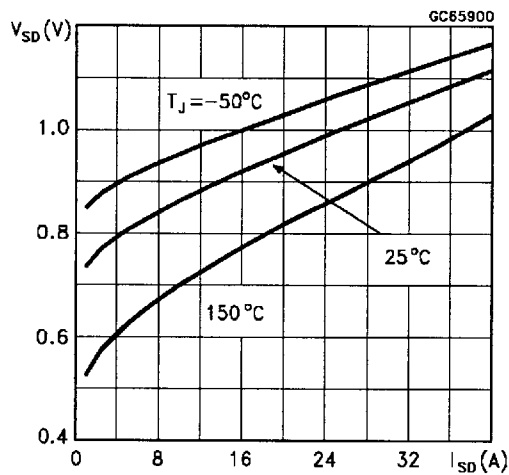


Fig. 1: Unclamped Inductive Load Test Circuit

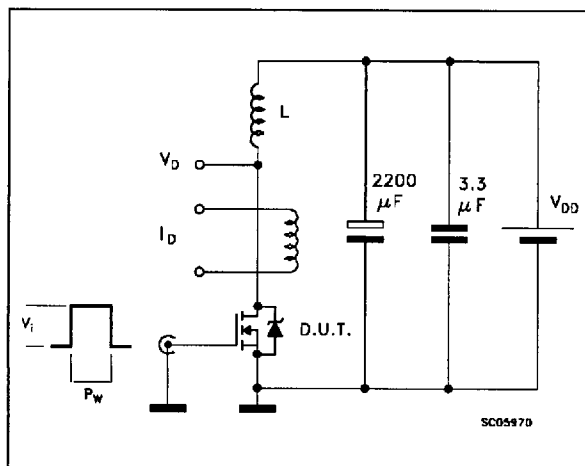


Fig. 2: Unclamped Inductive Waveform

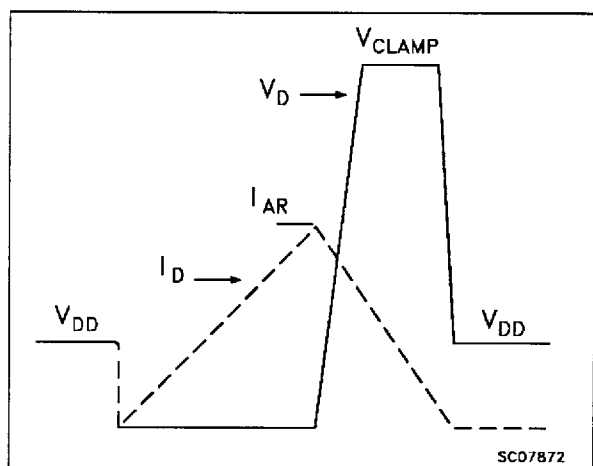


Fig. 3: Switching Times Test Circuits For Resistive Load

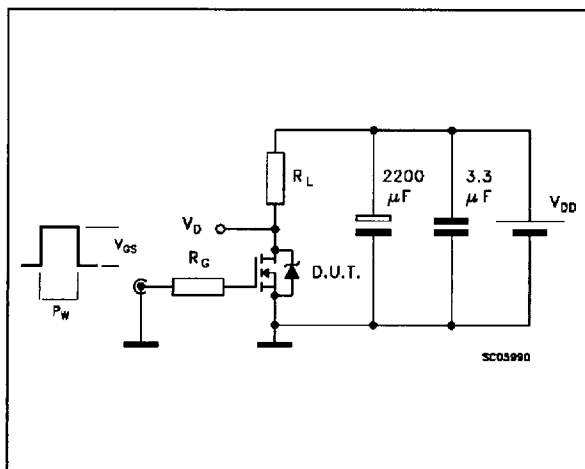


Fig. 4: Gate Charge test Circuit

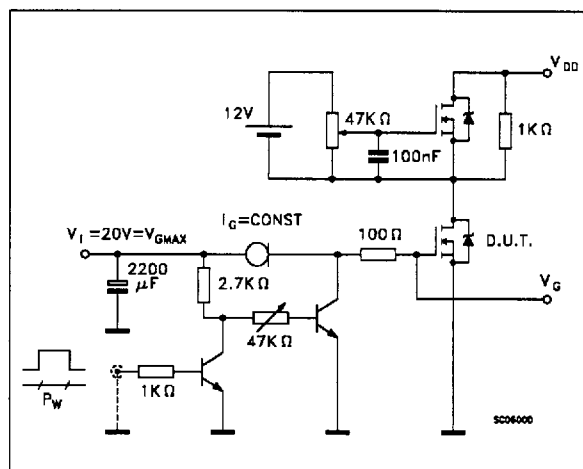
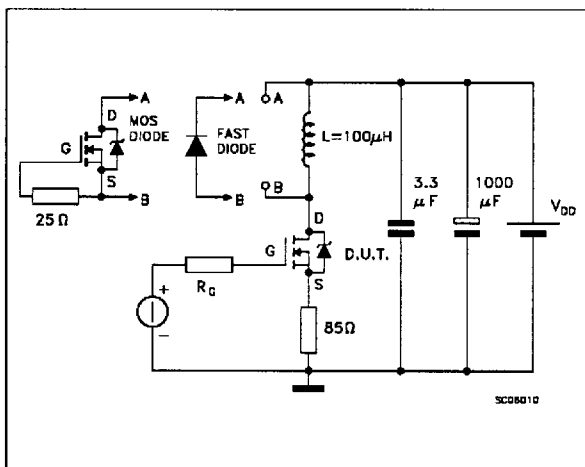


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



STD20N06

PSPICE PARAMETERS SUBCIRCUIT COMPONENTS

Symbol	Parameter	Value	Unit
S1	(V14_16<0) (See Power Mosfet Model Subcircuit)	ON	
S2	(V16_11<0) (See Power Mosfet Model Subcircuit)	ON	
LD	Drain Inductance	8	nH
LG	Gate Inductance	10	nH
LS	Source Inductance	10	nH
RDRAIN	Drain Resistance	$1.9E^{-2}$	Ω
RGATE	Gate Resistance	1	Ω
CGD	Gate Drain Capacitance	3.92	nF
CGS	Gate Source Capacitance	1.9	nF
ALFA	Drift Coefficient	$1E^{-3}$	V^{-1}
RGN	Negative Bias Resistance	10	K Ω

DIODE DRAIN GATE (Depletion Capacitance)

Symbol	Parameter	Value	Unit
CJO	Zero Bias p-n Capacitance	2.6	nF
VJ	p-n Potential	0.1	V
M	p-n Grading Coefficient	0.6	

DIODE DRAIN SOURCE

Symbol	Parameter	Value	Unit
CJO	Zero Bias p-n Capacitance	7.8	nF
VJ	p-n Potential	0.1	V
M	p-n Grading Coefficient	0.6	
TT	Transit Time	20	nsec

N MOSFET

Symbol	Parameter	Value	Unit
L	Channel Length	1	μ Meter
W	Channel Width	1	μ Meter
LEVEL	Model Index	3	
TOX	Oxide Thickness	1	Meter
VTO	Zero Bias Threshold Voltage	3.25	V
U0	Surface Mobility	600	cm^2/Vs
THETA	Mobility Modulation	0.005	V^{-1}
Vmax	Maximum Drift Velocity	0	Meter/sec
KP	Trans Conductance Coefficient	28	Amp/ V^2

For Transient Simulation Applicate U.I.C. (Use Initial Condition) Option

PSPICE NETLIST OF THE SUBCIRCUIT

```
.SUBCKT STD20N06 1 2 3
*VALUE OF THE PACKAGE INDUCTANCES
LS 1 11 10n
LG 2 12 10n
LD 3 13 7n
```

*RESISTANCE OF THE GATE
POLYSILICON
RG 12 16 1

*EPY AND DRIFT RESISTANCES
RD 13 14 1.9e-02
EDRI 14 15 POLY(2) (13 14) (13 11) 0 0 0 0
1e-3

*CAPACITANCE GATE SOURCE
CGS 16 11 1.90n

*OPTIONAL FOR NEGATIVE GATE BIAS
*S2 51 11 11 16 SWITCH
*CGN 51 16 3.92n
*RGN 51 16 10k

*MILLER CAPACITANCE
CGD 16 17 3.92n

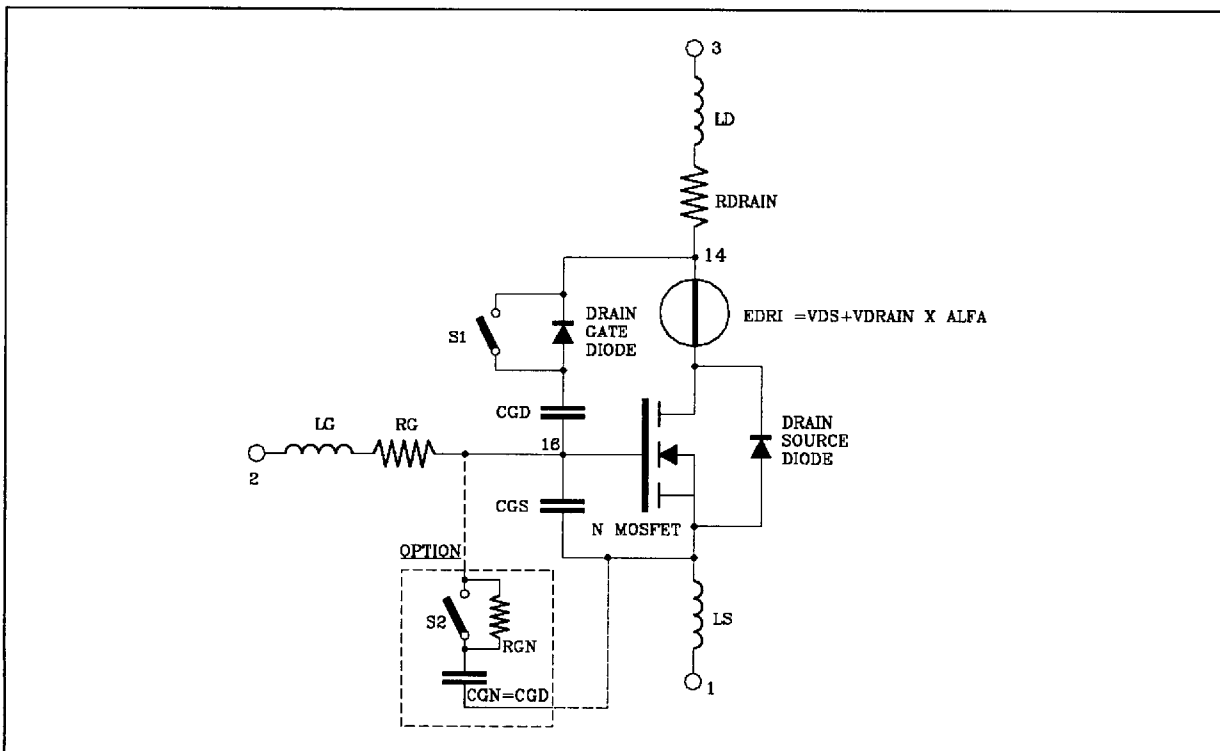
```
* DEPLETION CAPACITANCE
DGD 17 14 DGD
S1 17 14 16 14 SWITCH
.MODEL DGD D +IS=
+CJO=2.6n
+Vj=.1
+M=.6
```

```
.MODEL SWITCH VSWITCH
+RON=1m
+ROFF=1MEG
+VON=0.1
```

```
* OUTPUT CAPACITANCE AND BODY DRAIN DIODE
DBD 11 14 DBD
.MODEL DBD D
+TT=20n
+CJO=7.8n
+VJ=.1
+M=.6
```

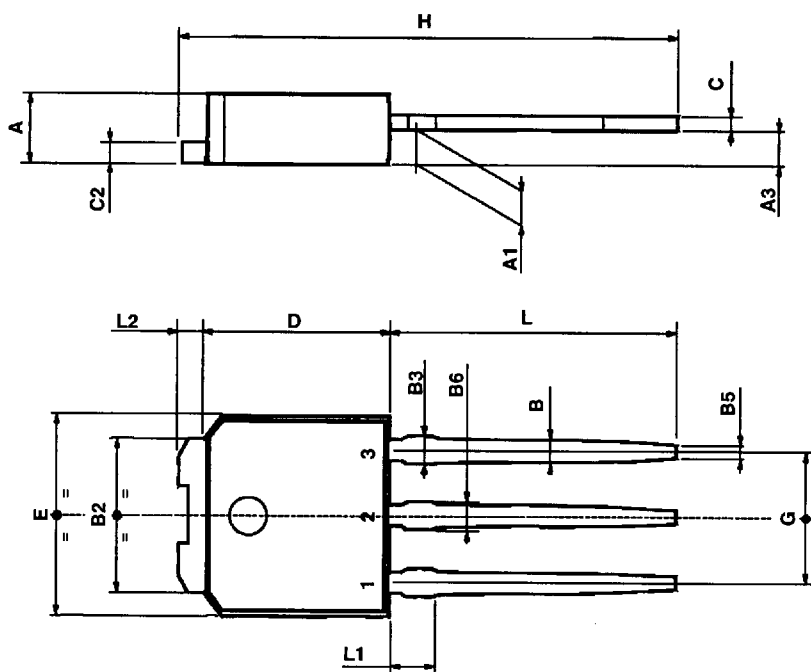
```
* MODEL OF THE MOSFET
MMAIN 15 16 11 11 MMAIN L=1u W=1u
.MODEL MMAIN NMOS
+LEVEL=3
+TOX=1
+VTO=3.25
+uo=600
+THETA=0.005
+VMAX=5e7
+KP=28
.ENDS
```

Power Mosfet Model Subcircuit



TO-251 (IPAK) MECHANICAL DATA

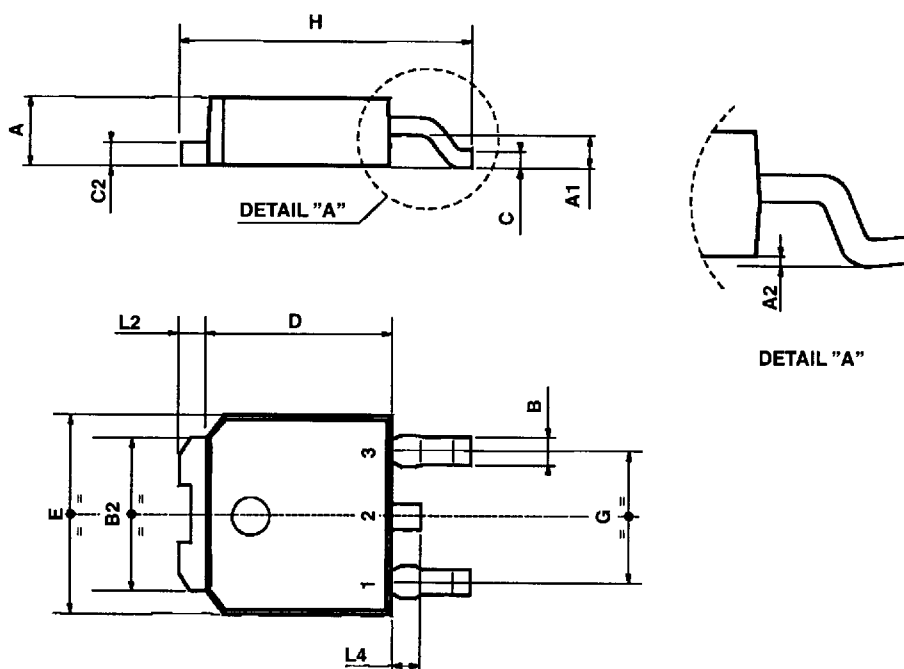
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



0068771-E

TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



0068772-B