

Z86217

CMOS Z8® 8-BIT MICROCONTROLLER FOR MOUSE AND TRACKBALL APPLICATIONS

FEATURES

Z8 Core

- 18-Pin DIP and SOIC Package
- 144 Bytes On-Chip RAM
- 2 Kbytes On-Chip Masked ROM
- 42 Fundamental Instructions

On-Chip Features

- Dedicated Ports for Opto-Transistor Output With CMOS Levels; Schmitt-Triggered
- High Drive Ports ($V_{OL} = 0.8$, $I_{OL} = 10$ mA, 6 Pins Max) With Internal 100K and 20K Pull-Up Resistors
- Oscillator Filter
- Hardwired Watch-Dog Timer

- Six Vectored Priority Interrupts
- 14 Input/Output Lines
- On-Chip Oscillator (Crystal, Ceramic Resonator, LC, or External Clock Drive)

Performance

- Up to 4 MHz Operation
- Low Power Consumption; 33 mW (Typical) With Two Standby Modes: STOP and HALT
- 250 ns Cycle Time
- ESD Protection Circuitry

GENERAL DESCRIPTION

The Z86217 is a member of the Z8® family of microcontrollers and offers easy software/hardware development tools. The proven reliability of the process and instruction set benefits the needs of the high-volume Mouse market. The device is housed in an 18-pin DIP or SOIC package and is manufactured in CMOS technology.

The Z86217 provides on-board pull-up resistors, a scalable trip-point buffer for accommodation of opto-transistor outputs, and high drive ports capable of up to 10 mA current sinking per pin (6 pins maximum). The permanently enabled Watch-Dog Timer (WDT) provides added operational reliability in the various environments the Mouse is used.

There are two basic address spaces available to support this wide range of configurations, Program Memory, and 124 bytes of general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and I/O data communications, the Z86217 offers two on-chip counter/timers with a large number of user selectable modes.

MASK OPTIONS

The Z86217 provides High Drive Ports ($I_{OL}=10$ mA at $V_{OL} = 0.8V$, 36 pins max), Permanently Enabled Watch-Dog Timer, and Oscillator Filter. The Watch-Dog Timer operates upon power-up of the MCU. The oscillator filter assists in filtering out high-frequency noise from the oscillator input pin. The high-drive ports provide extra sinking current capability.

Notes:

Refer to the DC electrical characteristics for detailed specification of the sinking current.

All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

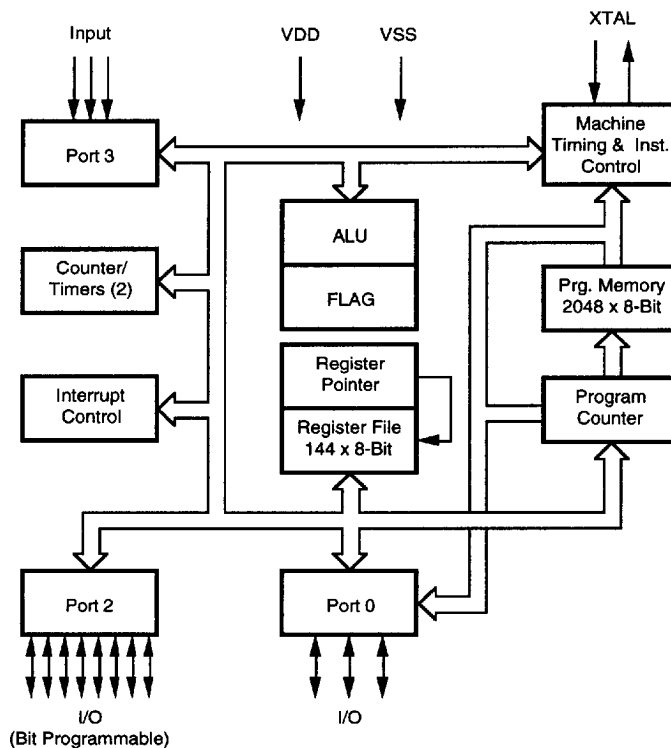


Figure 1. Functional Block Diagram

PIN DESCRIPTIONS

This Section describes the pin numbers and respective signals plus their functions (Figures 2 and 3, Tables 2 and 3).

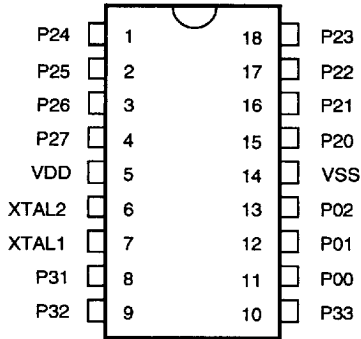


Figure 2. 18-Pin DIP and SOIC Pin Configuration

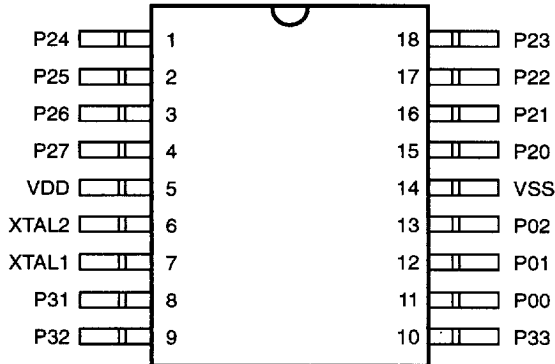


Figure 3. 18-Pin SOIC Pin Configuration

Table 2. 18-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4,5,6,7	In/Output
5	V _{DD}	Power Supply	Input
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1	Input
9	P32	Port 3, Pin 2	Input
10	P33	Port 3, Pin 3,	Input
11-13	P00-P02	Port 0, Pins 0,1,2	In/Output
14	V _{SS}	Ground	Input
15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output

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9	P32	Port 3, Pin 2	Input
10	P33	Port 3, Pin 3,	Input
11-13	P00-P02	Port 0, Pins 0,1,2	In/Output
14	V _{SS}	Ground	Input
15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output

PIN FUNCTIONS

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (4 MHz max) to the on-chip clock oscillator and buffer.

Port 0 (P02-P00). Port 0 is a 3-bit I/O, programmable, bi-directional, CMOS compatible I/O port. These three I/O lines can be configured under software control to be an input or output (Figure 4). When Port 0 is configured as an input port, all lines have a 100 Kohm (typical) internal pull-up resistor (see Figures 39 resistance variation).

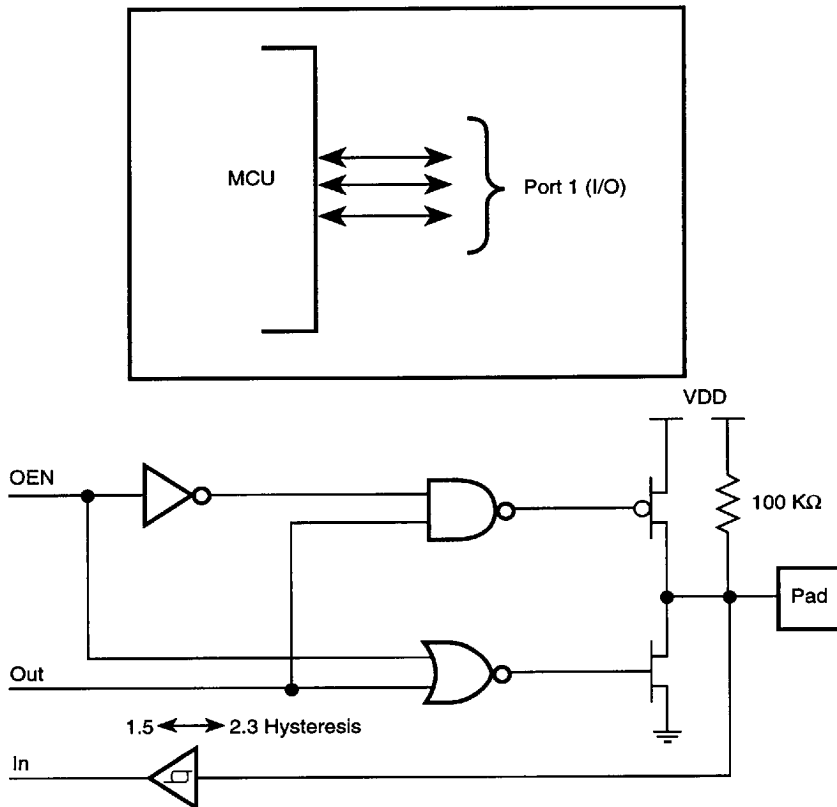


Figure 4. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit programmable, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as out-

puts may be globally programmed as either push-pull or open-drain (Figure 5). P23-20 input lines have 100 Kohm (typical) pull-up resistors. These resistors are not applied in push-pull mode (see Figure 39 for resistance variation).

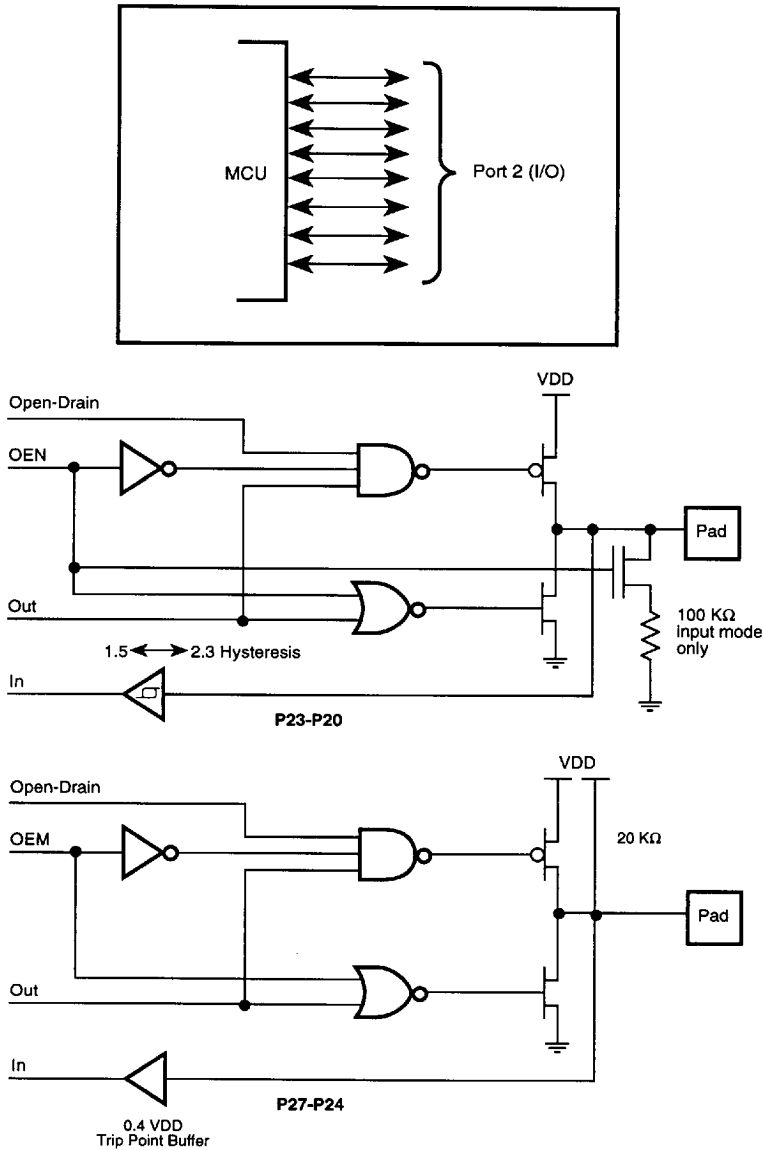


Figure 5. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P32) lines. These three input lines can also be used as the interrupt sources IRQ3-IRQ0

and as the timer input signal (T_{IN}). P31 and P33 provide $\approx 100\text{ Kohm}$ (typical) internal pull-up resistor (see Figure 39 for resistance variation and Figure 6 for Port 3 configuration).

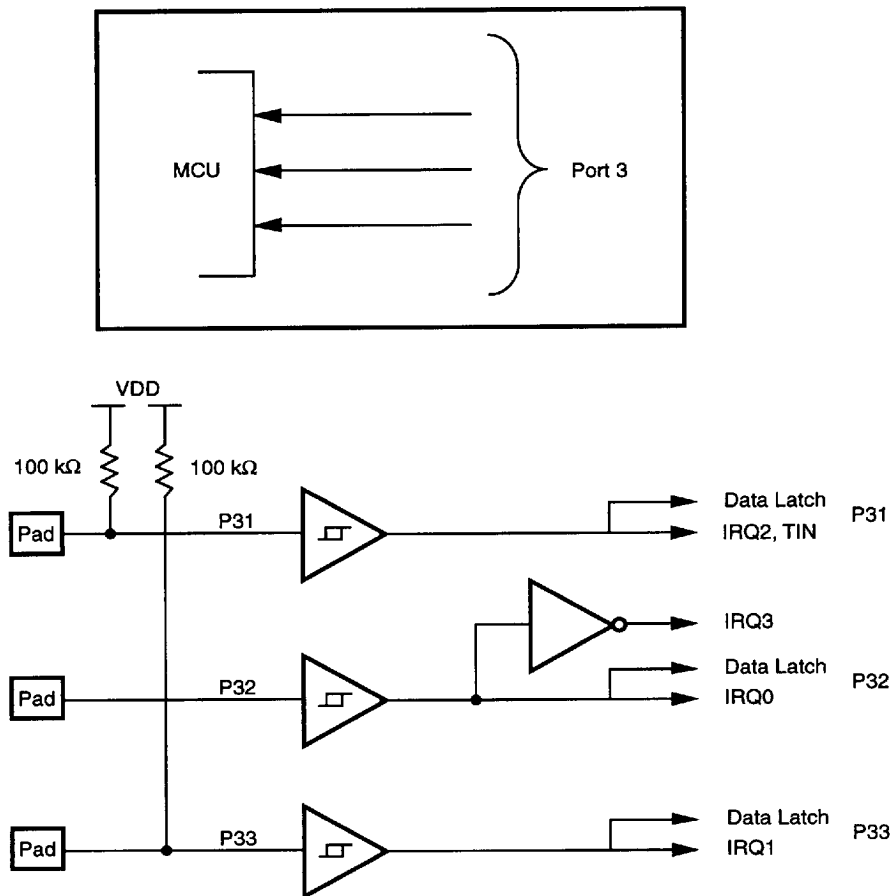


Figure 6. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z8 MCU incorporates special functions to enhance the Z8's application in mice, trackballs, and other consumer applications.

Reset. Upon power up, the Power-On Reset circuit waits for 5.0 ms plus 18 crystal clocks and then starts program execution at address 000CH (Figure 7). Reference the Z86217 control registers' Reset value (Table 4).

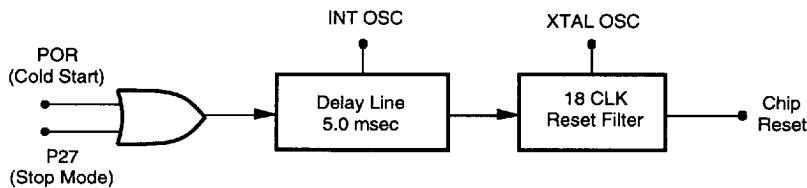


Figure 7. Internal Reset Configuration

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Table 4. Z86217 Control Registers

Addr.	Reg.	Reset Condition								Comments
		D7	D6	D5	D4	D3	D2	D1	D0	
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	1	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
FB	IMR	0	U	U	U	U	U	U	U	
FC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	U	U	U	U	U	U	U	U	
FF	SPL	U	U	U	U	U	U	U	U	

Note:

* A reset after a Low on P27 to get out of STOP mode may affect device reliability.

Program Memory. The Z86217 can address up to 2 Kbytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2048 are on-chip mask-programmed ROM.

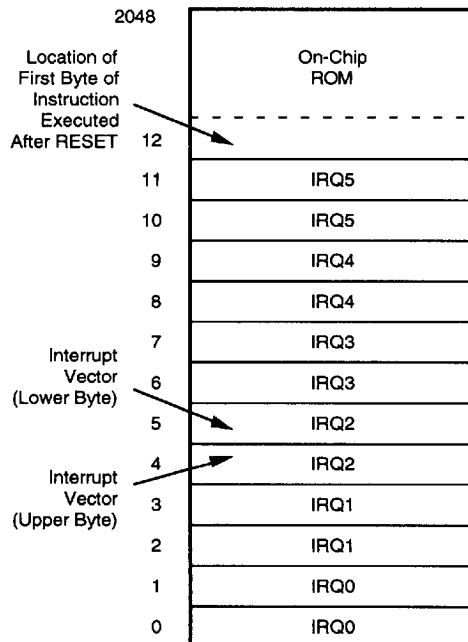


Figure 8. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 15 control and status registers (R0-R3, R4-R127 and R241-R255, respectively - Figure 9). The Z86217 instructions can access registers directly or indirectly via an 8-bit address field. This allows short 4-bit register addressing using the

Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 10) addresses the starting location of the active working-register group.

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	General-Purpose	GPR
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Not Implemented	
R128 R127	General-Purpose Registers	
R4	Port 3	P3
R3	Port 2	P2
R2	Reserved	
R1	Reserved	
R0	Port 0	P0

Figure 9. Register File

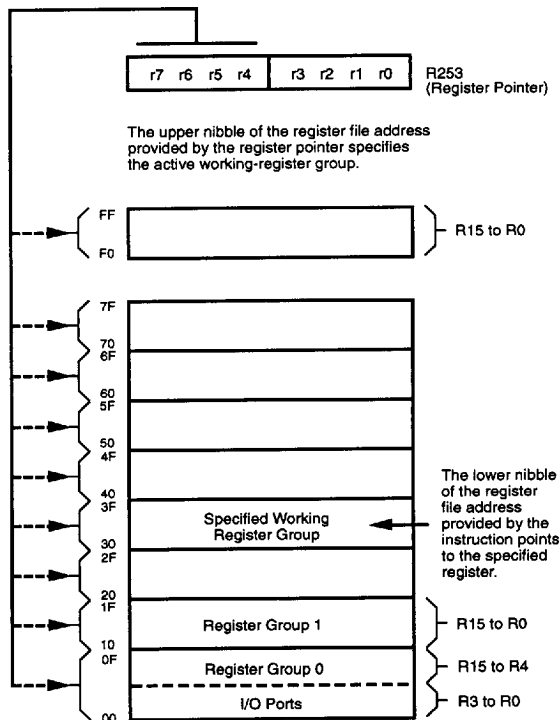


Figure 10. Register Pointer

Stack Pointer. The Z86217 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 11).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggeable or not retriggeable, or as a gate input for the internal clock.

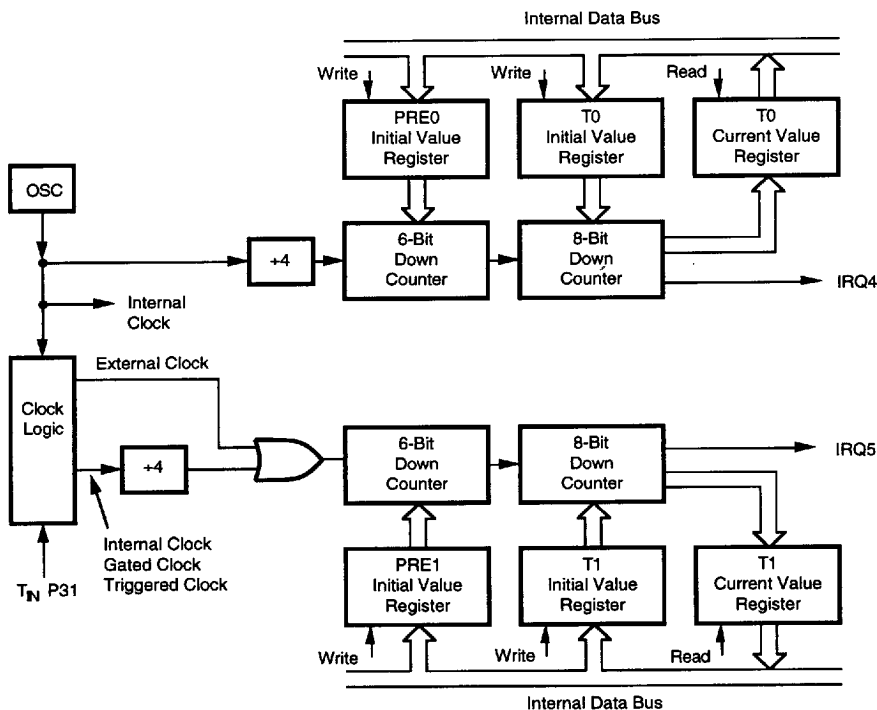


Figure 11. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86217 has six interrupts from five different sources. These interrupts are maskable and prioritized (Figure 12). The five sources are divided as follows: the falling edge of P31, P33, the rising and falling edge of P32, and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 5).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86217 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the Interrupt Service Routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests needs service.

Table 4. Interrupt Types, Sources, and Vectors

Source	Name	Vector	Location	Comments
P32	IRQ0	0,1	External	(F)Edge
P33	IRQ1	2,3	External	(F)Edge
P31	IRQ2	4,5	External	(F)Edge
P32	IRQ3	6,7	External	(R)Edge
T0	IRQ4	8,9	Internal	
T1	IRQ5	10,11	Internal	

Notes:

F = Falling edge triggered

R = Rising edge triggered

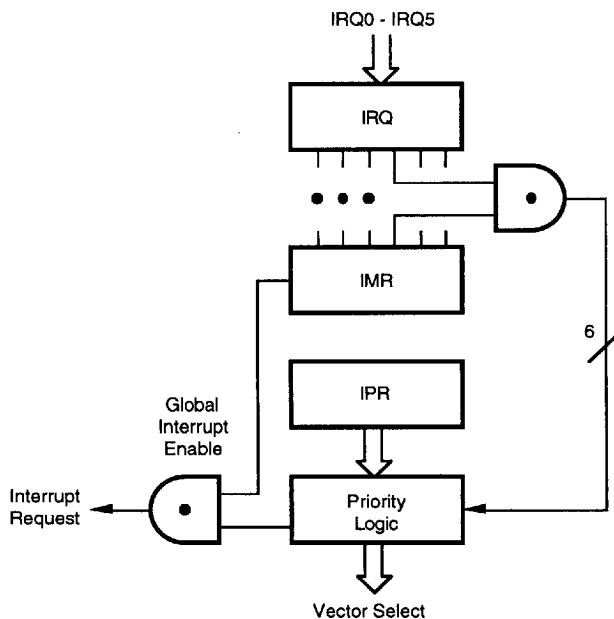


Figure 12. Interrupt Block Diagram

Clock. The Z86217 on-chip oscillator has a parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 4 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance is between 10 pF to 250 pF and is specified by the crystal manufacturer, ceramic resonator and PCB layout) from each pin to ground (Figure 13).

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. The program execution begins at location 000CH. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 120 μ A (typical—WDT running). The STOP mode can be released by two methods. The first method is a RESET of the device by removing V_{DD} . The second method is if P27 is configured as an input line when the device executes the STOP instruction. A low input condition on P27 releases the STOP mode.

Program execution under both conditions begins at location 000C (HEX). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as an output when the STOP

instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
OR
NOP    P2M, #80H
STOP
```

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction. i.e.:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter the STOP mode
      or
FF    NOP    ; clear the pipeline
7F    HALT   ; enter the HALT mode
```

In STOP or HALT mode, the value of each output line prior to the HALT or STOP instruction is retained during execution.

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled upon power-up of the MCU. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

Opcode WDT (5FH). Execution of WDT clears the WDT counter. This has to be done at least every 10 ms. Otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of 5.0 ms +18 XTAL clock cycles.

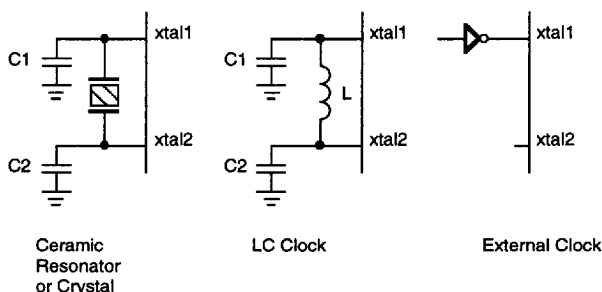


Figure 13. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Brown-Out Protection (V_{BO}). The brown-out trip voltage (V_{BO}) is less than 3V and operates to the following conditions:

Maximum (V_{BO}) Conditions:

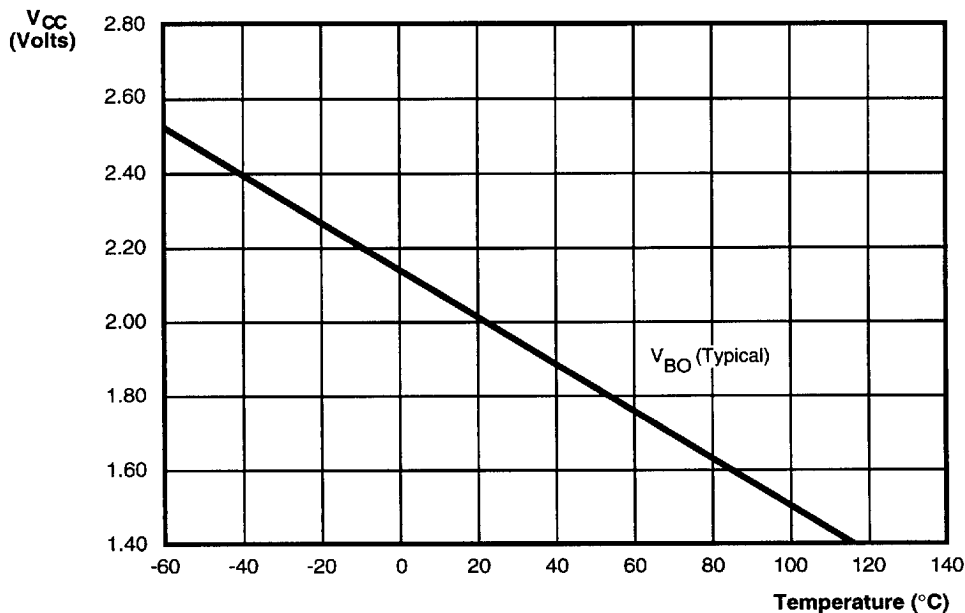
Case 1: $T_A = -40^{\circ}\text{C}$, $+105^{\circ}\text{C}$, Internal Clock Frequency equal or less than 1 MHz

Case 2: $T_A = -40^{\circ}\text{C}$, $+85^{\circ}\text{C}$, Internal Clock Frequency equal or less than 2 MHz

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the brown-out protection trip point (V_{BO}) is reached. The device is guaranteed to function normally at supply voltages above the brown-out trip point for the temperatures and operating frequencies in Case 1 and Case 2 above. The actual brown-out trip point is a function of temperature and process parameters (Figure 14).

2 MHz (Typical)

Temp	-40°C	0°C	$+25^{\circ}\text{C}$	$+70^{\circ}\text{C}$	$+105^{\circ}\text{C}$
V_{BO}	2.55	2.4	2.1	1.7	1.6



* Power-on Reset threshold for V_{CC} and 4 MHz V_{BO} overlap

Figure 13. Typical Z86217 V_{BO} vs Temperature

EMI CHARACTERISTICS

The Z86217 operates in a low EMI emission mode (Figure 15). The measurements were made while operating the

Z86217 in three states: (1) Idle condition; (2) static output; (3) switched output.

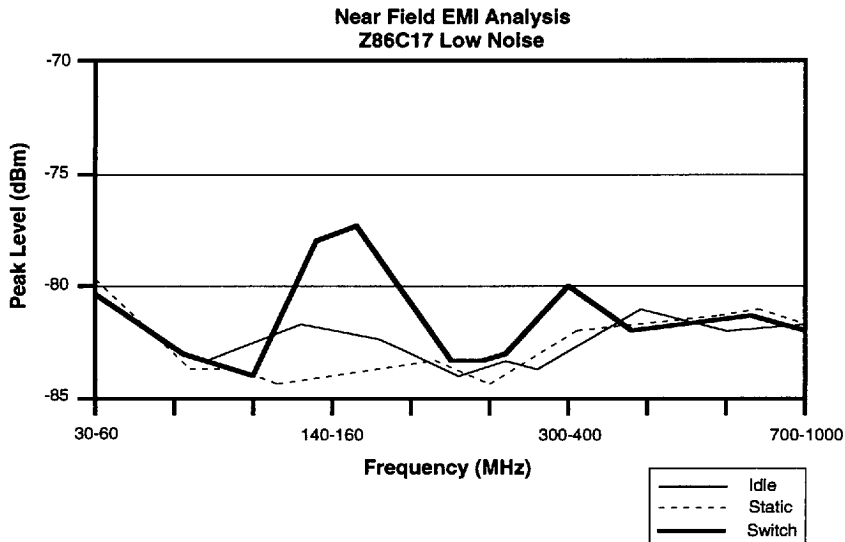


Figure 15. Near Field EMI Analysis

EMI CHARACTERISTICS (Continued)

Internal Pull-Up and Pull-Down Resistances. The Pull-up Resistance is achieved through a Voltage Dependent Resistance configuration. The characteristics are shown in Figure 39.

One Trip Point. The One Trip Point is implemented for use in mouse applications. The One Trip Point consists of a CMOS device configured to activate high at 0.4 V_{DD}. This

provides a convenient method for triggering the input ports for the photo-transistors in mouse applications.

Mouse Application. A typical mouse application circuit diagram is shown in Figure 16. The photo-transistors tie directly into the port lines of the Z86217 and the microcontroller receives its power, ground and transmission capability from a standard RS232 line.

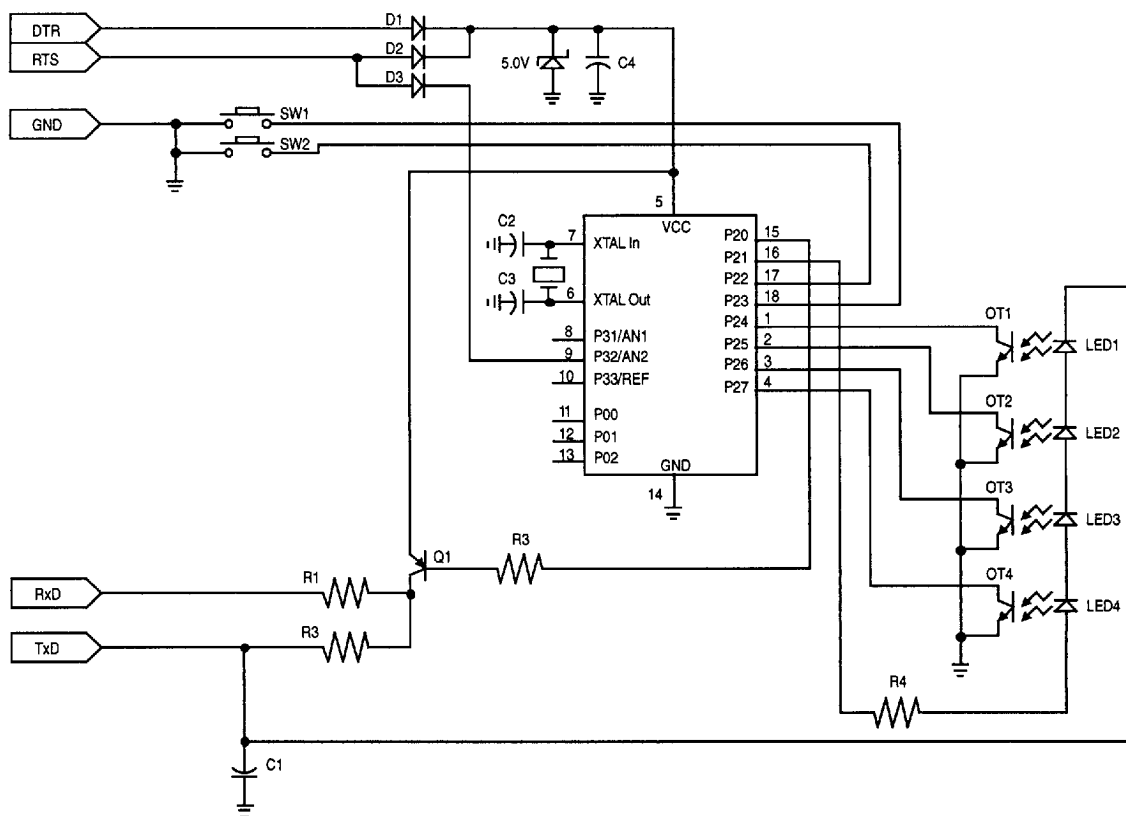


Figure 16. Circuit Diagram Of Z86217 Two Button Mouse Application

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 17).

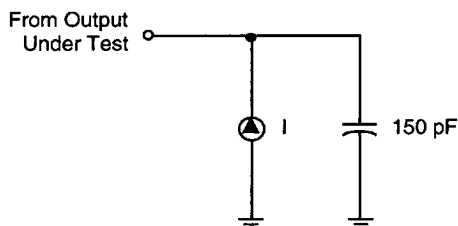


Figure 17. Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Sym	Parameter	Min	Max	Units
V_{DD}	Supply Voltage*	-0.3	+7	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp	†	†	C

Notes:

* Voltages on all pins with respect to GND

† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

$T_A = GND = 0V$, $f = 1.0$ MHz, unmeasured pins to GND

Parameter	Max
Input capacitance	10 pF
Output capacitance	20 pF
I/O capacitance	25 pF

V_{CC} SPECIFICATION

$V_{CC} = 3.0V$ to $5.5V$

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{DD}	T _A = 0°C to +70°C		Typical @ 25°C	Units	Conditions
			Min	Max			
	Max Input Voltage	3.0V		12		V	V _{IN} = 250 μ A
		5.5V		12		V	V _{IN} = 250 μ A
V _{CH}	Clock Input High Voltage	3.0V	0.7 V _{DD}	V _{DD} + 0.3	2.0	V	Driven by External Clock Generator
		5.5V	0.7 V _{DD}	V _{DD} + 0.3	3.0	V	Driven by External Clock Generator
V _{CL}	Clock Input Low Voltage	3.0V	V _{SS} - 0.3	0.2 V _{DD}	0.8	V	Driven by External Clock Generator
		5.5V	V _{SS} - 0.3	0.2 V _{DD}	1.5	V	Driven by External Clock Generator
V _{IH}	Input High Voltage Schmitt-Triggered	3.0V	0.7 V _{DD}	V _{DD} + 0.3	1.6	V	
		5.5V	0.7 V _{DD}	V _{DD} + 0.3	2.6	V	
V _{IH}	Input High Voltage CMOS Input	3.0V	0.7 V _{DD}	V _{DD} + 0.3	1.4	V	
		5.5V	0.7 V _{DD}	V _{DD} + 0.3	2.6	V	
V _{IL}	Input Low Voltage Schmitt-Triggered	3.0V	V _{SS} - 0.3	0.2 V _{DD}	0.8	V	
		5.5V	V _{SS} - 0.3	0.2 V _{DD}	1.5	V	
V _{IL}	Input Low Voltage CMOS Input	3.0V	V _{SS} - 0.3	0.2 V _{DD}	1.3	V	
		5.5V	V _{SS} - 0.3	0.2 V _{DD}	2.4	V	
V _{OH}	Output High Voltage	3.0V	V _{DD} - 0.4		2.8	V	I _{OH} = -2.0 mA
		5.5V	V _{DD} - 0.4		5.5	V	I _{OH} = -2.0 mA
V _{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I _{OL} = +4.0 mA
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA
V _{OL2}	Output Low Voltage	3.0V		1.5	0.8	V	I _{OL} = 10.0 mA, 6 Pin Max
		5.5V		0.8	0.3	V	I _{OL} = 10.0 mA, 6 Pin Max
V _{BO}	V _{CC} Brown-Out Voltage		1.6	2.7	2.3	V	@ 2 MHz Max
V _{TP}	Trip Point Voltage	3.0V		0.4 V _{DD}		V	
		5.5V		0.4 V _{DD}		V	
I _{IL}	Input Leakage	3.0V	-1.0	1.0	0.4	μ A	V _{IN} = 0V, V _{CC}
		5.5V	-1.0	1.0	0.4	μ A	V _{IN} = 0V, V _{CC}
I _{OL}	Output Leakage	3.0V	-1.0	1.0	0.4	μ A	V _{IN} = 0V, V _{CC}
		5.5V	-1.0	1.0	0.4	μ A	V _{IN} = 0V, V _{CC}

Note:

For 2.75V operating, the device operates down to V_{BO}. The minimum operational V_{DD} is determined on the value of the voltage V_{BO} at the ambient temperature. The V_{BO} increases as the temperature decreases.

Symbol	Parameter	V _{DD}	T _A = 0°C to +70°C		Typical @ 25°C	Units	Conditions
			Min	Max			
I _{DD}	Supply Current	3.0V		1.5	0.41	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		3.0	1.44	mA	All Output and I/O Pins Floating @ 1 MHz
		3.0V		2.0	0.93	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		4.0	2.60	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		3.0	1.64	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		6.0	4.28	mA	All Output and I/O Pins Floating @ 4 MHz
I _{DD1}	Standby Current	3.0V		0.6	0.15	mA	HALT mode V _{IN} = 0V, V _{CC} @ 1 MHz
		5.5V		1.3	0.70	mA	HALT mode V _{IN} = 0V, V _{CC} @ 1 MHz
		3.0V		0.8	0.20	mA	HALT mode V _{IN} = 0V, V _{CC} @ 2 MHz
		5.5V		1.5	0.80	mA	HALT mode V _{IN} = 0V, V _{CC} @ 2 MHz
		3.0V		1.0	0.3	mA	HALT mode V _{IN} = 0V, V _{CC} @ 4 MHz
		5.5V		2.0	1.0	mA	HALT mode V _{IN} = 0V, V _{CC} @ 4 MHz
I _{DD2}	Standby Current	3.0V		200	120	μA	STOP mode V _{IN} = 0V, V _{CC} WDT is Running
		5.5V		200	120	μA	STOP mode V _{IN} = 0V, V _{CC} WDT is Running
I _{PU}	Pull-Up Current						
	Port P00-P03	3.0V	-8	-35	-13	μA	V _m =0V
	Port P20-P23 Port P31-P33	5.5V	-25	-100	-56	μA	V _m =0V

AC ELECTRICAL CHARACTERISTICS

Timing Diagrams

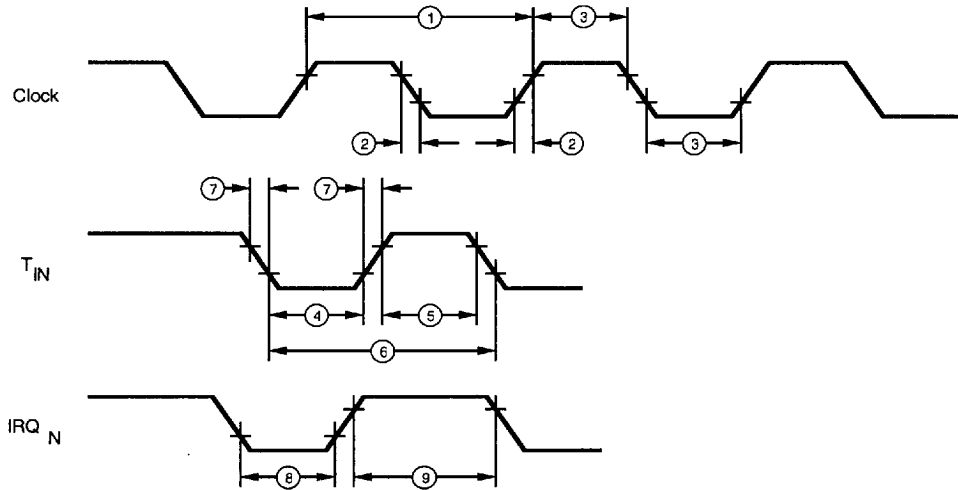


Figure 18. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

T _A = 0°C to +70°C									
No	Symbol	Parameter	V _{DD}	1 MHz		4 MHz		Units	Notes
				Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	1,000	100,000	250	100,000	ns	[1]
			5.5V	1,000	100,000	250	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	[1]
			5.5V		25		25	ns	
3	TwC	Input Clock Width	3.0V		475		100	ns	[1]
			5.5V		475		100	ns	[1]
4	TwTinL	Timer Input Low Width	3.0V		100		100	ns	[1]
			5.5V		70		70	ns	[1]
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer Time Out Timer	3.0V	25		25		ms	[1]
			5.5V	10		10		ms	[1]
11	T _{POR}	Power-On Reset Time	3.0V	6		6		ms	[1]
			5.5V	2		2		ms	[1]

Notes:

[1] Timing Reference uses 0.9 V_{DD} for a logic 1 and 0.1 V_{DD} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31)

Z8® CONTROL REGISTER DIAGRAMS

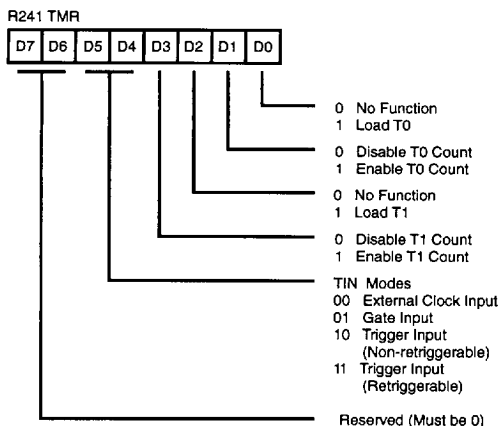


Figure 19. Timer Mode Register (F1H: Read/Write)

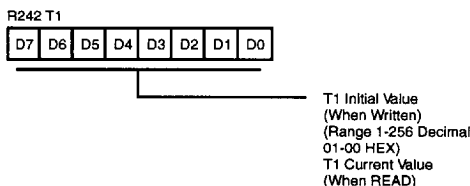


Figure 20. Counter Time 1 Register (F2H: Read/Write)

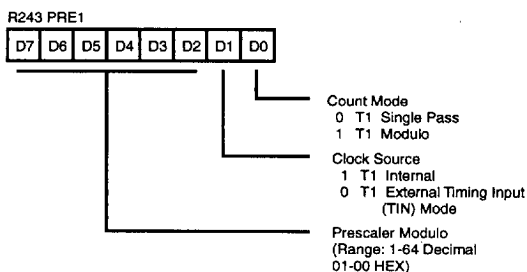


Figure 21. Prescaler 1 Register (F3H: Write Only)

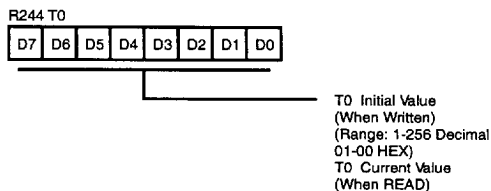


Figure 22. Counter/Timer 0 Register (F4H: Read/Write)

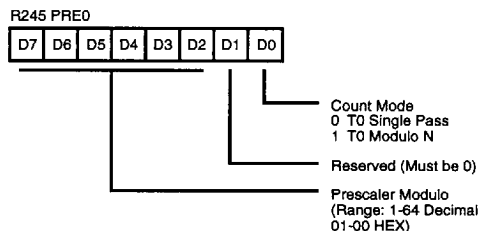


Figure 23. Prescaler 0 Register (F5H: Write Only)

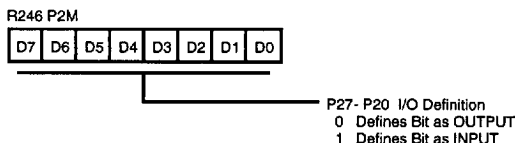


Figure 24. Port 2 Mode Register (F6H: Write Only)

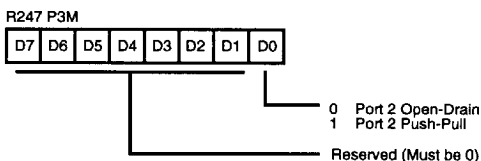


Figure 25. Port 3 Mode Register (F7H: Write Only)

R248 P01M

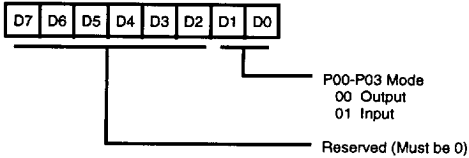


Figure 26. Port 0 and 1 Mode Register (F8H: Write Only)

R251 IMR

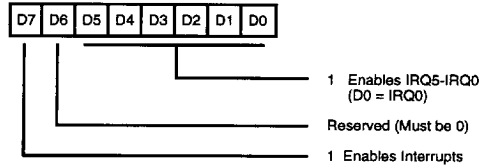


Figure 29. Interrupt Mask Register (FBH: Read/Write)

R249 IPR

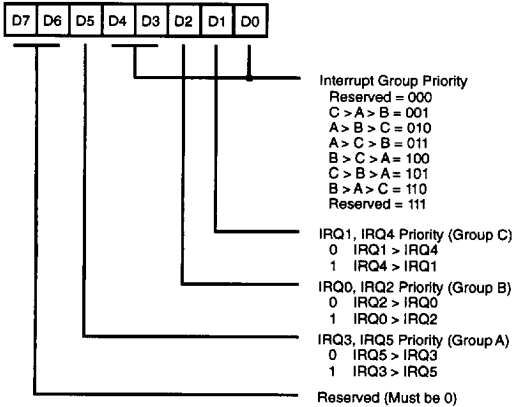


Figure 27. Interrupt Priority Register (F9H: Write Only)

R252 Flags

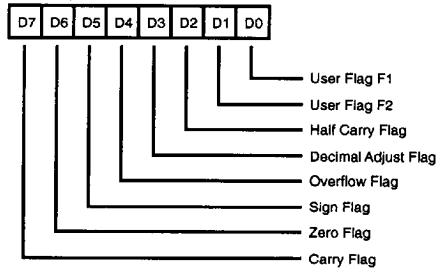


Figure 30. Flag Register (FCH: Read/Write)

R253 RP

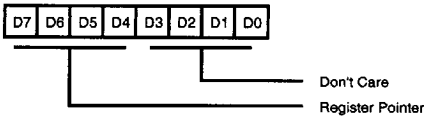


Figure 31. Register Pointer (FDH: Read/Write)

R250 IRQ

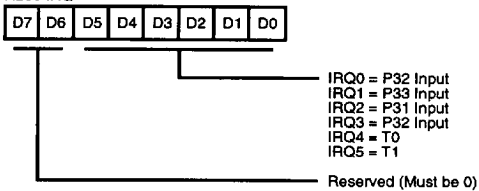


Figure 28. Interrupt Request Register (FAH: Read/Write)

R255 SPL

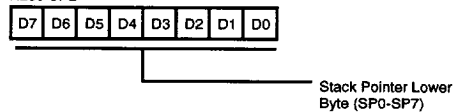


Figure 32. Stack Pointer (FFH: Read/Write)

DEVICE CHARACTERISTICS

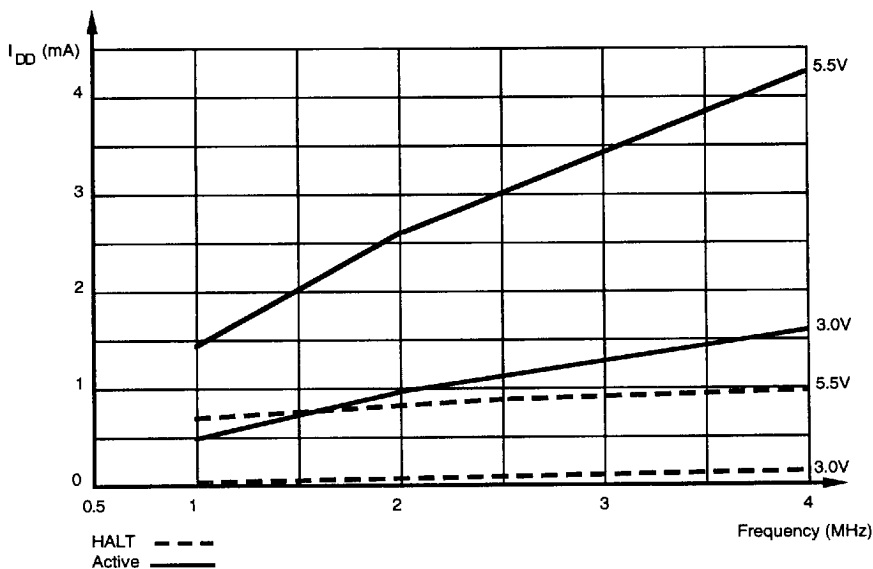


Figure 33. Typical I_{DD} vs Frequency

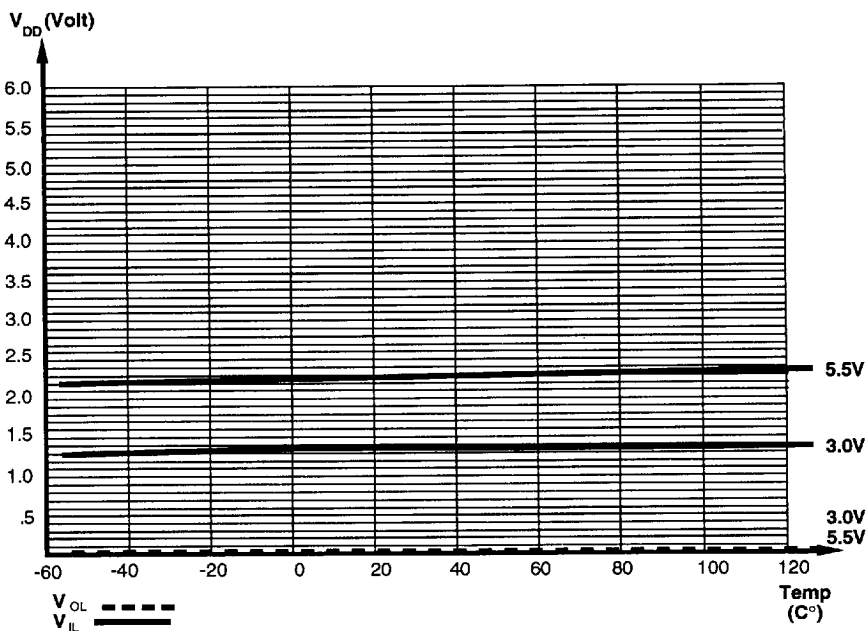
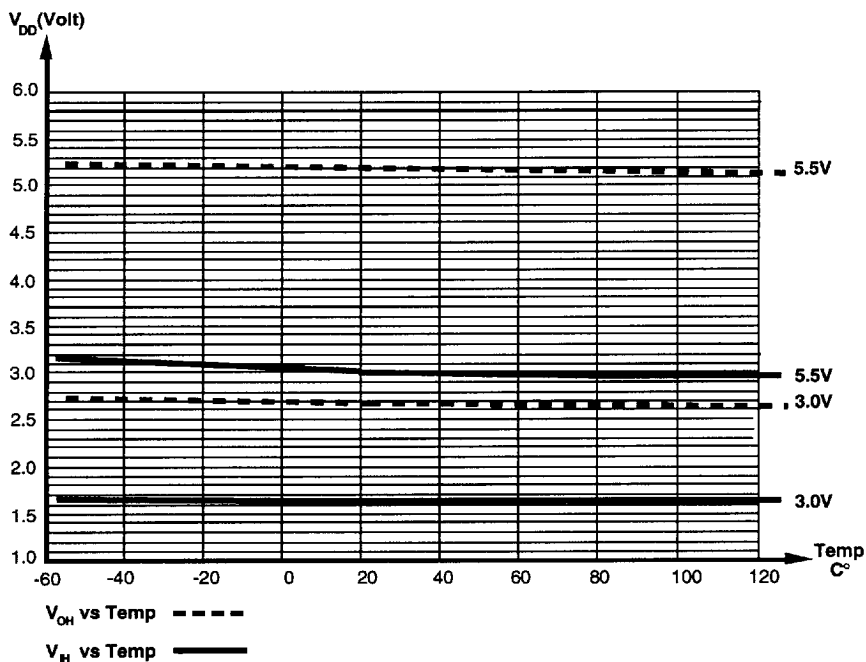
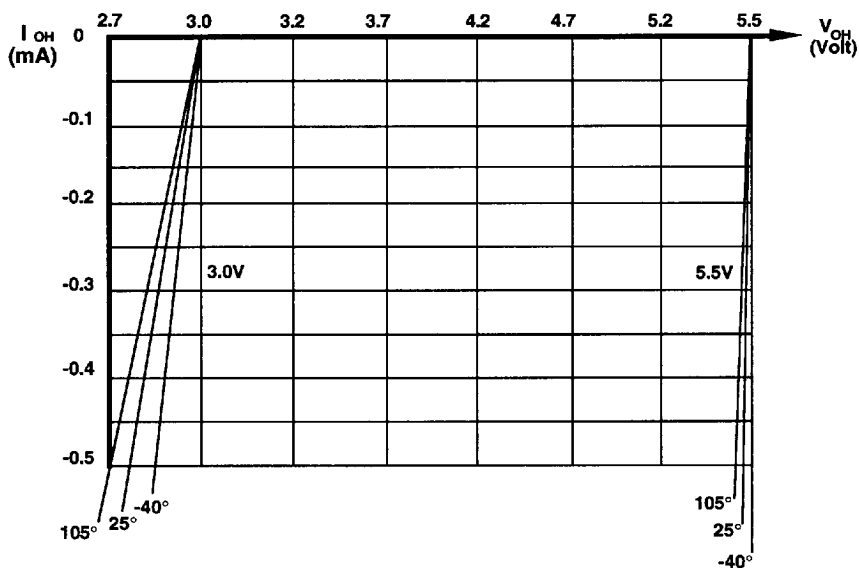
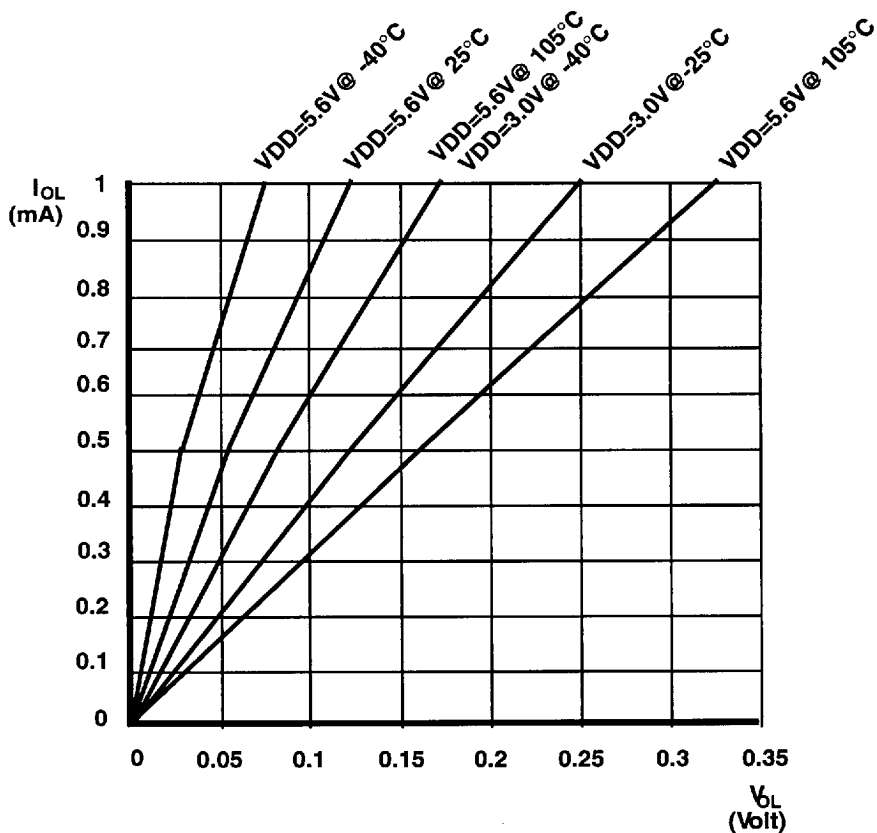


Figure 34. V_{IL} , V_{OL} vs Temperature

Figure 35. V_{IH} , V_{OH} vs TemperatureFigure 36. Typical I_{OH} vs V_{OH}

DEVICE CHARACTERISTICS (Continued)

Figure 37. Typical I_{OL} vs V_{OL}

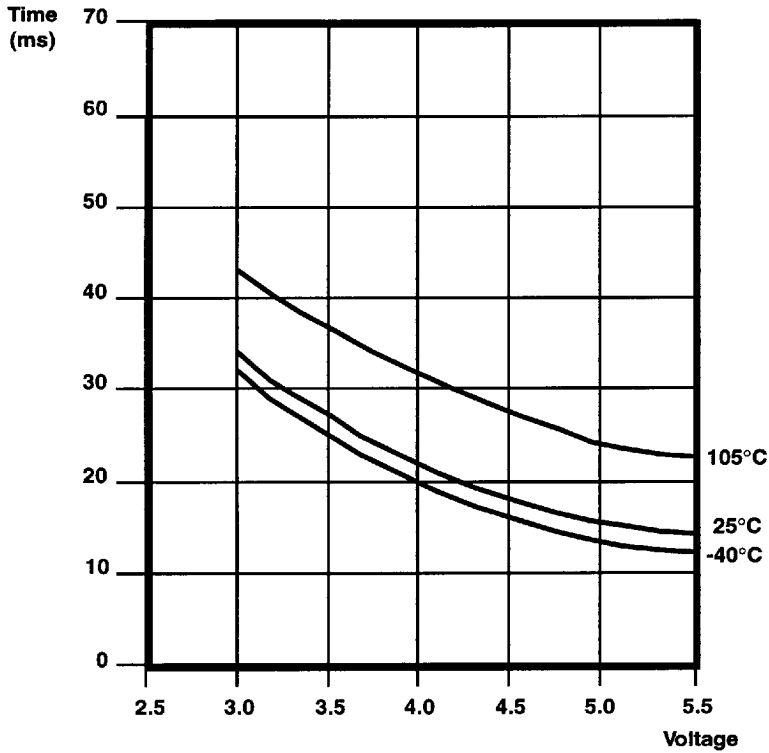


Figure 38. Typical WDT Time Out Period
vs V_{DD} Over Temperature

DEVICE CHARACTERISTICS (Continued)

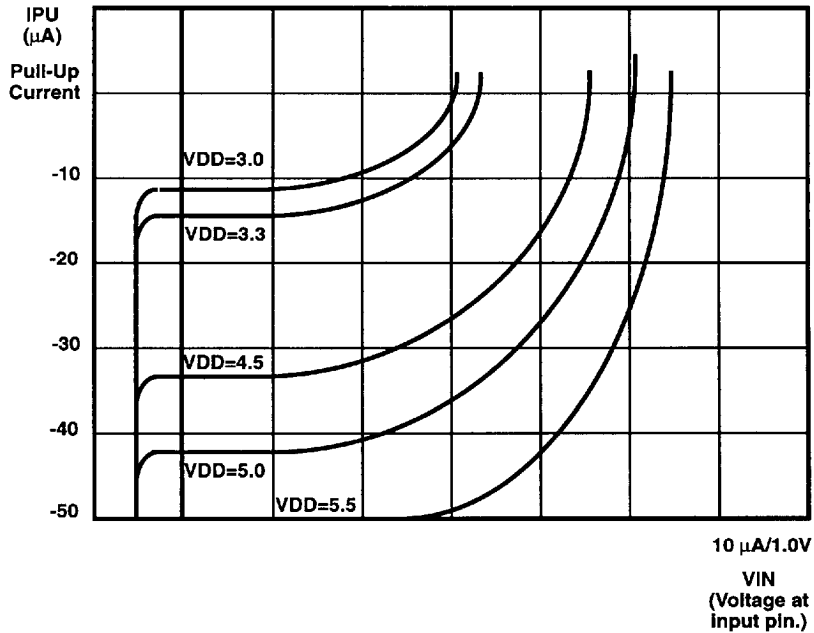


Figure 39. Pull-Up Resistance Characteristics
Port P23-P20, P31, P33, P02-P00

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

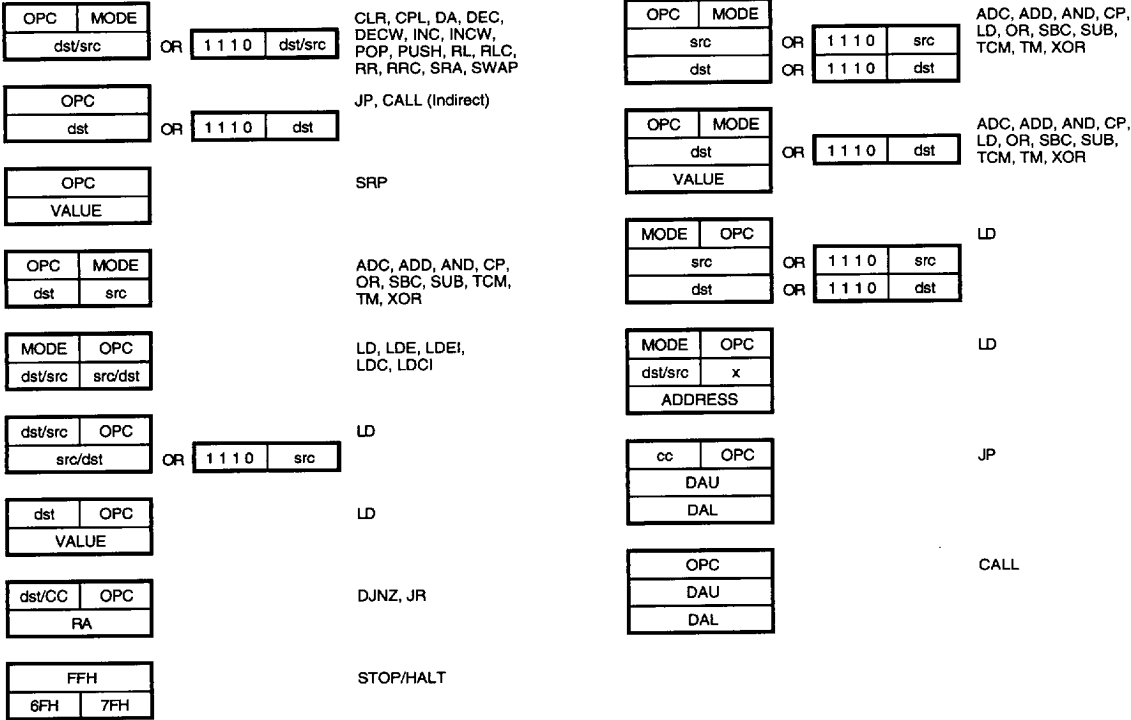
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	—	Always true	—
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Insighed greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000	F	Never true (Always False)	—

INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "---". For example:

dst --- dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The

notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

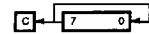
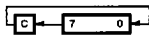
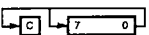
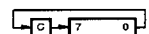
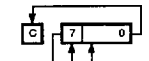
dst(7)

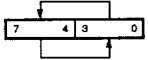
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected						
			C	Z	S	V	D	H	
ADC dst, src dst ← dst + src + C	†	1[]	*	*	*	*	0	*	
ADD dst, src dst ← dst + src	†	0[]	*	*	*	*	0	*	
AND dst, src dst ← dst AND src	†	5[]	-	*	*	*	0	-	-
CALL dst SP ← SP - 2 @SP ← PC, PC ← dst	DA IRR	D6 D4	-	-	-	-	-	-	-
CCF C ← NOT C		EF	*	-	-	-	-	-	-
CLR dst dst ← 0	R IR	B0 B1	-	-	-	-	-	-	-
COM dst dst ← NOT dst	R IR	60 61	-	*	*	*	0	-	-
CP dst, src dst - src	†	A[]	*	*	*	*	*	-	-
DA dst dst ← DA dst	R IR	40 41	*	*	*	*	X	-	-
DEC dst dst ← dst - 1	R IR	00 01	-	*	*	*	*	-	-
DECW dst dst ← dst - 1	RR IR	80 81	-	*	*	*	*	-	-
DI IMR(7) ← 0		8F	-	-	-	-	-	-	-
DJNZ r, dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA	rA r = 0 - F	-	-	-	-	-	-	-
EI IMR(7) ← 1		9F	-	-	-	-	-	-	-
HALT		7F	-	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected						
			C	Z	S	V	D	H	
INC dst dst ← dst + 1	r R IR	rE r = 0 - F 20 21	-	*	*	*	*	-	-
INCW dst dst ← dst + 1	RR IR	A0 A1	-	*	*	*	*	-	-
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1		BF	*	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR	cD c = 0 - F 30	-	-	-	-	-	-	-
JR cc, dst if cc is true, PC ← PC + dst Range: +127, -128	RA	cB c = 0 - F	-	-	-	-	-	-	-
LD dst, src dst ← src	r r R r r X r lr lr R R R IR IR IM IR R	Im rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-	-
LDC dst, src dst ← src	r lrr	C2	-	-	-	-	-	-	-
LDCI dst, src dst ← src r ← r + 1; rr ← rr + 1	lr lrr	C3	-	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	- - - - -
OR dst, src dst←dst OR src	†	4[]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - -
PUSH src SP←SP - 1; @SP←src	R IR	70 71	- - - - -
RCF C←0		CF	0 - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst←src←C	†	3[]	* * * * 1 *
SCF C←1		DF	1 - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
STOP		6F	1 - - - -
SUB dst, src dst←dst←src	†	2[]	[[[[1 [
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[]	- * * 0 - -
TM dst, src dst AND src	†	7[]	- * * 0 - -
XOR dst, src dst←dst XOR src	†	B[]	- * * 0 - -

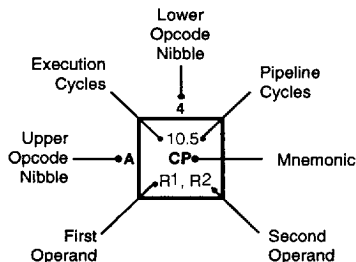
† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst src	Lower Opcode Nibble
r r	[2]
r Ir	[3]
R R	[4]
R IR	[5]
R IM	[6]
IR IM	[7]

OPCODE MAP

		Lower Nibble (Hex)																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Upper Nibble (Hex)	0	6.5 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	6.5 ADD r1, Ir2	10.5 ADD R2, R1	10.5 ADD IR2, R1	10.5 ADD R1, IM	10.5 ADD IR1, IM	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/10.0 JR cc, RA	6.5 LD r1, IM	12.10.0 JP cc, DA	6.5 INC r1		
	1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, IM	10.5 ADC IR1, IM									
	2	6.5 INC R1	6.5 INC IR1	6.5 SUB r1, r2	6.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R1, IM	10.5 SUB IR1, IM									
	3	8.0 JP IRR1	6.1 SRP IM	6.5 SBC r1, r2	6.5 SBC r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, IM	10.5 SBC IR1, IM									
	4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, IM	10.5 OR IR1, IM									
	5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, IM	10.5 AND IR1, IM								6.0 WDT	
	6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, IM	10.5 TCM IR1, IM								6.0 STOP	
	7	10/12.1 PUSH R2	12/14.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, IM	10.5 TM IR1, IM								7.0 HALT	
	8	10.5 DECW RR1	10.5 DECW IR1															6.1 DI
	9	6.5 RL R1	6.5 RL IR1															6.1 EI
	A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, IM	10.5 CP IR1, IM									14.0 RET
	B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR IR2, R1	10.5 XOR R1, IM	10.5 XOR IR1, IM									16.0 IRET
	C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Ir2	18.0 LDCI Ir1, Ir2				10.5 LD r1,x,R2									6.5 RCF
	D	6.5 SRA R1	6.5 SRA IR1			20.0 CALL* IRR1		20.0 CALL DA	10.5 LD r2,x,R1									6.5 SCF
	E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, IR2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, IM	10.5 LD IR1, IM									6.5 CCF
	F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2		10.5 LD R2, IR1											6.0 NOP
		2				3				2				3			1	
		Bytes per Instruction																



Legend:

R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

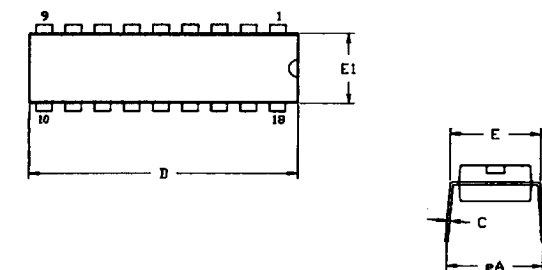
Sequence:

Opcode, First Operand,
Second Operand

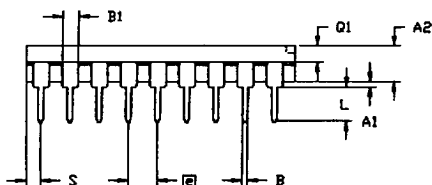
Note: Blank areas not defined.

*2-byte instruction appears as
a 3-byte instruction

PACKAGE INFORMATION

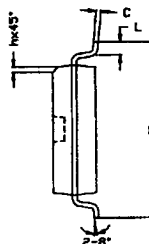
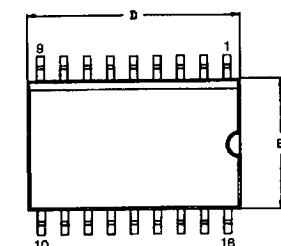


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
■	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065



CONTROLLING DIMENSIONS : INCH

18-Pin Plastic DIP Package Diagram



CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
■	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86217

4 MHz

Z8621704PSC

Z8621704SSC

For fast results, contact your local Zilog sales offices for assistance in ordering the part desired.

Package

P=Plastic DIP

S=Small Outline Integrated Circuit

Temperature

S = 0°C to +70°C

Speed

04 = 4 MHz

Environmental

C = Plastic Standard

Example:

Z 86217 04 P S C is an 86217, 4 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

