PRODUCT SPECIFICATION T-49-19-07

Z86C09/C19

CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-bit CMOS microcontroller, 18-pin DIP
- Low cost
- 3.0 to 5.5 volt operating range
- Low power consumption-50 mW (typical)
- Fast instruction pointer, 1.0 microseconds @ 12 MHz
- Two standby modes - STOP and HALT
- 14 input/output lines (2 with Comparator inputs)
- All digital inputs are CMOS levels and Schmitt triggered
- 2K, 4 Kbytes of ROM, Z86C09, Z86C19, respectively
- 124 bytes of RAM
- Two Expanded Register File Control Registers
- Two programmable 8-bit Counter/Timers
- 6-bit programmable prescaler
- 6 vectored, priority interrupts from five different sources
- Clock speeds 8 and 12 MHz
- Brown-out protection
- Watchdog/Power-On Reset Timer
- Two Comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC, or external clock drive.

GENERAL DESCRIPTION

The Z86C09 and Z86C19 Consumer Controller Processors (CCP™) introduce a new level of sophistication to single-chip architecture. The Z86C09 and Z86C19 are members of the Z8 single-chip microcontroller family with 2K and 4K bytes of ROM, respectively, and 124 bytes of RAM. The devices are housed in a 18-pin DIP, and are CMOS compatible. Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C09/C19 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many industrial, automotive, and advanced scientific applications.

The device applications demand powerful I/O capabilities. The CCP fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 124 bytes of General-Purpose Registers, two I/O Port registers and fifteen Control and Status registers. The Expanded Register File consists of two control registers.

To unburden the program from coping with real-time problems such as counting/timing and input/output data communication, the Z86C09/C19 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators that can process analog signals with a common reference voltage (Figure 1).

GENERAL DESCRIPTION (Continued)

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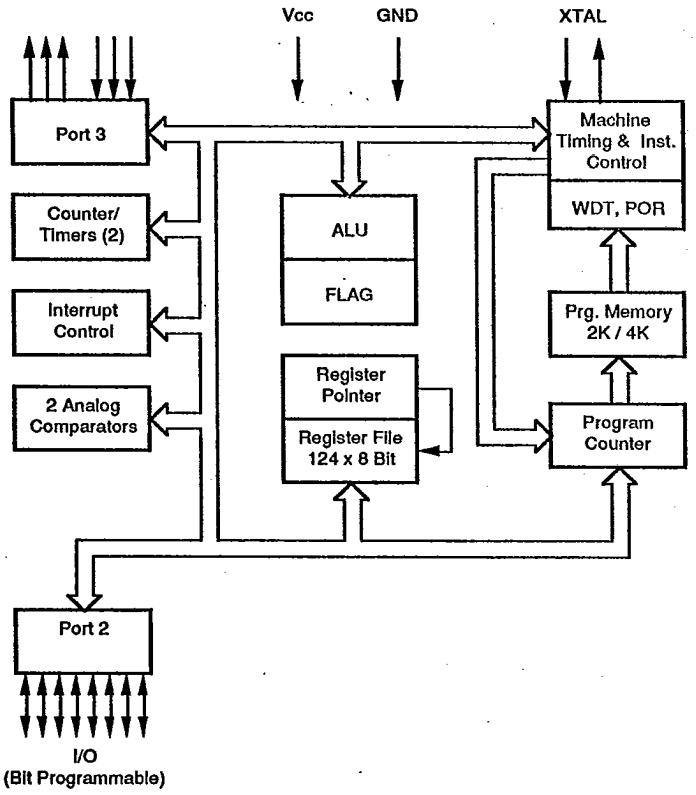

Figure 1. Functional Block Diagram

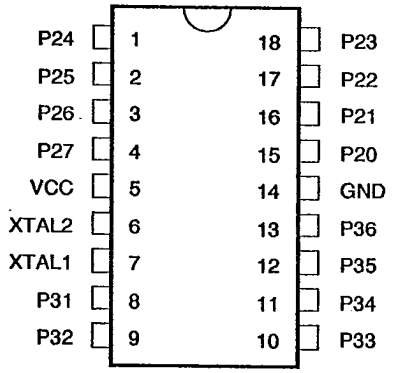

Figure 2. Pin Configuration

PIN DESCRIPTION

Table 1. Pin Identification

No	Symbol	Function	Direction
1-4	P24-7	Port 2 pin 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	Input
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-3	Port 3 pin 1, 2, 3	Fixed Input
11-13	P34-6	Port 3 pin 4, 5, 6	Fixed Output
14	GND	Ground	Input
15-18	P20-3	Port 2 pin 0, 1, 2, 3	In/Output

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 P20-P27. Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These 8 I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open drain (Figure 3).

PIN DESCRIPTION (Continued)

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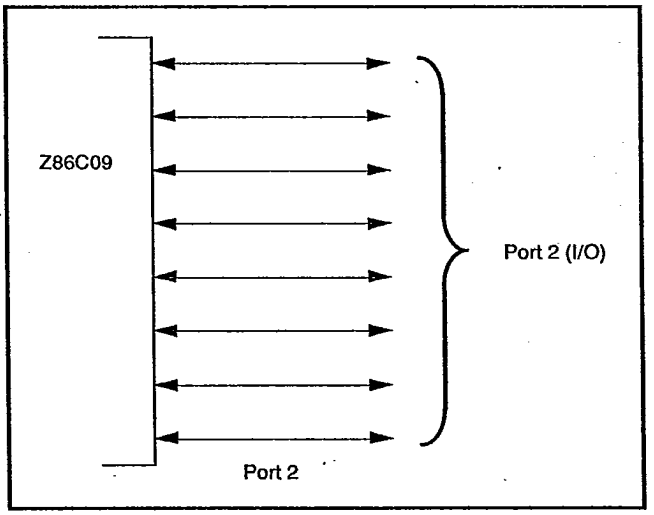

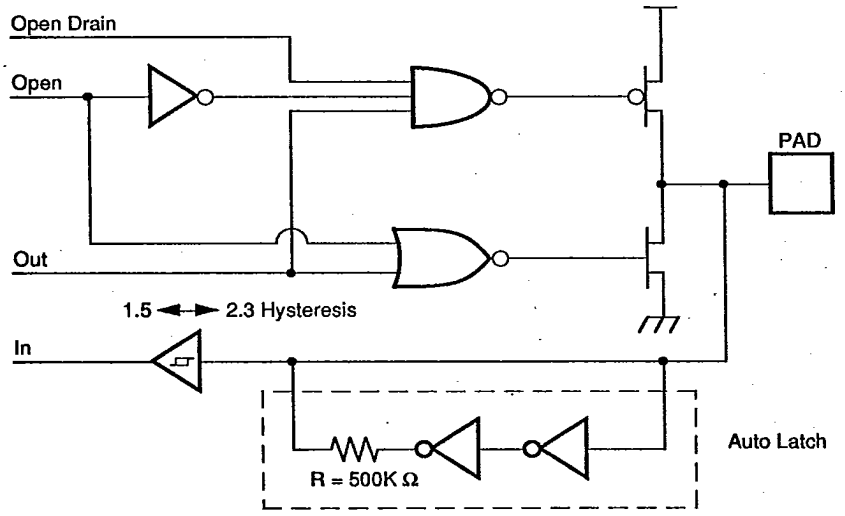

Figure 3. Port 2 Configuration

Auto-Latch. The auto-latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This will reduce excessive supply current flow in the input buffer when it is not been driven by any source.

Port 3 P31-P36. Port 3 is a 6-bit, CMOS compatible port with three fixed input and three fixed output lines. These 6 lines consist of three fixed input (P31-P33) and three fixed output port (P34-P36) lines. Pins P31,P32 and P33 are standard CMOS inputs and pins P34,P35,and P36 are push-pull outputs. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (bit 1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to Counter/Timer 1 is made through P31 (Tin) and P36 (Tout), (Figure 4).

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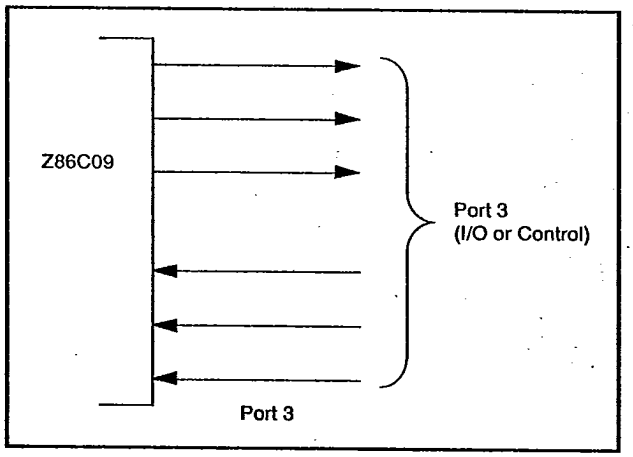

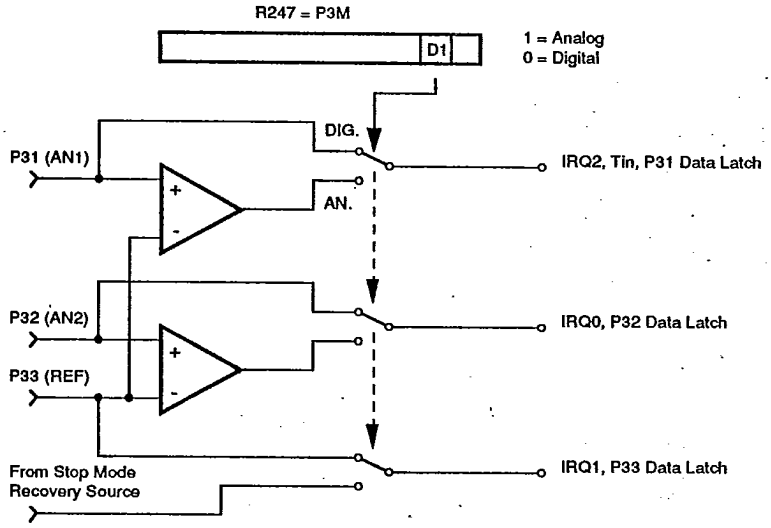

Figure 4. Port 3 Configuration

PIN DESCRIPTION (Continued)

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Comparator Inputs. Port 3, Pin P31 and Pin P32 each have a comparator front end. The comparator reference voltage Pin P33 is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. The internal P33 register and its corresponding IRQ1 is connected to the STOP Mode Recovery source selected by the SMR. In this mode, any of the STOP Mode Recovery sources can be used to toggle the P33 bit or generate IRQ1. In digital mode, Pin P33 can be used as a P33 register input or IRQ1 source (Figure 13).

Auto-Latch. The auto-latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not being driven by any source.

FUNCTIONAL DESCRIPTION

The Z8 CCP incorporates special functions to enhance the Z8's application in industrial, scientific research, and advanced technologies applications.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP Mode Recovery Source

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a STOP Mode Recovery operation.

Program Memory. Z86C09/C19 can address up to 2K/4K bytes of internal program memory respectively (Figure 5). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 2048/4096 consists of on-chip mask-programmed ROM.

The 2K/4K bytes of Program Memory is mask programmable. A ROM protect feature will prevent "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to program memory in all modes.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 6). These register groups are known as the ERF (Expanded Register File). Bits 3:0 of the Register Pointer (RP) select the active ERF group. Bits 7:4 of register RP select the working register group (Figure 7). Two system configuration registers reside in the Expanded Register File address space at bank F. The rest of the Expanded Register addressing space is not physically implemented, and is open for future expansion.

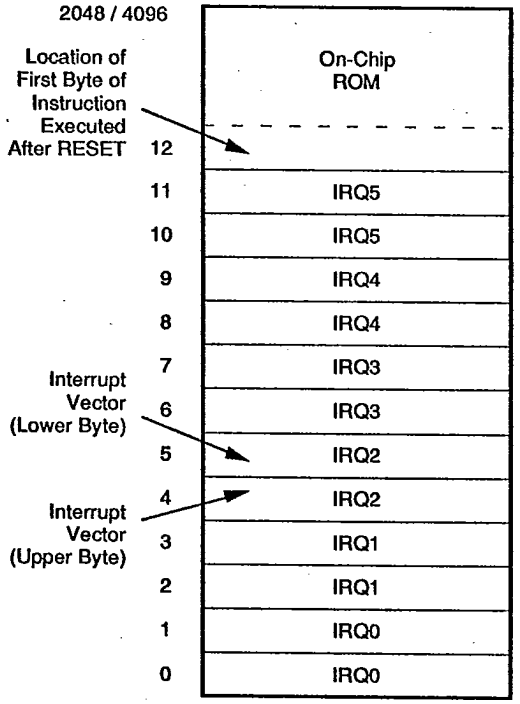

Figure 5. Program Memory Map

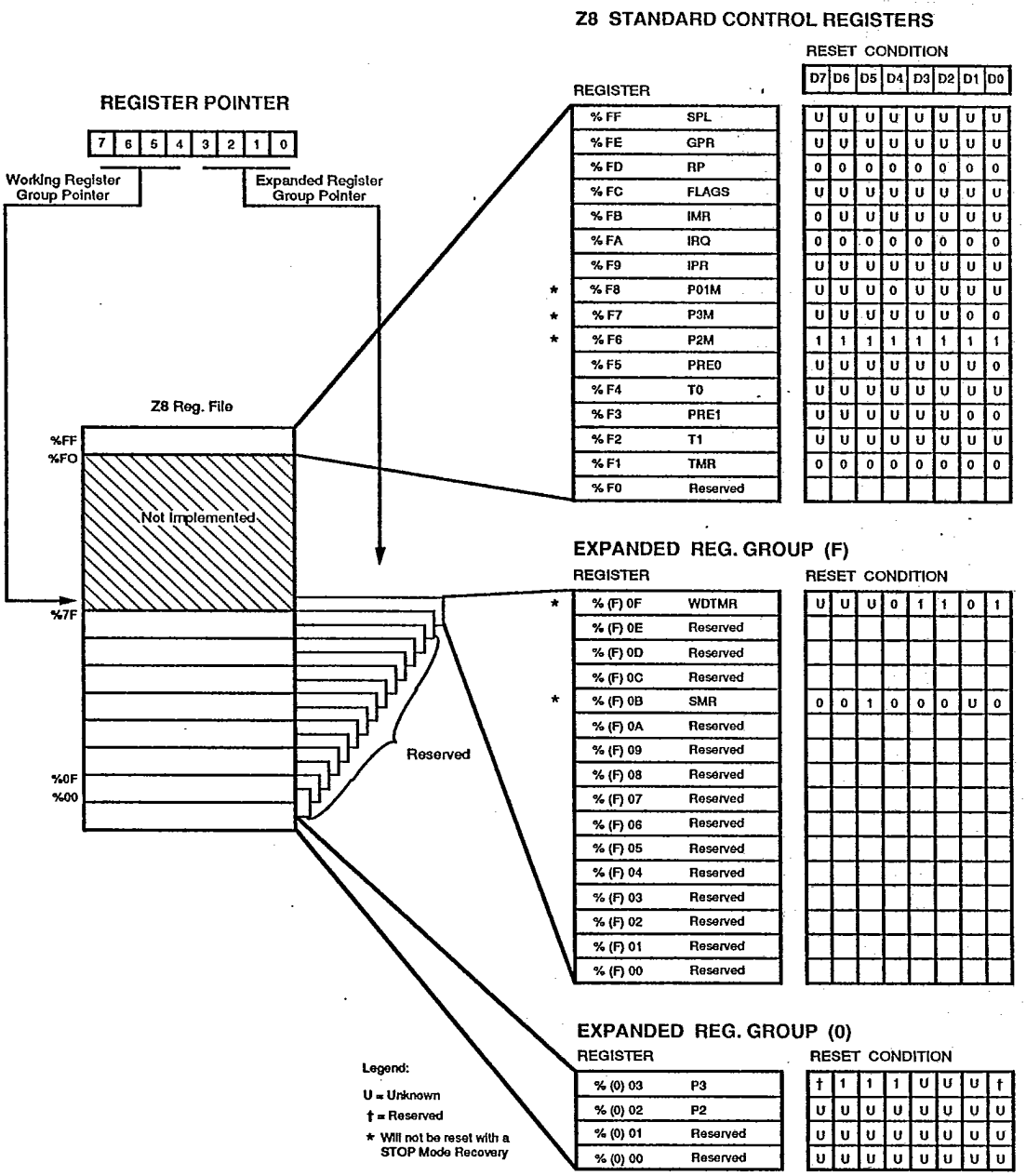

Figure 6. Expanded Register File Architecture

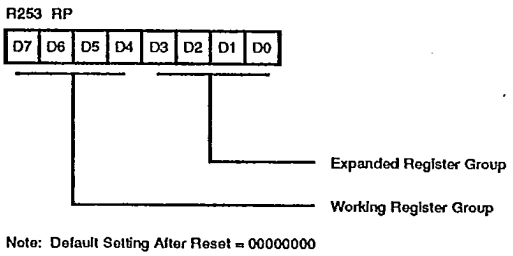

Figure 7. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 124 general purpose registers, and 15 control and status registers, and two system configuration registers in the Expanded Register Group (Figure 6). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 8). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Caution: D4 of Control Register P01M (R251) must be "0". If the Z86C09/19 is emulated by Z86C90, D4 of P01M has to change to "0" before submission to ROM code.

GPR. The Z86C09/C19 has one extra General Purpose Register located at %FE(R254).

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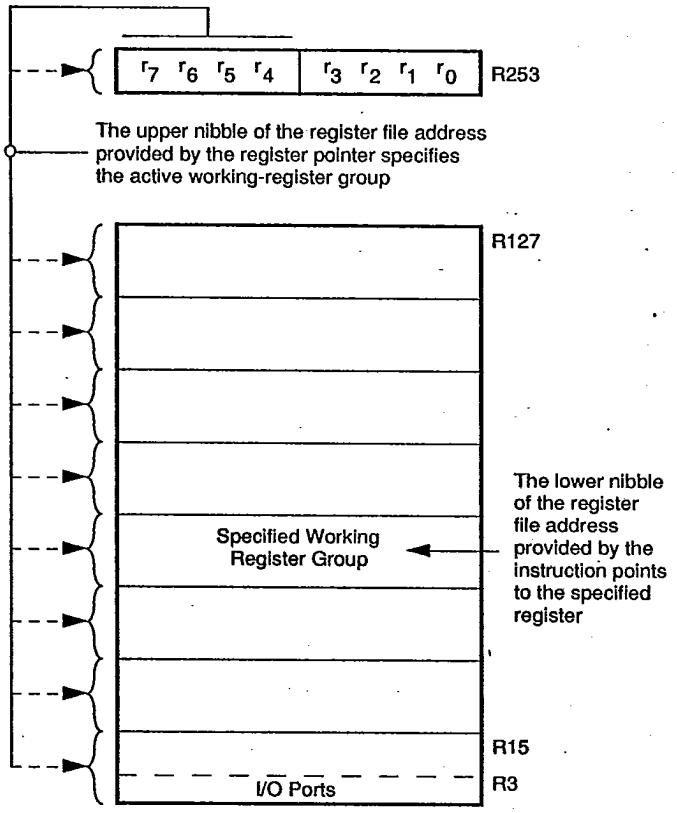

Figure 8. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

Stack. The Z86C09/C19 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 9).

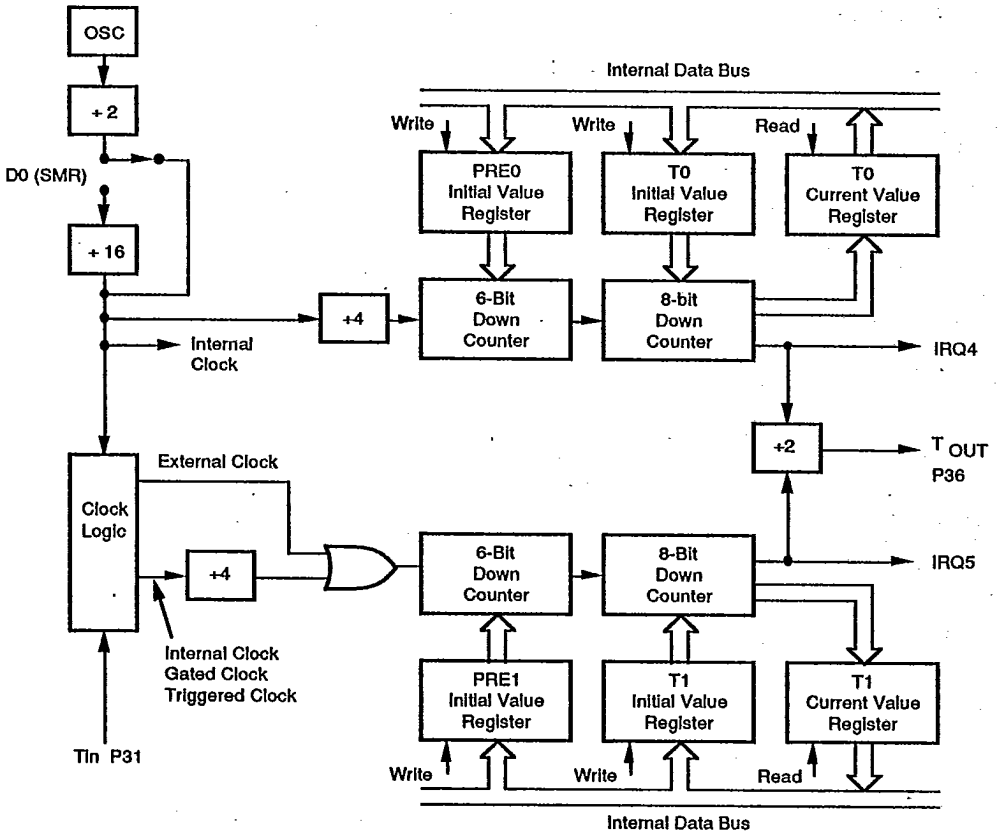

Figure 9. Counter/Timer Block Diagram

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request-IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or not-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (Tout) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Interrupts. The Z86C09/Z86C19 has six different interrupts from five different sources. The interrupts are mask-able and prioritized (Figure 10). The five sources are divided as follows; three sources are claimed by Port 3 lines P31-P33, and two sources in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 2).

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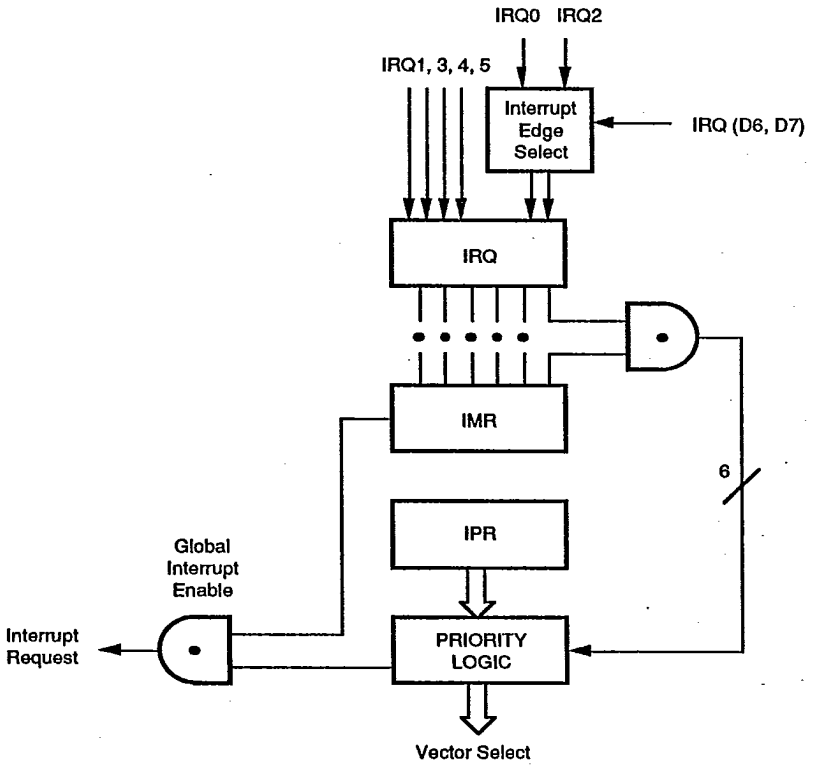

Figure 10. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

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Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	IRQ 0	0, 1	External (P32), ≠ Ø Edge Triggered
IRQ 1	IRQ 1	2, 3	External (P33), Ø Edge Triggered
IRQ 2	IRQ 2, TIN	4,5	External (P31), ≠ Ø Edge Triggered
IRQ 3		6, 7	Software Generated Only
IRQ 4	T0	8, 9	Internal
IRQ 5	TI	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86C09/C19 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs services. IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register).

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

The programming bits for the INTERRUPT EDGE SELECT are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

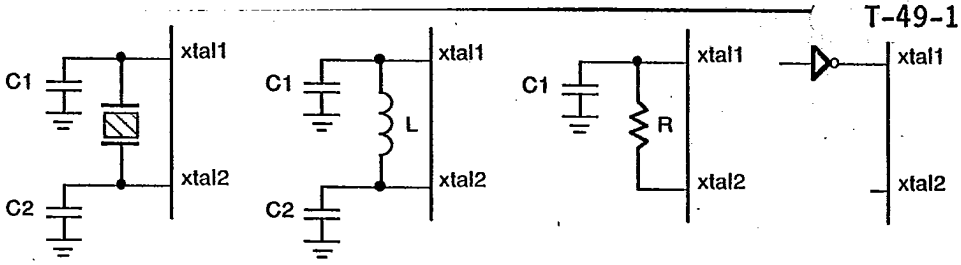
Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86C09/C19 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 KHz to 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (C1 is more than or equal to 22 pf) from each pin to ground. The RC oscillator option is mask-programmable, to be selected by the customer at the time the ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 11). The RC value vs Frequency curves are shown in Figure 48 and 49. **(Limitation:** The RC option is not avaiable in the 12 MHz part.)



Ceramic Resonator or Crystal	LC	RC	External Clock
C1, C2 = 47 pf TYP *	C1, C2 = 22 pf	@ 5V VCC (TYP)	
F = 8 MHz	L = 130 µH *	C1 = 33 pf	
	F = 3 MHz *	R = 1K	
		F = 16 MHz	

* Preliminary Value Including Pin Parasitics

Figure 11. Oscillator Configuration

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the Power-On Reset (POR) timer function. The POR time allows Vcc and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the three conditions:

1. Power fail to Power OK status
2. STOP mode recovery (If D5 of SMR=1)
3. WDT timeout

The POR time is a nominal 5mS. Bit 5 of the Stop Mode Register determines whether the POR timer is bypassed after STOP mode recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Will turn off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamps or less. The Stop mode is terminated by a RESET only, either by WDT timeout, POR, or SMR recovery. This causes the processor to restart the application program at address 000C (HEX).

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

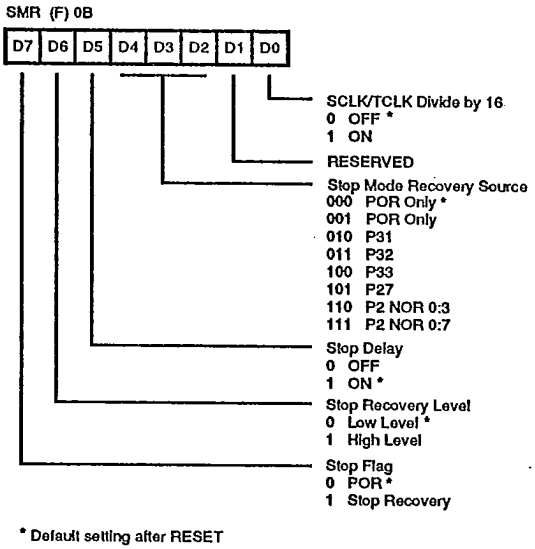
```
FF  NOP; clear the pipeline
6F  STOP; enter STOP mode
```

or

```
FF  NOP; clear the pipeline
7F  HALT; enter HALT mode
```

Stop Mode Register (SMR). This register selects the clock divide value and determines the mode of STOP mode recovery (Figure 12). All bits are write only except Bit 7 which is Read only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2,3, and 4 of the SMR specify the source of the STOP mode recovery signal. If the XTAL1 is used as a source to drive the POR counter, then the STOP Mode Recovery time is XTAL/512. The SMR is located in bank F of the Expanded Register Group at address 0BH.

FUNCTIONAL DESCRIPTION (Continued)



* Default setting after RESET

Figure 12. STOP Mode Recovery Register

SCLK/TCLK divide-by-16 select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic).

STOP Mode Recovery Source (D2, D3, and D4). These 3 bits of the SMR specify the wake-up source of the STOP Mode recovery (Figure 13 and Table 4).

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Table 4. Stop Mode Recovery Source

SMR D4	SMR D3	SMR D2	Operation Description of action
0	0	0	POR recovery only
0	0	1	POR recovery only
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

P31-P33 can not wake up from STOP mode if the input lines are configured as analog input.

STOP Mode Recovery Delay Select (D5). This bit disables the 5mS RESET delay after STOP Mode Recovery. The default condition of this bit is 1.

STOP Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP mode. A 0 indicates low level recovery. The default is 0 on POR. (See Figure 13).

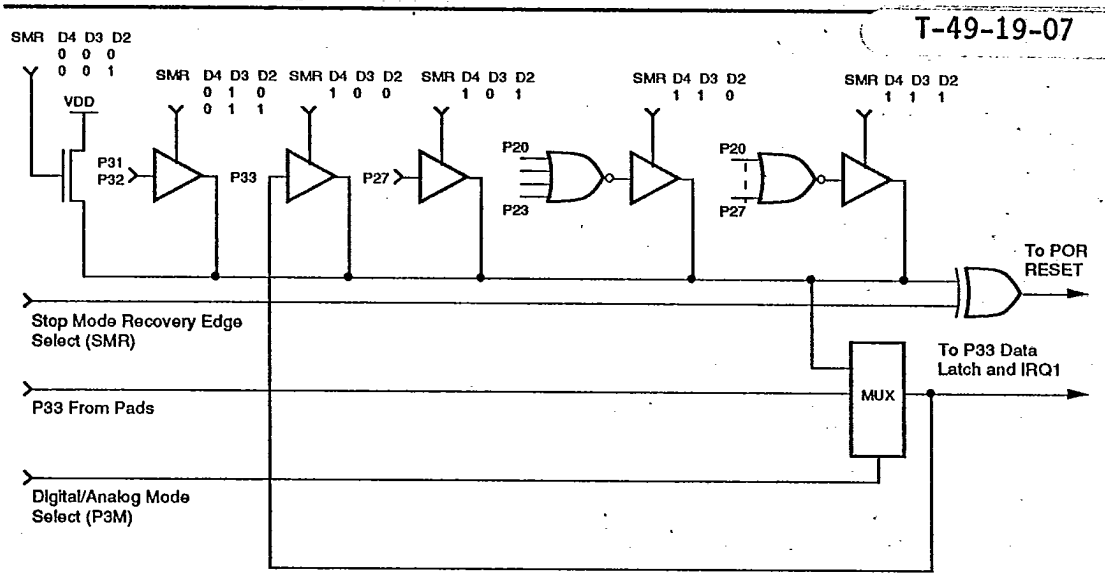

Figure 13. STOP Mode Recovery Source

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. It is active high, and is 0 (cold) on POR/WDT RESET. This bit is a READ only. It is used to distinguish between cold or warm start.

Watch Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that will reset the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and retriggered on subsequent executions of the WDT instruction. The timer circuit is driven by an on-board RC oscillator or external XTAL1 pin.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the timeout period. Bit 2 determines whether the WDT is active during HALT and Bit 3 determines WDT activity during STOP. Bits 5 through Bit 7 are reserved (Figure 14). This register is accessible only during the first 64 processor cycles (128 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch Dog Reset or a Stop Mode Recovery (Figure 15). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location OFH. It is organized as follows:

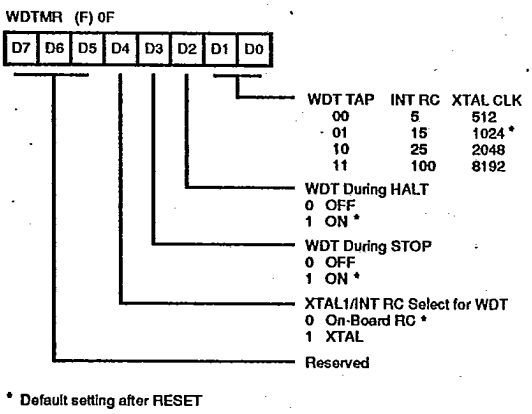

Figure 14. Watchdog Timer Mode Register

FUNCTIONAL DESCRIPTION (Continued)

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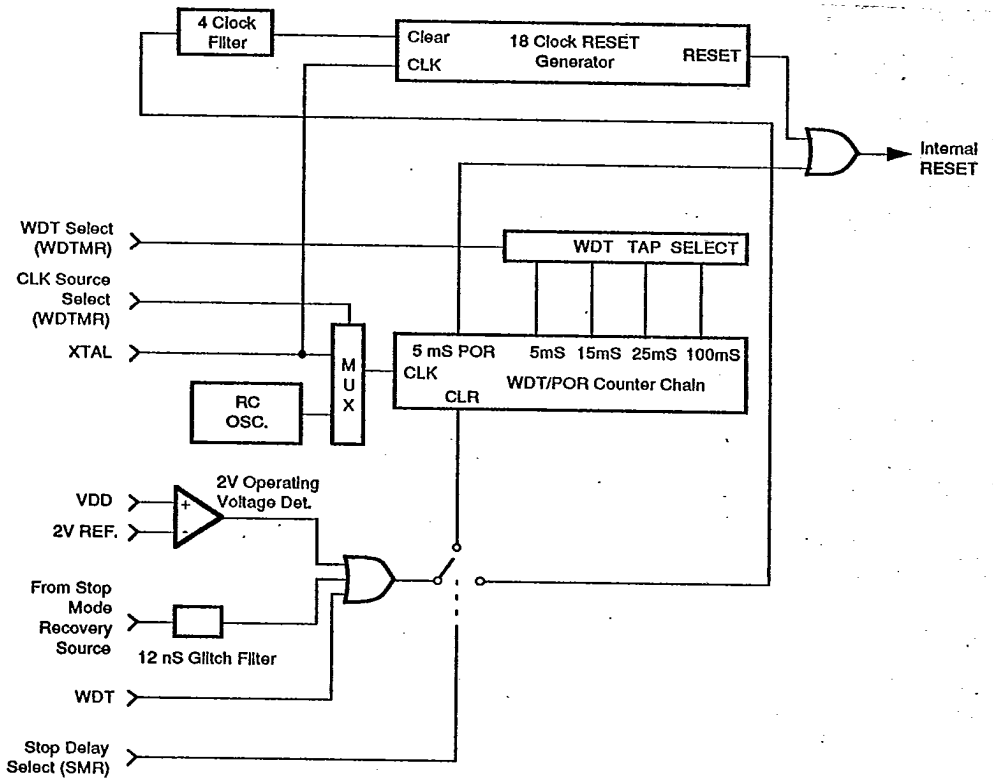


Figure 15. Resets and WDT

WDT Time Select (D1, D0). Selects the WDT time period. It is configured as shown in Table 5.

Table 5. WDT Time Select

D1	D0	Timeout Period (On-board RC) Clock Source	XTAL1 Clock Source
0	0	5mS min	XTAL1/512
0	1	15mS min	XTAL1/1024
1	0	25mS min	XTAL1/2048
1	1	100mS min	XTAL1/8192

Notes:
The default on a WDT initiated RESET is 15 mS.
See Figures 44 to 47 for details.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP mode, the on-board RC has to be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

On-Board Power-On-Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage (typically 2.1V).

Brown Out Protection (V_{BO}). The brown out trip voltage (V_{BO}) will be less than 3 volts and above 1.4 volts under the following conditions.

Maximum (V_{BO}) Conditions:

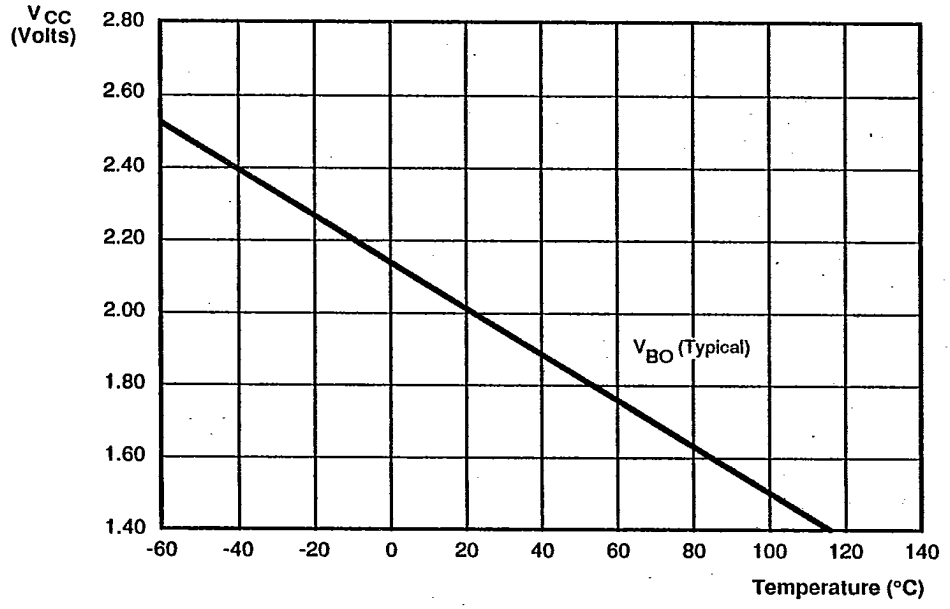
Case 1 T_A= -40, +105°C, Internal Clock Frequency equal or less than 1 MHz

Case 2 T_A= -40, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note:
The internal clock frequency is one half the external clock frequency.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device will function normally until the Brown Out Protection trip point (V_{BO}) is reached, for the temperatures and operating frequencies in case 1 and case 2 above. The device is guaranteed to function normally at supply voltages above the brown out trip point. The actual brown out trip point is a function of temperature and process parameters (Figure 16). T-49-19-07

ROM Protect. ROM protect is mask-programmable. It is selected by the customer at the time the ROM code is submitted. **The selection of ROM protect will disable the LDC and LDCI instructions.**



* Power-on Reset threshold for V_{CC} and 4 MHz V_{BO} overlap

Figure 16. Typical Z86C19 V_{BO} Voltage Vs Temperature

ABSOLUTE MAXIMUM RATINGS

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Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage *	-0.3	+7.0	V
TSTG	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp	†		C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 17).

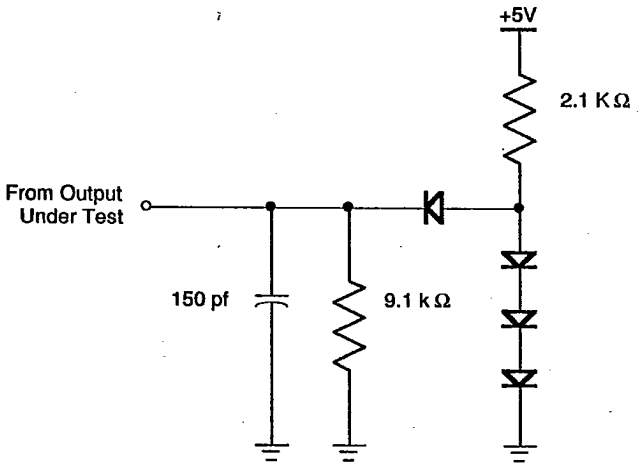

Figure 17. Test Load Configuration

DC ELECTRICAL CHARACTERISTICS
Z86C09/C19

T-49-19-07

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to 70°C Min	T_A = 0°C to 70°C Max	T_A = -40°C to 105°C Min	T_A = -40°C to 105°C Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	3.3V		12		12		V	$I_{IN} \leq 250\ \mu A$	
		5.0V		12		12		V	$I_{IN} \leq 250\ \mu A$	
V_{CH}	Clock Input High Voltage	3.3V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator	
		5.0V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	3.9	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.3V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.6	V	Driven by External Clock Generator	
		5.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	2.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.3V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.0	V		
		5.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.3V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	
$V_{OL}1$	Output Low Voltage	3.3V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	
$V_{OL}2$	Output Low Voltage	3.3V		1.0		1.0	0.4	V	I_{OL} = 6 mA, 3 Pin Max	
		5.0V		1.0		1.0	0.5	V	I_{OL} = +12 mA, 3 Pin Max	
V_{OFFSET}	Comparator Input Offset Voltage	3.3V		25		25	10	mV		
		5.0V		25		25	10	mV		
I_{IL}	Input Leakage (Input bias current of comparator)	3.3V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.0V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.3V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.0V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	3.3V		6		6	3.0	mA	@ 8 MHz	[4,5]
		5.0V		11.0		11.0	6.0	mA	@ 8 MHz	[4,5]
		3.3V		8.0		8.0	4.5	mA	@ 12 MHz	[4,5]
		5.0V		15		15	9.0	mA	@ 12 MHz	[4,5]

DC ELECTRICAL CHARACTERISTICS (Continued)

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Z86C09/C19

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to 70°C Min	Max	T_A = -40°C to 105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
$I_{CC}1$	Standby Current	3.3V		3.0		3.0	1.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4, 5]
		5.0V		5		5	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4, 5]
		3.3V		4.5		4.5	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4, 5]
		5.0V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4, 5]
		3.3V		1.4		1.4	0.7	mA	Clock Divide by 16 @ 8 MHz	[4, 5]
		5.0V		3.5		3.5	2.0	mA	Clock Divide by 16 @ 8 MHz	[4, 5]
		3.3V		2.0		2.0	1.0	mA	Clock Divide by 16 @ 12 MHz	[4, 5]
		5.0V		4.5		4.5	2.5	mA	Clock Divide by 16 @ 12 MHz	[4, 5]
$I_{CC}2$	Standby Current	3.3V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		5.0V		10		20	3.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		3.3V					TBD	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6]
		5.0V		TBD		TBD	200	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6]
I_{ALL}	Auto Latch Low Current	3.3V		7.0		14.0	4.0	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		20.0		30.0	10	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.3V		-4.0		-8.0	-2.0	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		-9.0		-16.0	-5.0	µA	$0V < V_{IN} < V_{CC}$	
T_{POR}	Power On Reset	3.3V	7	24	6	25	13	mS		
		5.0V	3	13	2	14	7	mS		
V_{BO}	V_{CC} Brown Out Voltage		1.50	2.65	1.2	2.95	2.1	V	2 MHz max Ext. CLK Freq.	[3]

Notes:

[1] $I_{CC}1$

	Type	Max	Unit	Freq
Clock Driven on Crystal	3.0	5.0	mA	8 MHz
or XTAL Resonator	0.3	50	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] 5.0V ± 0.5V, 3.0V ± 0.3V. The V_{BO} increases as the temperature decreases.

[4] All outputs unloaded, I/O pins floating, inputs at rail.

[5] $C_{L1} = C_{L2}$ = 100pf

[6] Same as note [4] except inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

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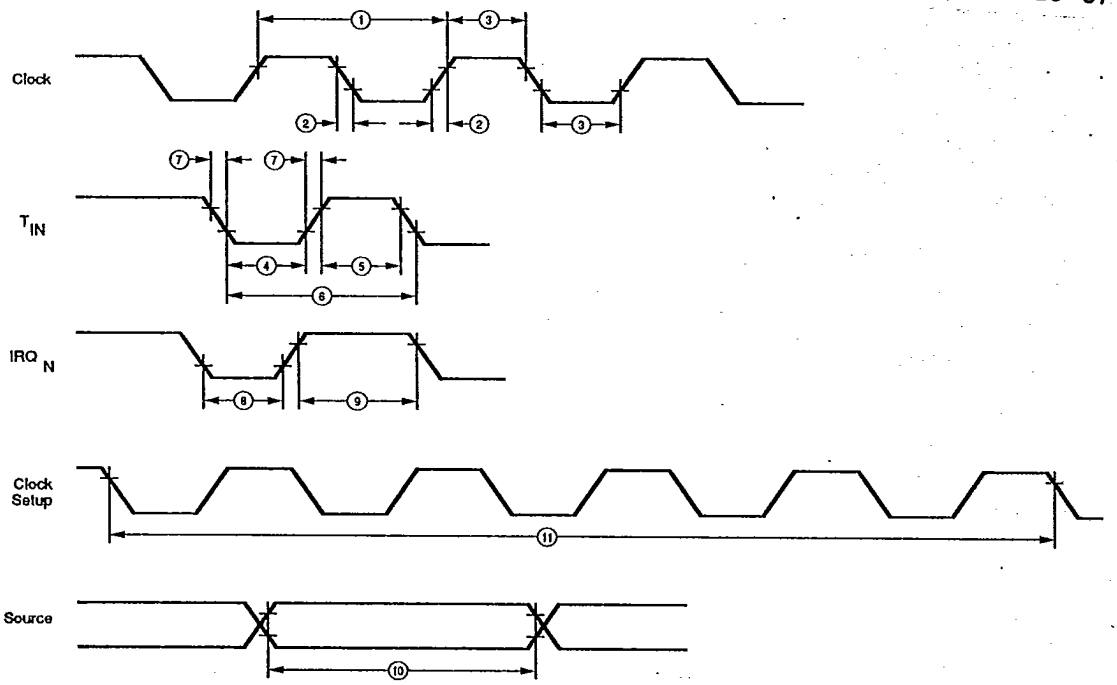

Figure 18. Additional Timing

AC ELECTRICAL CHARACTERISTICS
Z86C09/C19

No	Symbol	Parameter	V_{cc} Note[3]	T_A = 0°C TO 70°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	T_A = -40°C TO 105°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.3V	125	100,000	83	100,000	125	100,000	83	100,000	ns	[1]
			5.0V	125	100,000	83	100,000	125	100,000	83	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.3V		25		15		25		15	ns	[1]
			5.0V		25		15		25		15	ns	[1]
3	TwC	Input Clock Width	3.3V	37		26		37		26		ns	[1]
			5.0V	37		26		37		26		ns	[1]
4	TwTinL	Timer Input Low Width	3.3V	100		100		100		100		ns	[1]
			5.0V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.3V	3TpC		3TpC		3TpC		3TpC			[1]
			5.0V	3TpC		3TpC		3TpC		3TpC			[1]

AC ELECTRICAL CHARACTERISTICS (Continued)
Z86C09/C19

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No	Symbol	Parameter	V_{cc} Note[3]	T_A = 0°C TO 70°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	T_A = -40°C TO 105°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
6	TpTin	Timer Input Period	3.3V	8TpC		8TpC		8TpC		8TpC			[1]
			5.0V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin, TfTin	Timer Input Rise and Fall Timer	3.3V		100		100		100		100	ns	[1]
			5.0V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.3V	100		100		100		100		ns	[1,2]
			5.0V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.3V	3TpC		3TpC		3TpC		3TpC			[1,2]
			5.0V	3TpC		3TpC		3TpC		3TpC			[1,2]
10	Twsm	STOP Mode Recovery Width Spec	3.3V	12		12		12		12		ns	
			5.0V	12		12		12		12		ns	
11	Tost	Oscillator Startup Time	3.3V		5TpC		5TpC		5TpC		5TpC		Reg. [4]
			5.0V		5TpC		5TpC		5TpC		5TpC	ns	
	Twdt	Watchdog Timer Refresh Time	3.3V	15		15		12		12			[5]
			5.0V	5		5		3		3		ms	D0 = 0 D1 = 0
			3.3V	30		30		25		25		ms	D0 = 0
			5.0V	16		16		12		12		ms	D1 = 1
			3.3V	60		60		50		50		ms	D0 = 0
			5.0V	25		25		30		30		ms	D1 = 1
			3.3V	250		250		200		200		ms	D0 = 1
			5.0V	120		120		100		100		ms	D1 = 1

Notes:

[1] Timing Reference uses 0.9 V_{cc} for a logic "1" and 0.1 V_{cc} for a logic "0".
[2] Interrupt request via Port 3 (P31-P33)
[3] 5.0V ± 0.5V, 3.3V ± 0.3V
[4] SMR-D5 = 0
[5] Reg. WDTMR

EXPANDED REGISTER FILE CONTROL REGISTERS

T-49-19-07

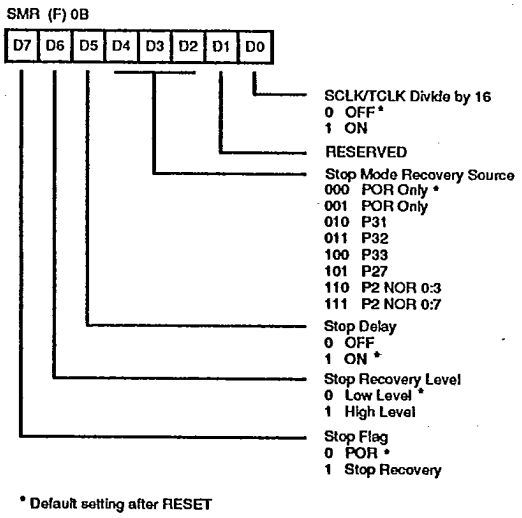

Figure 19. STOP Mode Recovery Register

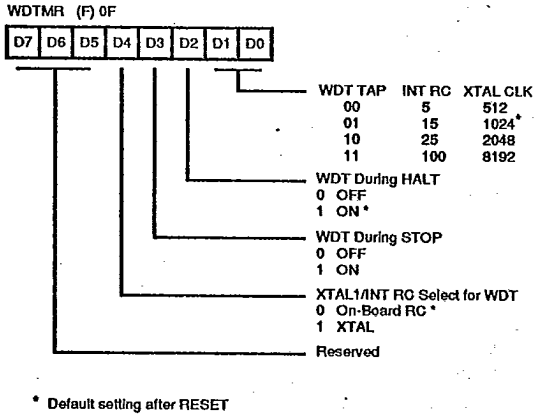

Figure 20. Watchdog Timer Mode Register

Z8 CONTROL REGISTER DIAGRAMS

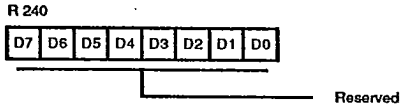

Figure 21. Reserved

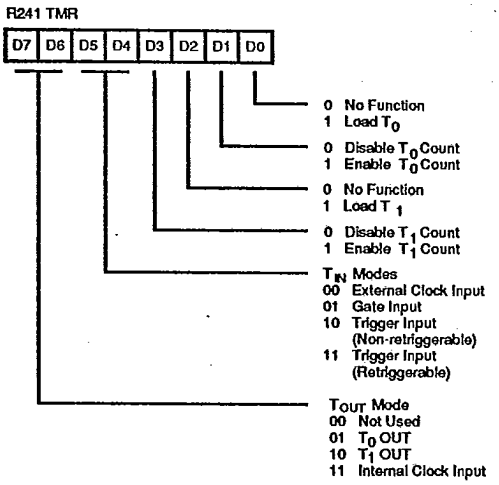

Figure 22. Timer Mode Register
(F1H: Read/Write)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

T-49-19-07

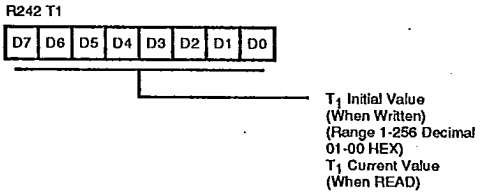

Figure 23. Counter Timer 1 Register
(F2H: Read/Write)

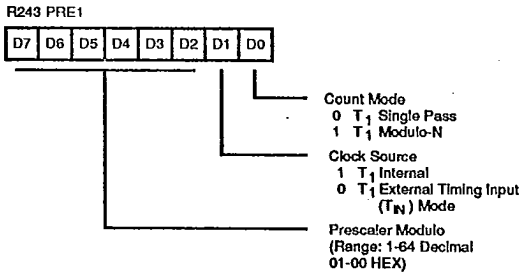

Figure 24. Prescaler 1 Register
(F3H: Write Only)

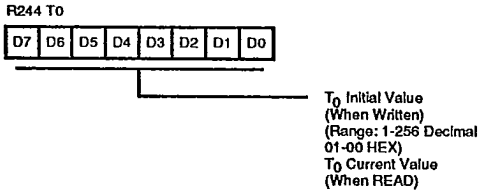

Figure 25. Counter/Timer 0 Register
(F4H: Read/Write)

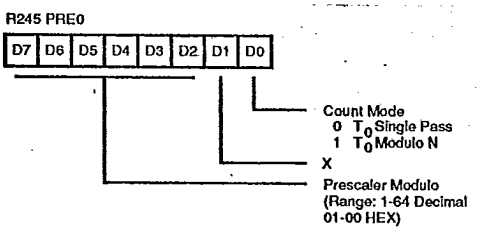

Figure 26. Prescaler 0 Register
(F5H: Write Only)

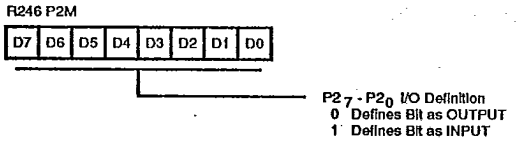

Figure 27. Port 2 Mode Register
(F6H: Write Only)

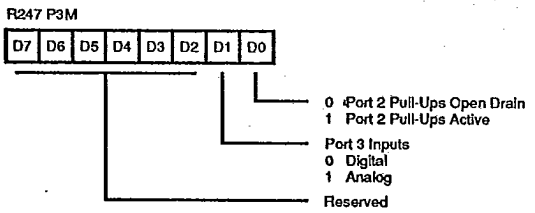

Figure 28. Port 3 Mode Register
(F7H: Write Only)

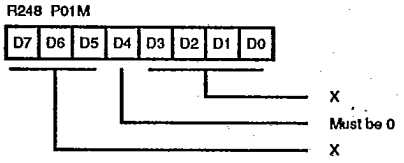

Figure 29. Port 0 and 1 Mode Register

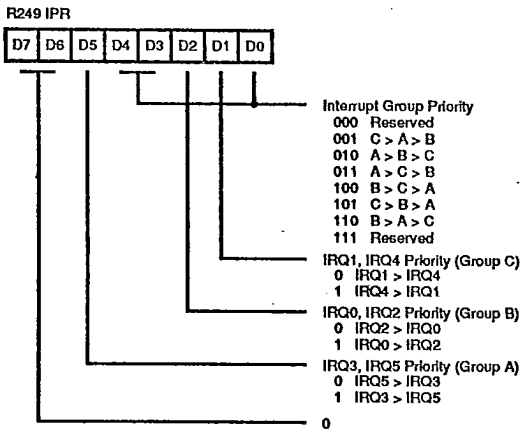

Figure 30. Interrupt Priority Register
(F9H: Write Only)

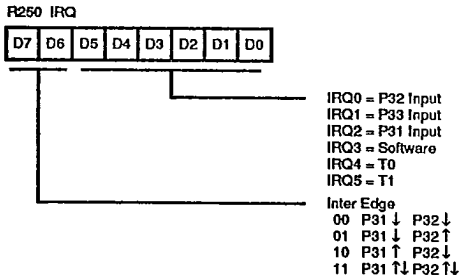

Figure 31. Interrupt Req Register
(FAH: Read/Write)

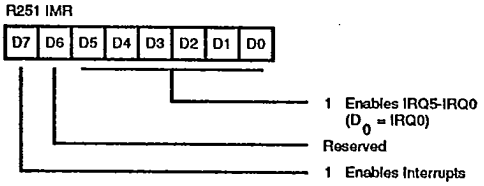

Figure 32. Interrupt Mask Register
(FBH: Read/Write)

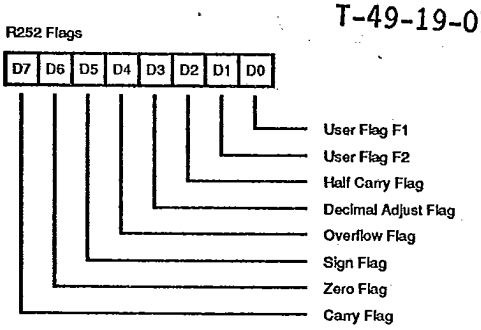

Figure 33. Flag Register
(FCH: Read/Write)

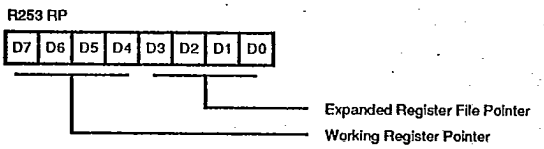

Figure 34. Register Pointer
(FDH: Read/Write)

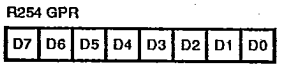

Figure 35. General Purpose Register
(FEH: Read/Write)

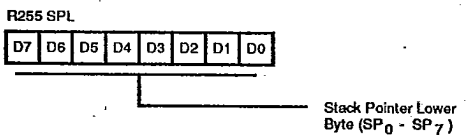

Figure 36. Stack Pointer
(FFH: Read/Write)

DEVICE CHARACTERISTICS
Graphs Illustrate Device Characteristics

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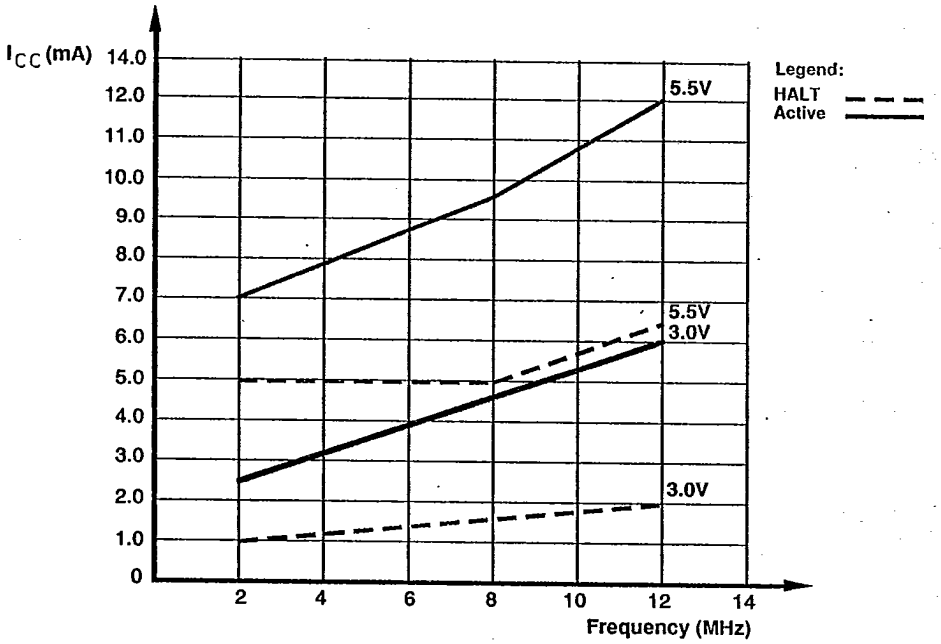


Figure 37. Maximum I_{cc} Vs Frequency

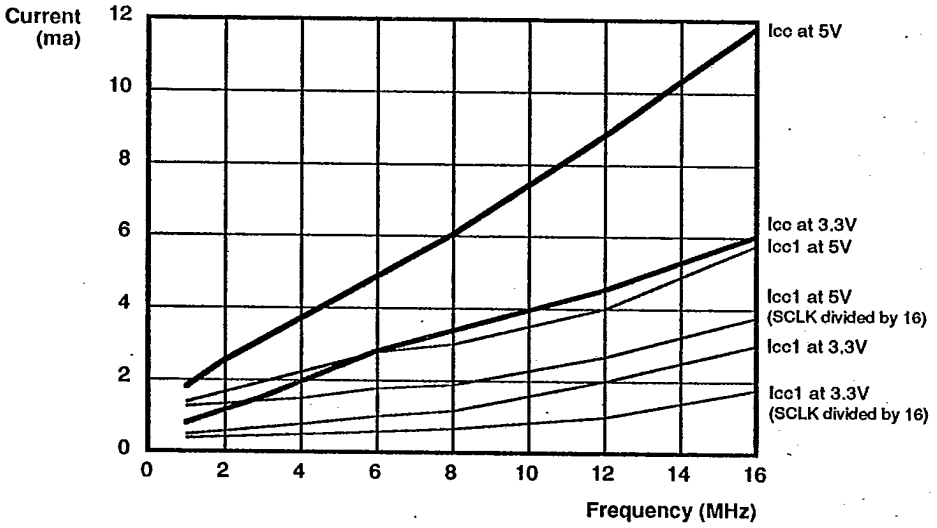
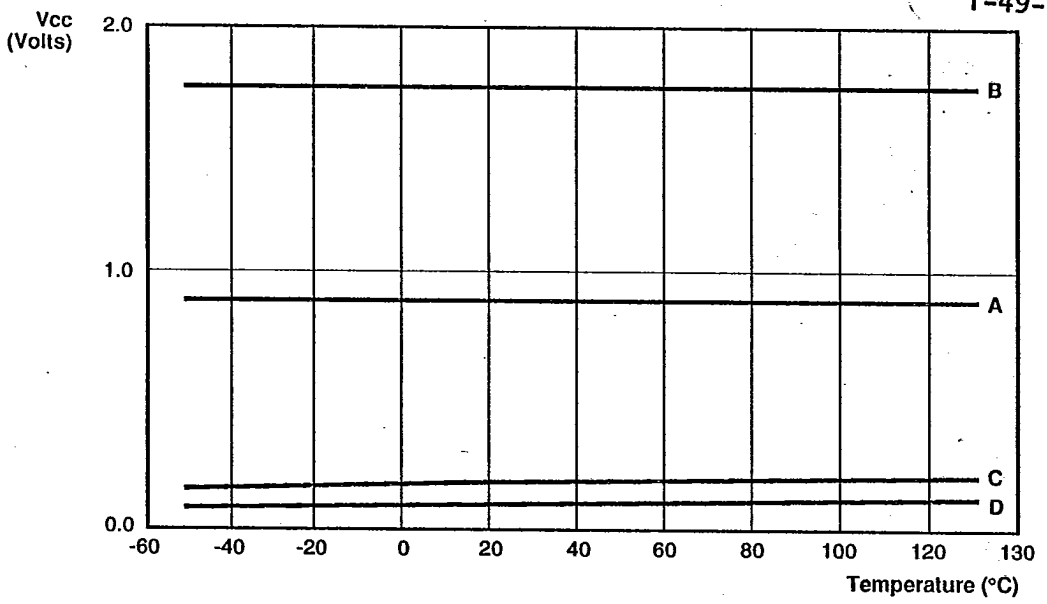


Figure 38. Typical I_{cc} Vs Frequency



Legend:
A = Vil at Vcc = 3.3V B = Vil at Vcc = 5.5V C = Vol at Vcc = 3.0V D = Voil at Vcc = 5.5V

Figure 39. Typical V_{OL}, V_{IL} Vs Temperature

DEVICE CHARACTERISTICS (Continued)
Graphs Illustrate Device Characteristics

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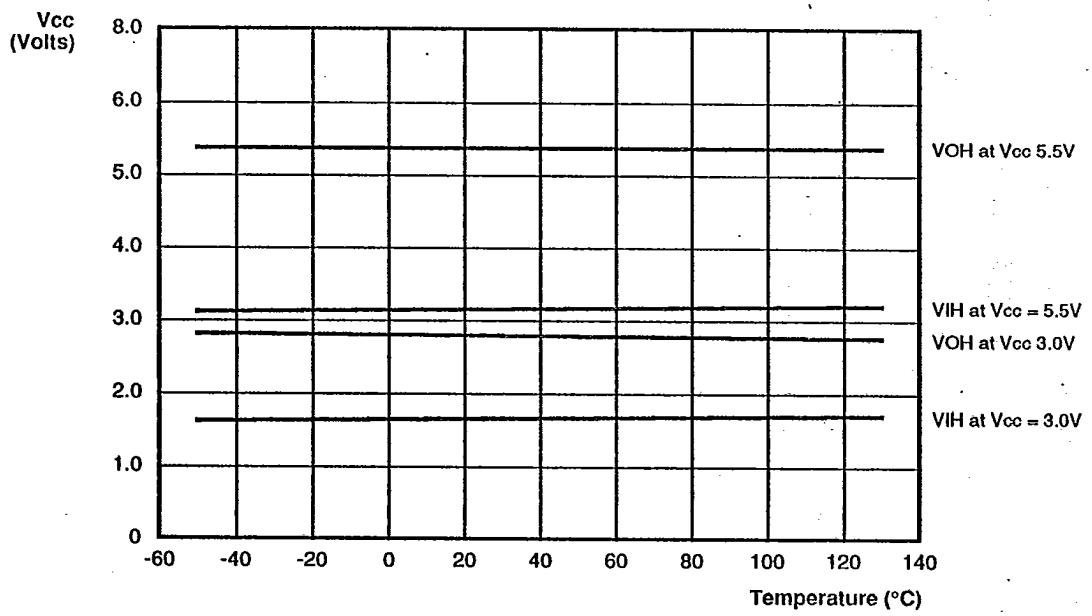
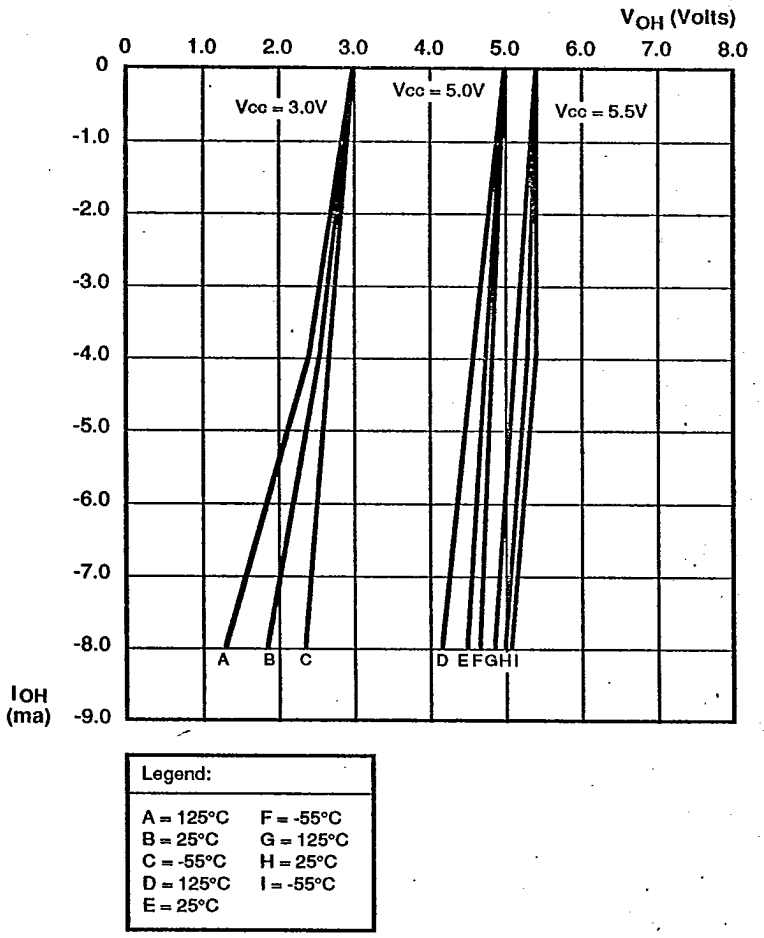


Figure 40. Typical V_{OH}, V_{IH} Vs Temperature



Legend:	
A = 125°C	F = -55°C
B = 25°C	G = 125°C
C = -55°C	H = 25°C
D = 125°C	I = -55°C
E = 25°C	

Figure 41. Typical V_{OH} Vs I_{OH} Over Temperature

DEVICE CHARACTERISTICS (Continued)
Graphs Illustrate Device Characteristics

T-49-19-07

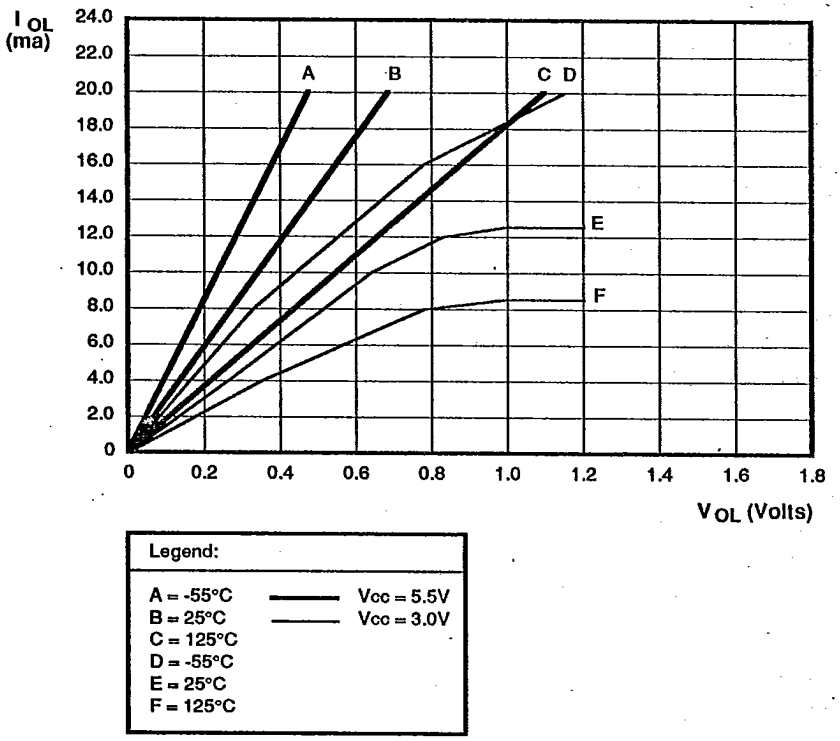
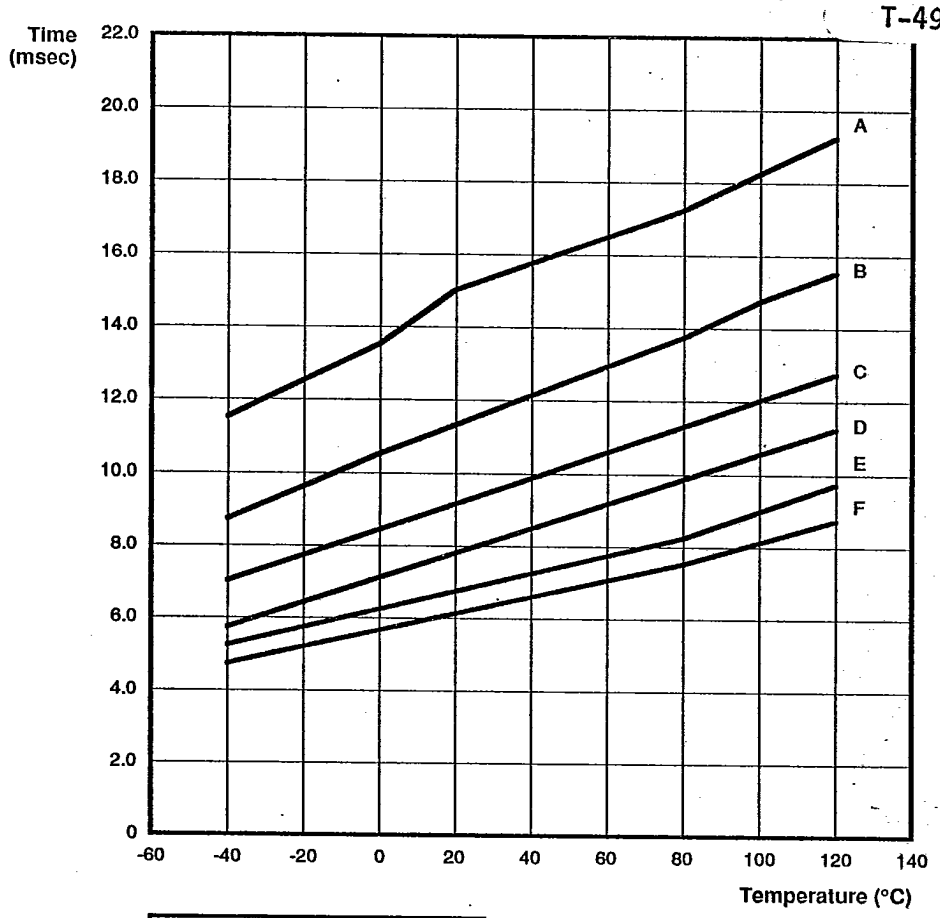


Figure 42. Typical I_{OL} Vs V_{OL} Over Temperature



Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5v
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 43. Typical Power-On Reset Time Vs Temperature

DEVICE CHARACTERISTICS (Continued)
Graphs Illustrate Device Characteristics

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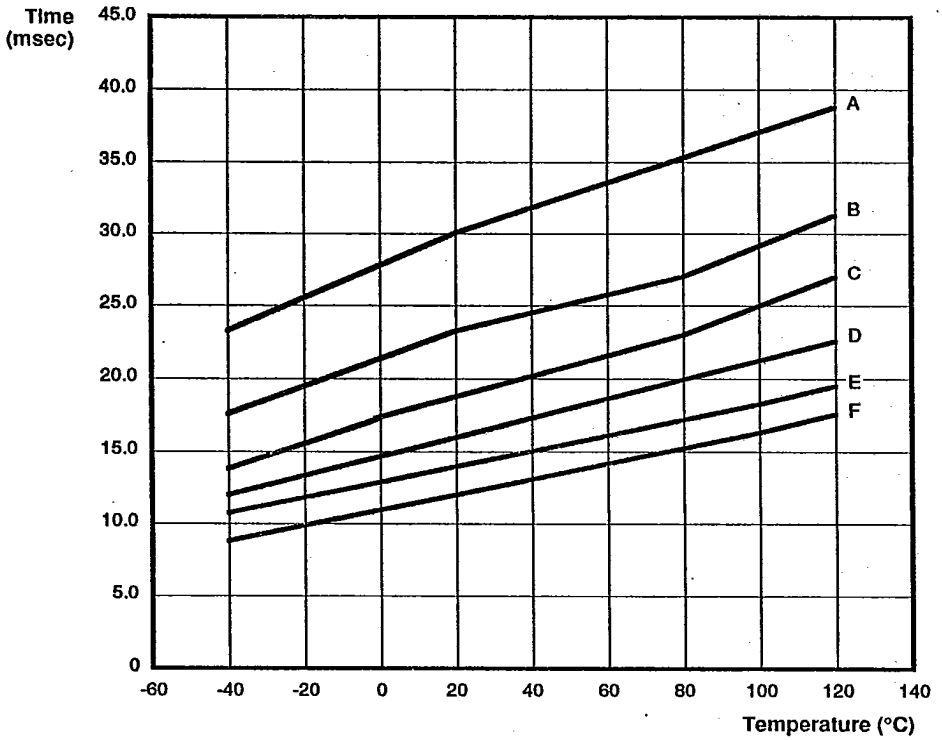

Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5v
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 44. Typical 5 ms WDT Setting Vs Temperature

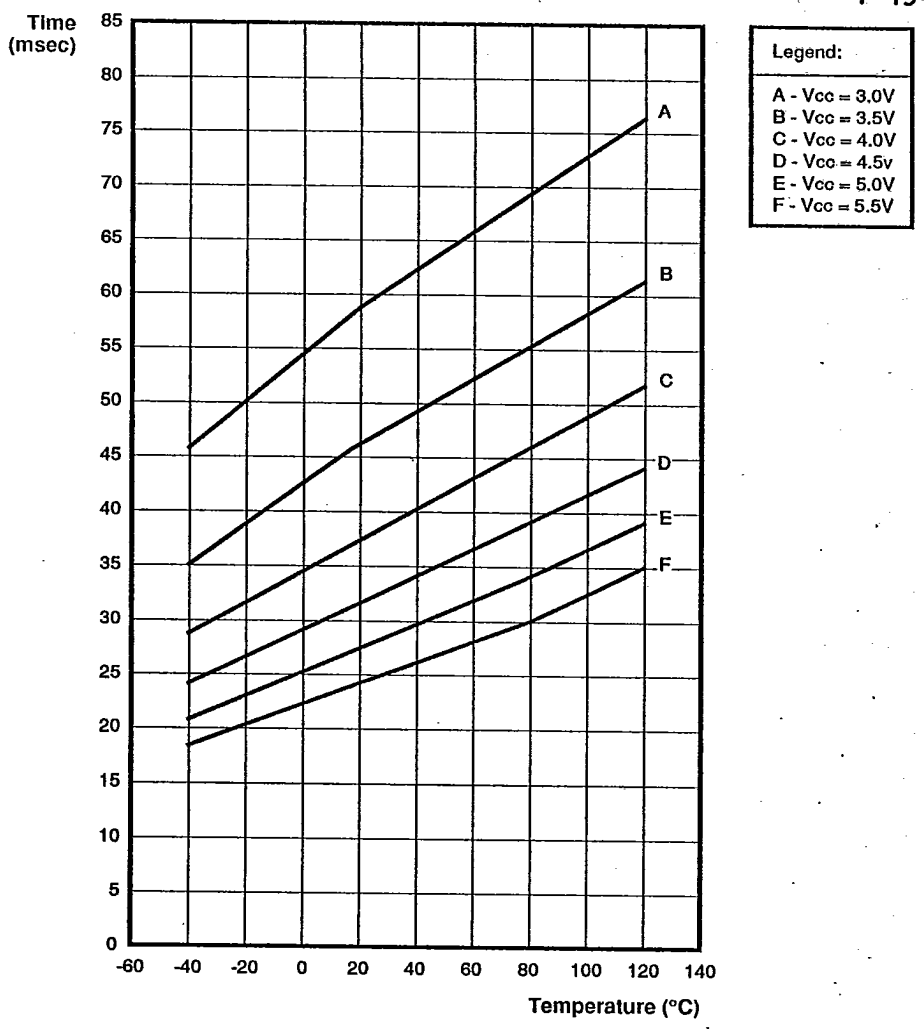

Figure 45. Typical 15 ms WDT Setting Vs Temperature

DEVICE CHARACTERISTICS (Continued)
Graphs Illustrate Device Characteristics

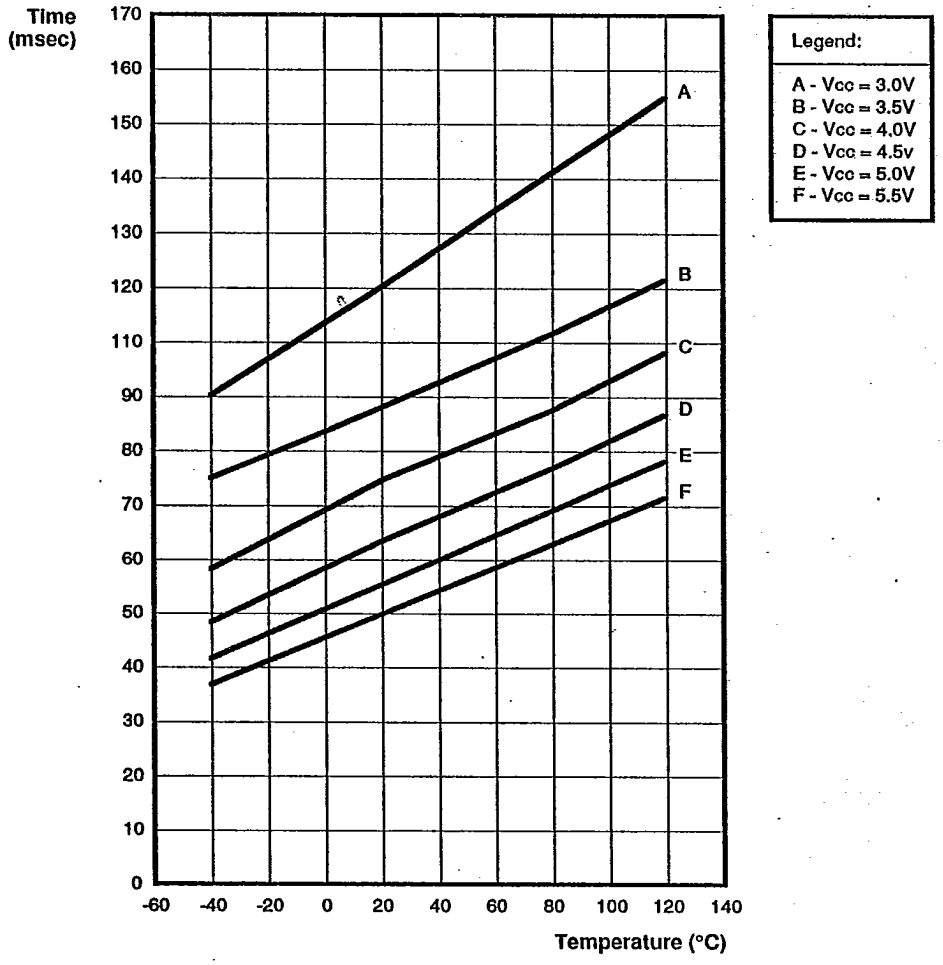

Figure 46. Typical 25 ms WDT Setting Vs Temperature

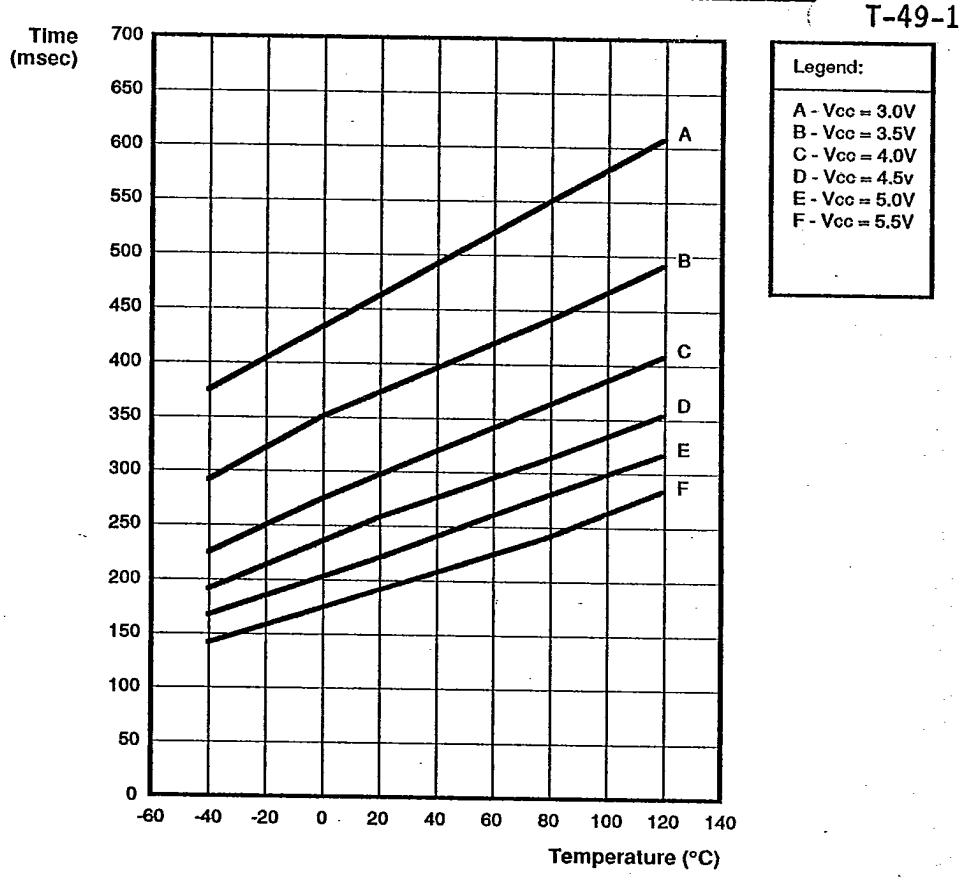

Figure 47. Typical 100 ms WDT Setting Vs Temperature

DEVICE CHARACTERISTICS (Continued)
Graphs Illustrate Device Characteristics

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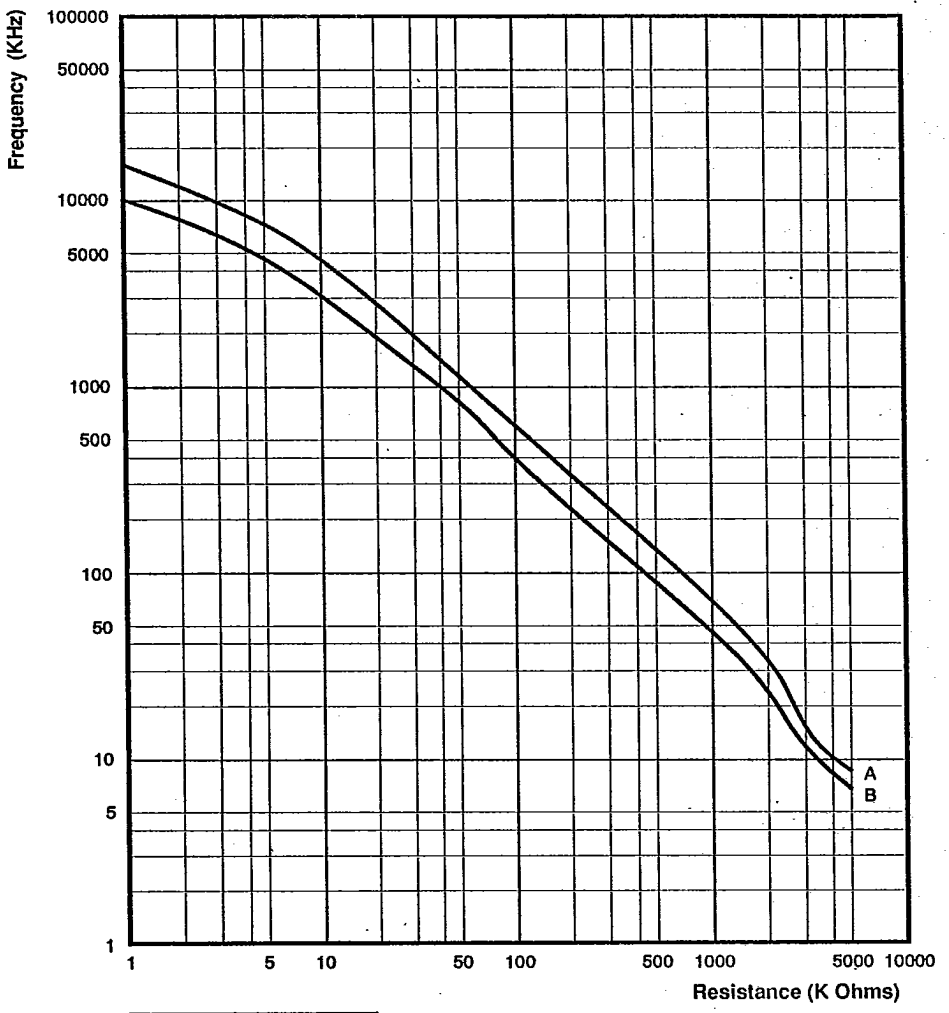
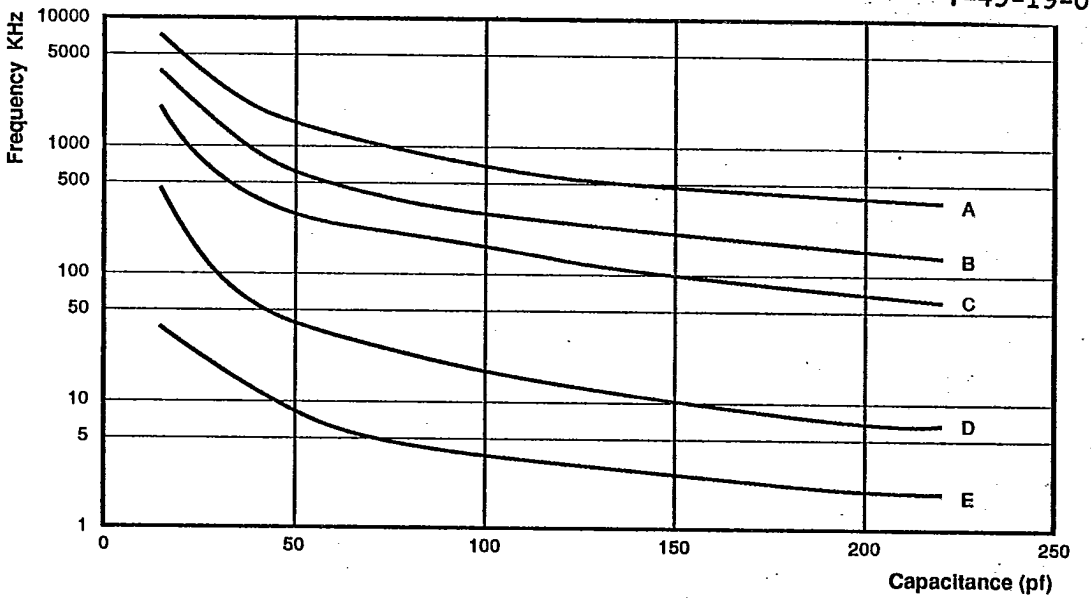


Legend:
A - Vcc = 5.0V C = 33pf B - Vcc = 3.3V C = 33pf

Note: This chart for reference only. Each process will have a different characteristc curve.

Figure 48. Typical Frequency Vs RC Resistance



Legend:
A - Vcc = 5.0V R = 22K Ohms
B - Vcc = 5.0V R = 56K Ohms
C - Vcc = 5.0V R = 100K Ohms
D - Vcc = 5.0V R = 1M Ohms
C - Vcc = 5.0V R = 4M Ohms

Figure 49. Typical RC Resistance/Capacitance Vs Frequency

DEVICE CHARACTERISTICS (Continued)
Graphs Illustrate Device Characteristics

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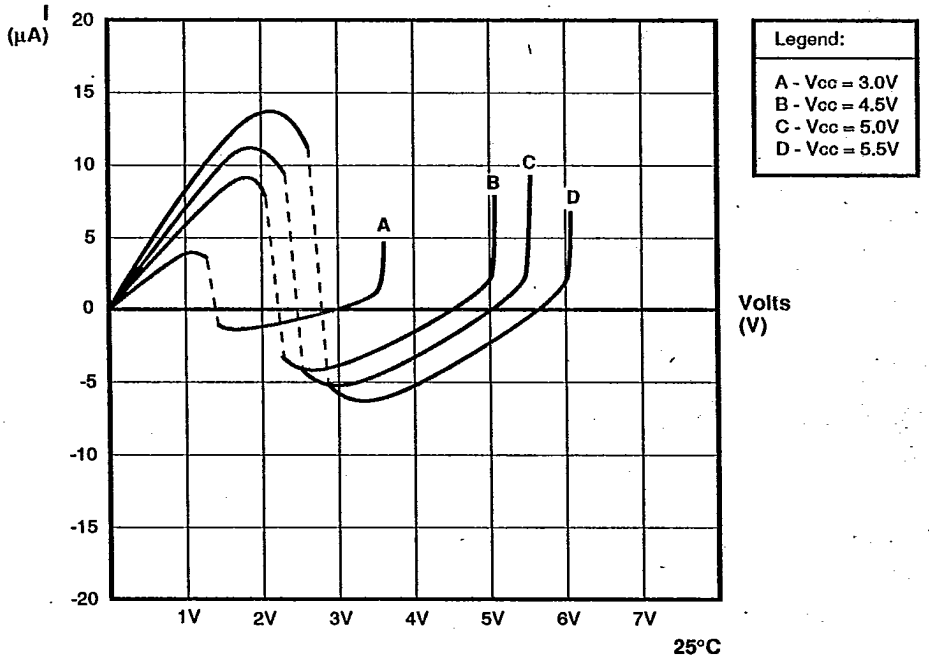

Figure 50. Auto Latch Characteristic

INSTRUCTION SET NOTATION

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Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flages are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

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Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS

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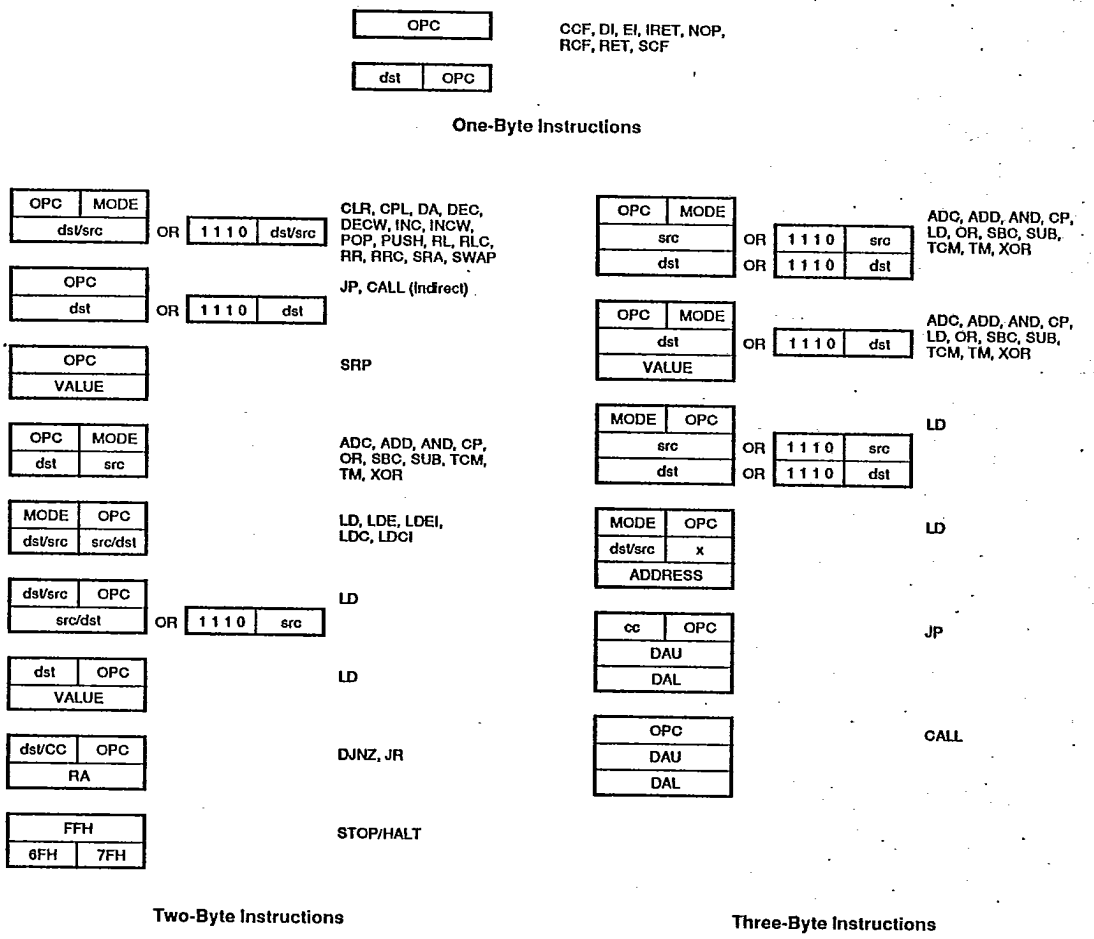

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

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Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	2	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

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Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst	R IR		90 91	*	*	*	*	-	-
RLC dst	R IR		10 11	*	*	*	*	-	-
RR dst	R IR		E0 E1	*	*	*	*	-	-
RRC dst	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

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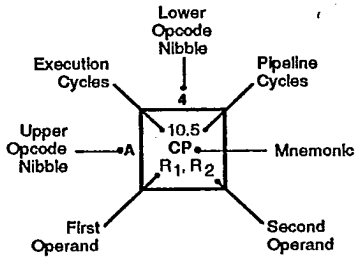
Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	6.5 ADD r1, Ir2	10.5 ADD R2, R1	10.5 ADD IR2, R1	10.5 ADD R1, IM	10.5 ADD IR1, IM	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/10.0 JR cc, RA	6.5 LD r1, IM	12.10.0 JP cc, DA	6.5 INC r1	
1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, IM	10.5 ADC IR1, IM								
2	6.5 INC R1	6.5 INC IR1	6.5 SUB r1, r2	6.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R1, IM	10.5 SUB IR1, IM								
3	8.0 JP IRR1	6.1 SRP IM	6.5 SBC r1, r2	6.5 SBC r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, IM	10.5 SBC IR1, IM								
4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, IM	10.5 OR IR1, IM								
5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, IM	10.5 AND IR1, IM								6.0 WDT
6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, IM	10.5 TCM IR1, IM								6.0 STOP
7	10/12.1 PUSH R2	12/14.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, IM	10.5 TM IR1, IM								7.0 HALT
8	10.5 DECW RR1	10.5 DECW IR1														6.1 DI
9	6.5 RL R1	6.5 RL IR1														6.1 EI
A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, IM	10.5 CP IR1, IM								14.0 RET
B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR IR2, R1	10.5 XOR R1, IM	10.5 XOR IR1, IM								16.0 IRET
C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2				10.5 LD r1,x,R2								6.5 RCF
D	6.5 SRA R1	6.5 SRA IR1			20.0 CALL* IRR1		20.0 CALL DA	10.5 LD r2,x,R1								6.5 SCF
E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, IR2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, IM	10.5 LD IR1, IM								6.5 CCF
F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2		10.5 LD R2, IR1										6.0 NOP
Bytes per Instruction	2			3					2				3		1	



Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank are not defined.

* 2-byte instruction appears as a 3-byte instruction