PRODUCT SPECIFICATION

Z86C90/C89

ROMLESS CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-bit CMOS microcomputer
- 40- or 44-pin package
- Low cost
- 3.0 to 5.5 volt operating range
- Low power consumption - 50 mW (Typical)
- Fast instruction pointer - 1.0 microsecond @ 12 MHz
- Two standby modes - STOP and HALT
- 32 input/output lines (two with comparator inputs)
- All digital inputs are CMOS levels, Schmitt triggered
- ROMless
- 256 bytes of RAM (236 for general purpose)
- Two Expanded Register File control registers
- Two programmable 8-bit Counter/Timers
- 6-bit programmable prescaler
- Six vectored, priority interrupts from six different sources
- Clock speeds 8 and 12 MHz
- Brown-Out protection
- Programmable Watch Dog/Power-On Reset Timer
- Two Comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, or external clock drive (Z86C90).
- On-chip oscillator that accepts an RC network or external clock drive (Z86C89).

GENERAL DESCRIPTION

The Z86C90/C89 CCP™ (Consumer Controller Processor) introduces a new level of sophistication to single-chip architecture. The Z86C90/C89 are ROMless members of the Z8 single-chip microcontroller family with 236 bytes of general purpose RAM. The only difference that exists between the Z86C89 and the Z86C90 is that the on-chip oscillator of the Z86C89 can accept an external RC network or other external clock source, while the Z86C90's on-chip oscillator accepts a crystal, ceramic resonator, LC, or external clock source drive. The CCP controllers are housed in a 40-pin DIP, 44-pin Leaded Chip Carrier, or a 44-pin Quad Flat Pack, and are CMOS compatible. The CCP offers the use of external memory which enables this Z8 microcomputer to be used where code flexibility is required. Zilog's CMOS microcomputer offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C90/C89 architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial, automotive, computer peripherals, and advanced scientific applications.

The CCP applications demand powerful I/O capabilities. The Z86C90/C89 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

There are four basic address spaces available to support this wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File. The Register File is composed of 236 bytes of general purpose registers, four I/O port registers, and fifteen control and status registers. The Expanded Register File consists of two control registers.

To unburden the program from coping with the real-time problems, such as counting/timing and data communication, the Z86C90/C89 offers two on-chip counter/timers. Included are a large number of user selectable modes, and two on-board comparators to process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only); /N//S (NORMAL and SYSTEM are both active Low).

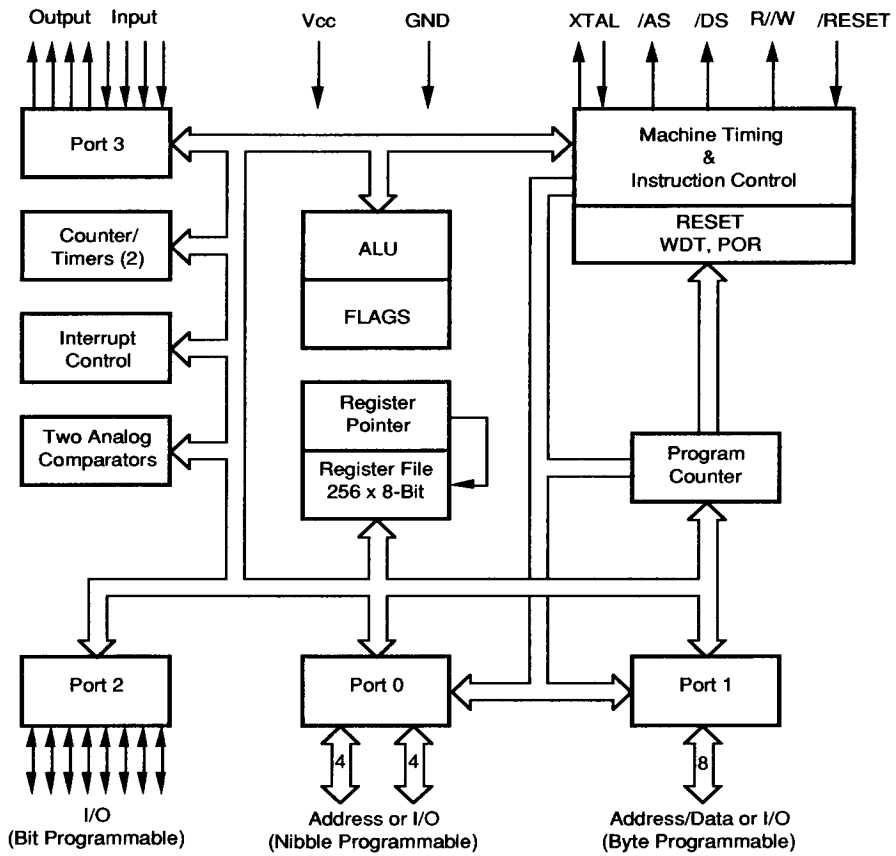


Figure 1. Functional Block Diagram

PIN DESCRIPTION

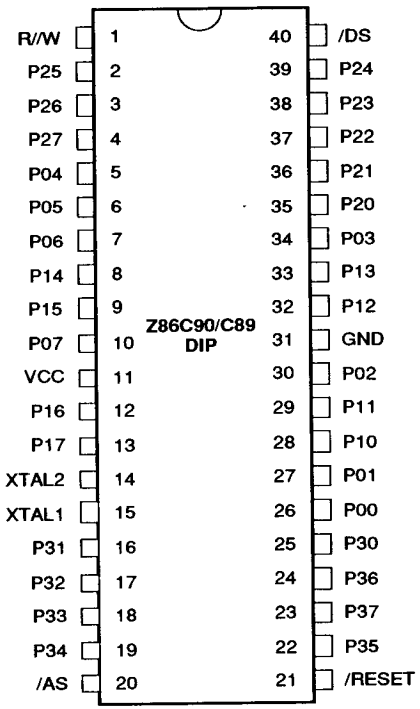


Figure 2. 40-Pin Dual-In-Line Pin Assignments

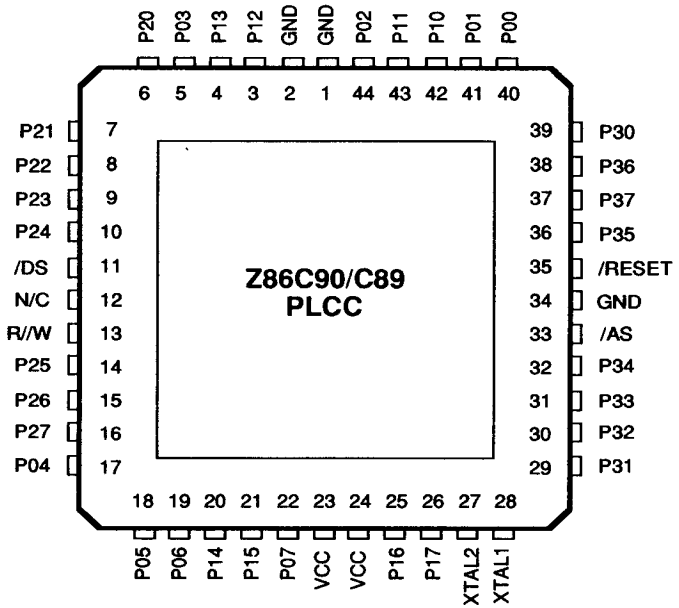


Figure 3. 44-Pin Leaded Chip Carrier Pin Assignments

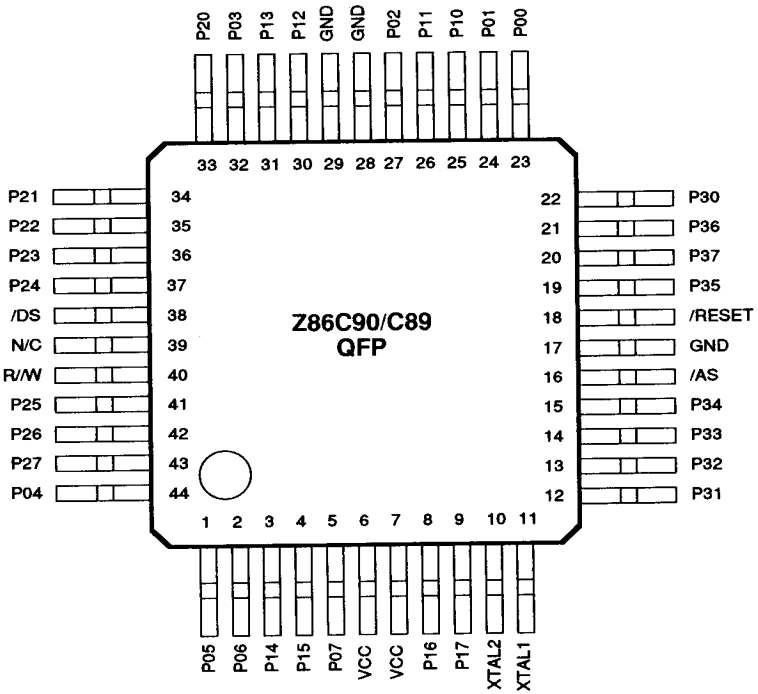


Figure 4. 44-Pin Quad Flat Pack Pin Assignments

PIN DESCRIPTION (Continued)

Table 1. 40-Pin Dual-In-Line Pin Identification

Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-27	Port 2 pin 5,6,7	In/Output
5-7	P04-P06	Port 0 pin 4,5,6	In/Output
8-9	P14-P15	Port 1 pin 4,5	In/Output
10	P07	Port 0 pin 7	In/Output
11	V_{cc}	Power Supply	Input
12-13	P16-P17	Port 1 pin 6,7	In/Output
14	XTAL2	Crystal, Oscillator Clock	Output
15	XTAL1	Crystal, Oscillator Clock	Input
16-18	P31-P33	Port 3 pin 1,2,3	Input
19	P34	Port 3 pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3 pin 5	Output
23	P37	Port 3 pin 7	Output
24	P36	Port 3 pin 6	Output
25	P30	Port 3 pin 0	Input
26-27	P00-P01	Port 0 pin 0,1	In/Output
28-29	P10-P11	Port 1 pin 0,1	In/Output
30	P02	Port 0 pin 2	In/Output
31	GND	Ground	Input
32-33	P12-P13	Port 1 pin 2,3	In/Output
34	P03	Port 0 pin 3	In/Output
35-39	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

Table 2. 44-Pin Leaded Chip Carrier Pin Identification

Pin #	Symbol	Function	Direction
1-2	GND	Ground	Input
3-4	P12-P13	Port 1 pin 2,3	In/Output
5	P03	Port 0 pin 3	In/Output
6-10	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	N/C	Not Connected	Input
13	R//W	Read/Write	Output
14-16	P25-27	Port 2 pin 5,6,7	In/Output
17-19	P04-P06	Port 0 pin 4,5,6	In/Output
20-21	P14-P15	Port 1 pin 4,5	In/Output
22	P07	Port 0 pin 7	In/Output
23-24	V_{cc}	Power Supply	Input
25-26	P16-P17	Port 1 pin 6,7	In/Output
27	XTAL2	Crystal, Oscillator Clock	Output
28	XTAL1	Crystal, Oscillator Clock	Input
29-31	P31-P33	Port 3 pin 1,2,3	Input
32	P34	Port 3 pin 4	Output
33	/AS	Address Strobe	Output
34	GND	Ground	Input
35	/RESET	Reset	Input
36	P35	Port 3 pin 5	Output
37	P37	Port 3 pin 7	Output
38	P36	Port 3 pin 6	Output
39	P30	Port 3 pin 0	Input
40-41	P00-P01	Port 0 pin 0,1	In/Output
42-43	P10-P11	Port 1 pin 0,1	In/Output
44	P02	Port 0 pin 2	In/Output

PIN DESCRIPTION (Continued)

Table 3. 44-Pin Quad Flat Pack Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-P06	Port 0 pin 5,6	In/Output
3-4	P14-P15	Port 1 pin 4,5	In/Output
5	P07	Port 0 pin 7	In/Output
6-7	V_{cc}	Power Supply	Input
8-9	P16-P17	Port 1 pin 6,7	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output
11	XTAL1	Crystal, Oscillator Clock	Input
12-14	P31-P33	Port 3 pin 1,2,3	Input
15	P34	Port 3 pin 4	Output
16	/AS	Address Strobe	Output
17	GND	Ground	Input
18	/RESET	Reset	Input
19	P35	Port 3 pin 5	Output
20	P37	Port 3 pin 7	Output
21	P36	Port 3 pin 6	Output
22	P30	Port 3 pin 0	Input
23-24	P00-P01	Port 0 pin 0,1	In/Output
25-26	P10-P11	Port 1 pin 0,1	In/Output
27	P02	Port 0 pin 2	In/Output
28-29	GND	Ground	Input
30-31	P12-P13	Port 1 pin 2,3	In/Output
32	P03	Port 0 pin 3	In/Output
33-37	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	N/C	Not Connected	Input
40	R//W	Read/Write	Output
41-43	P25-27	Port 2 pin 5,6,7	In/Output
44	P04	Port 0 pin 4	In/Output

PIN FUNCTIONS

/DS. *(output, active Low).* Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS. *(output, active Low).* Address Strobe is pulsed once at the beginning of each machine cycle. Address output is via Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/W. *(output, write Low).* Read/Write, the R/W signal is low when the CCP is writing to the external program or data memory.

Port 0 (P00-P07). Port 0 is an 8-bit, bidirectional, CMOS compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt triggered and the output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction to Port 0 of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode.

Port 0 is set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals /AS, /DS and R/W (Figure 5).

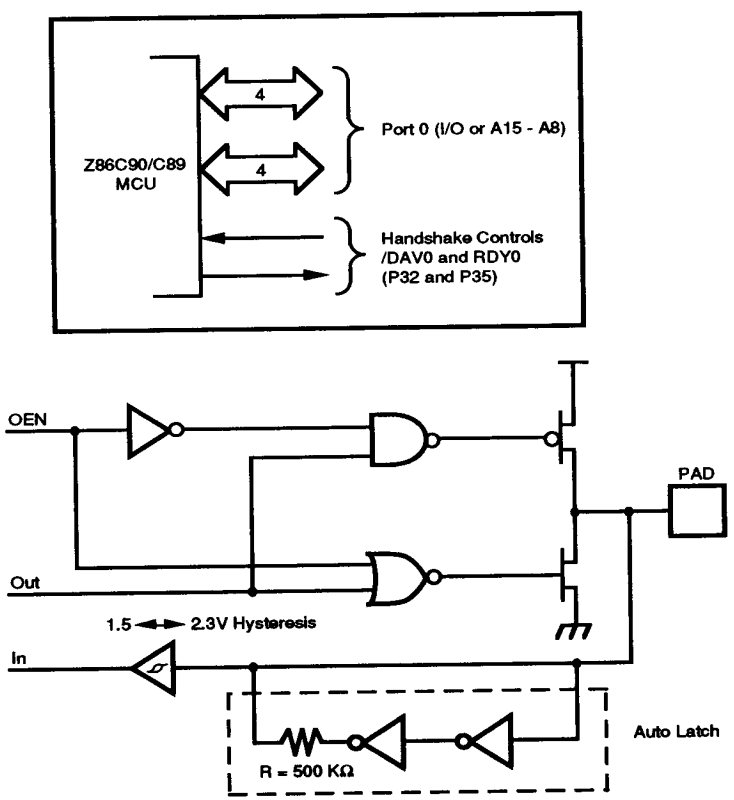


Figure 5. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P10-P17). Port 1 is a multiplexed Address (A7-A0) and Data (D7-D0), CMOS compatible port. Port 1 is dedicated to the Zilog ZBUS®-compatible memory interface. The operations of Port 1 are supported by the Address Strobe (/AS) and Data Strobe (/DS) lines, and by the Read/Write (R//W) and Data Memory (/DM) control lines. Data memory read/write operations are done through this port (Figure 6). If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS and R//W, allowing the Z86C90/C89 to share common resources in multiprocessor and DMA applications.

The CCP wakes up with the 8 bits of Port 1 configured as address outputs for external memory.

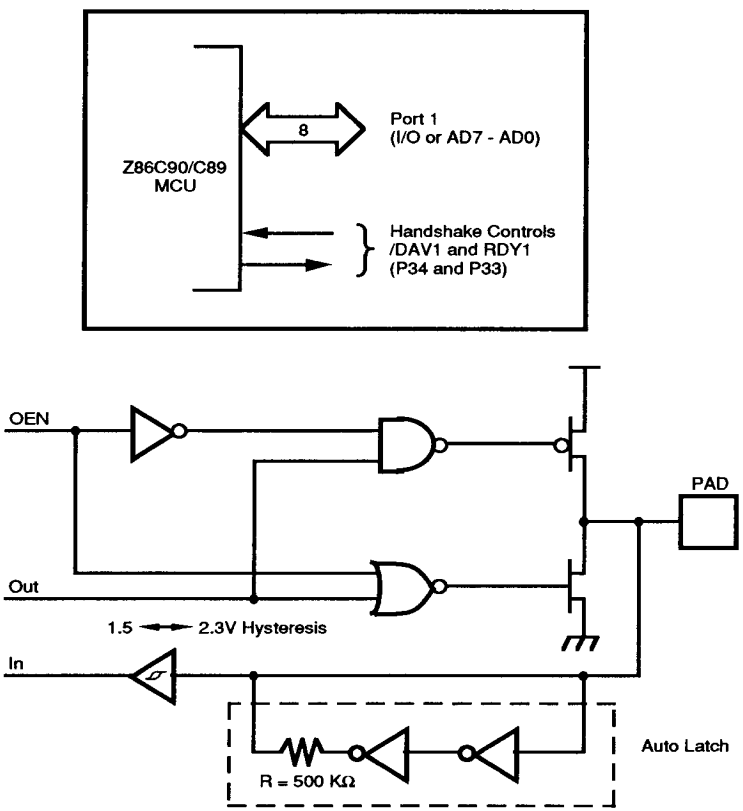


Figure 6. Port 1 Configuration

Port 2 (P20-P27). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt triggered. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 may be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to bit-7 Port 2 (Figure 7).

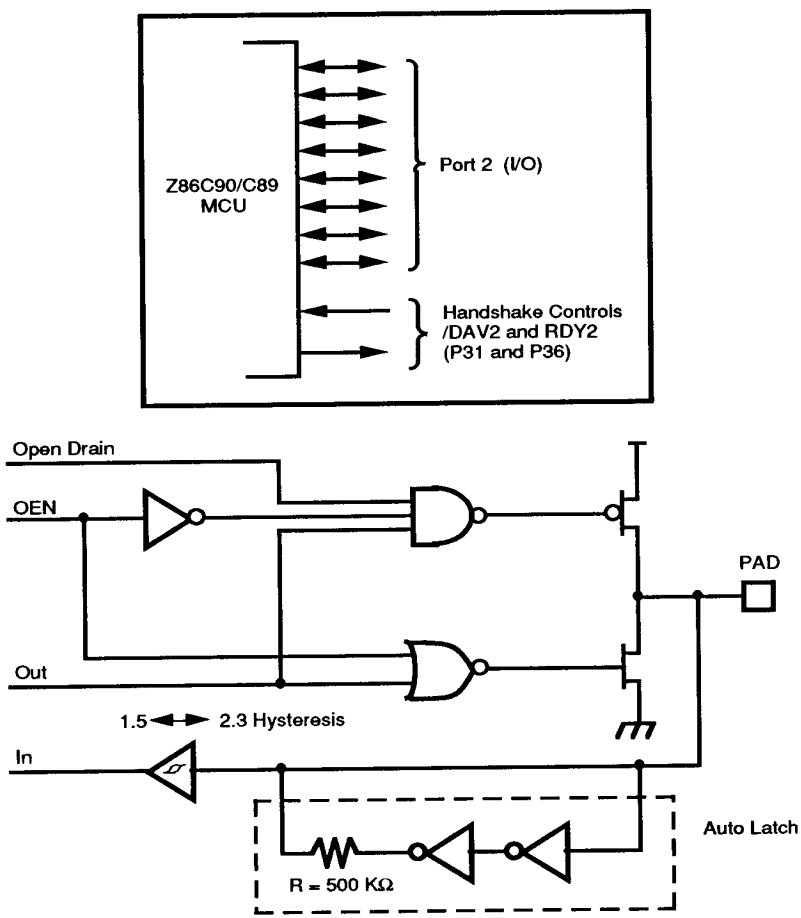


Figure 7. Port 2 Configuration

Port 3 (P30-P37). Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output. Port 3 consists of four-fixed input (P30-P33) and four-fixed output (P34-P37), and can be configured under software control for Input/Output, Counter/Timers, interrupt, Port handshake and Data Memory functions. Port 3, Pin-0 input is Schmitt triggered, and pins P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming the Port 3 Mode Register (bit-1). Port 3, pins 0 and 3 are falling edge interrupt inputs. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines Ports 0, 1 and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}) and Data Memory Select [(/DM) (Figure 8)].

Auto-Latch. The Auto-Latch puts valid CMOS levels on all CMOS inputs (except P31-P33) that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

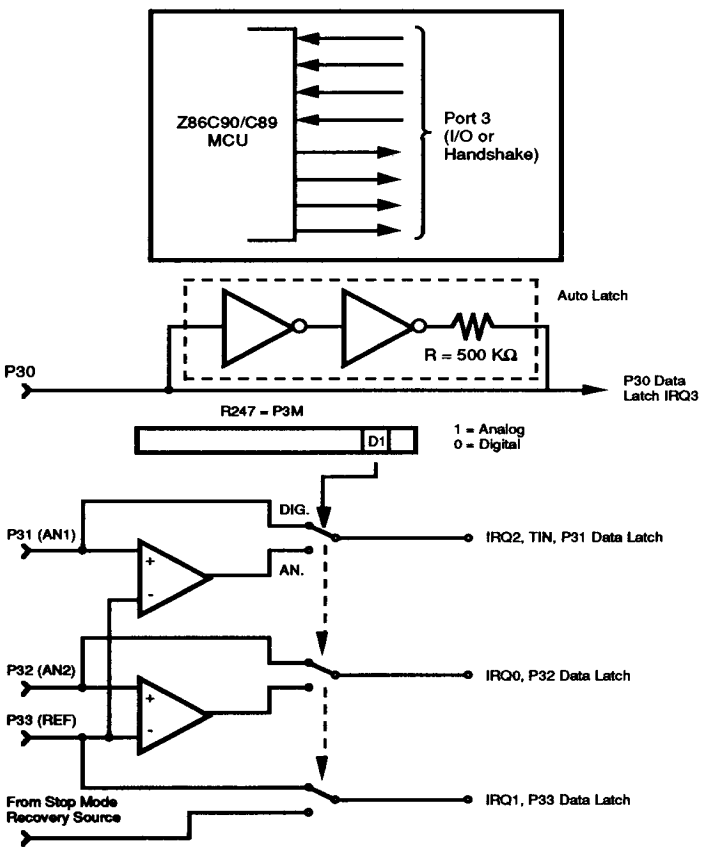


Figure 8. Port 3 Configuration

Table 4. Pin Assignments

Pin	I/O	CTC1	AN IN	Int.	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT					R/D		DM
P35	OUT				R/D			
P36	OUT	T_{OUT}					R/D	
P37	OUT							

Notes:
HS = Handshake Signals
D = DAV
R = RDY

Comparator Inputs. Port 3, Pins P31 and P32 each have a comparator front end. The comparator reference voltage (Pin P33) is common to both comparators. In analog mode, P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, Pin P33 can be used as a P33 register input or IRQ1 source.

/RESET. *(input, active-Low).* Initializes the MCU. Reset is accomplished either through Power-On, Watch Dog Timer reset, STOP Mode Recovery, or external reset. During Power-On Reset and Watch Dog Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line should be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

After the POR time, /RESET is a Schmitt triggered input. To avoid asynchronous and noisy reset problems, the Z86C90/C89 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active low while /AS cycles at a rate of TpC/2. Program execution begins at location 000C (HEX), 5-10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms. The Z86C90/C89 does not reset WDTMR, SMR, P2M, or P3M registers on a STOP Mode Recovery operation.

FUNCTIONAL DESCRIPTION

The Z8 CCP incorporates special functions to enhance the Z8's functionality in industrial, scientific research and advanced technologies applications.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP Mode Recovery Source
- Brown-out Recovery
- External Reset

Program Memory. The Z86C90/C89 addresses up to 64K external program memory (Figure 9). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at location 000C (HEX) after a reset.

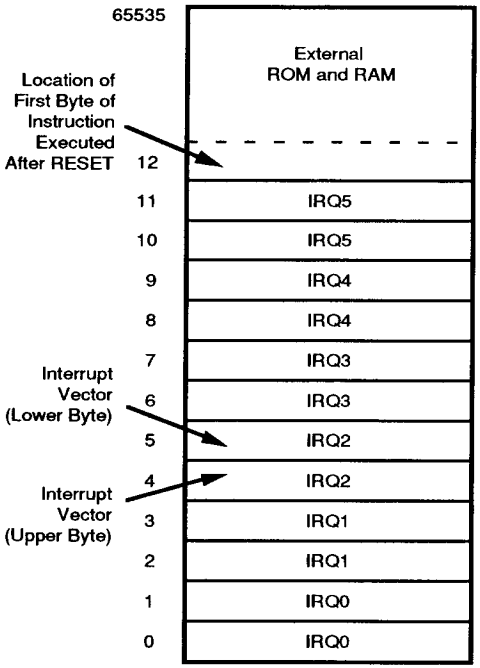


Figure 9. Program Memory Map

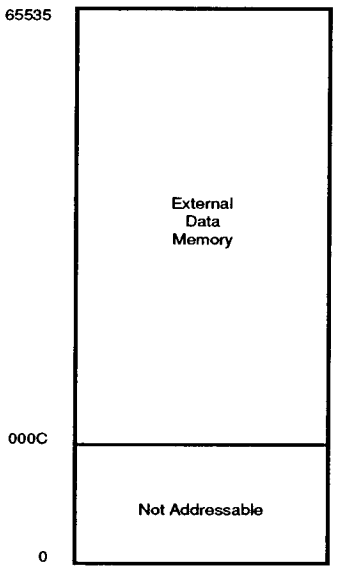


Figure 10. Data Memory Map

Data Memory. *(/DM).* The Z86C90/C89 ROMless version addresses up to 64K bytes of external data memory beginning at location 000CH (Figure 10). External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that is programmed to appear on pin P34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory.

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group (Figure 11). These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 12). Two system configuration registers reside in the Expanded Register File at Bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion.

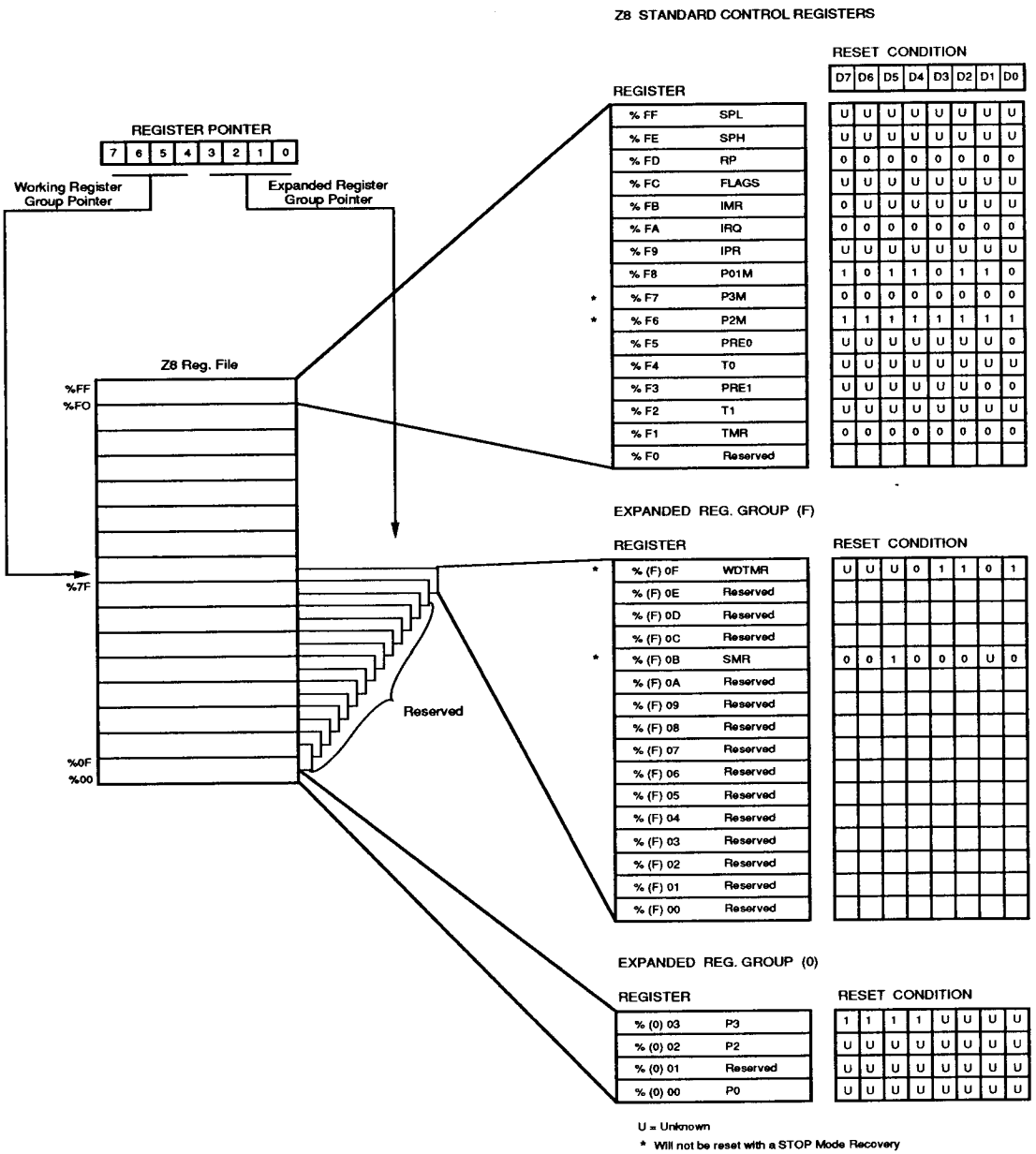


Figure 11. Expanded Register File Architecture

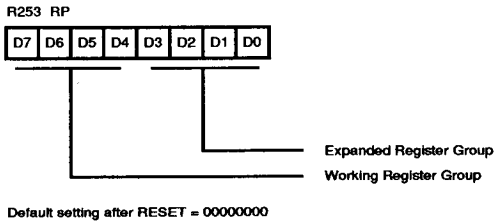


Figure 12. Register Pointer Register

Register File. The register file consists of four I/O port registers, 236 general purpose registers and 15 control and status registers (R0-R3, R4-239 and R240-R255, respectively), plus two system configuration registers in the expanded register group. The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 13). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Register Bank E0-EF is only accessed through working registers and indirect addressing modes.

Stack. The Z86C90/C89 external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack residing anywhere in the data memory for ROMless mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general purpose registers (R4-R239). SPH is used as a general purpose register only when using internal stacks.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 14).

The 6-bit prescaler divides the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

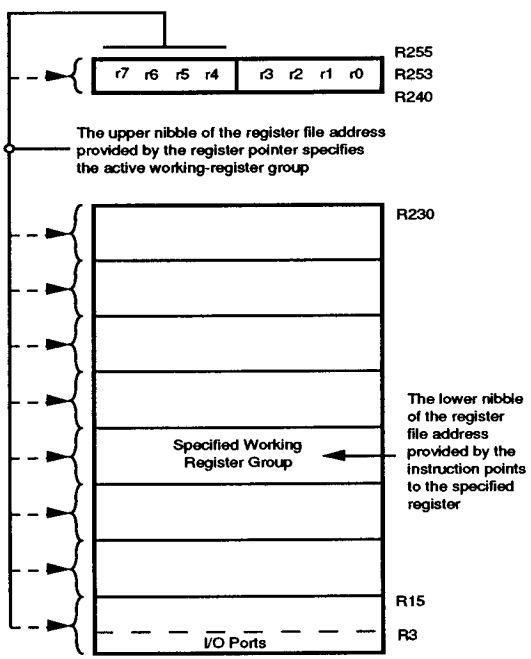


Figure 13. Register Pointer

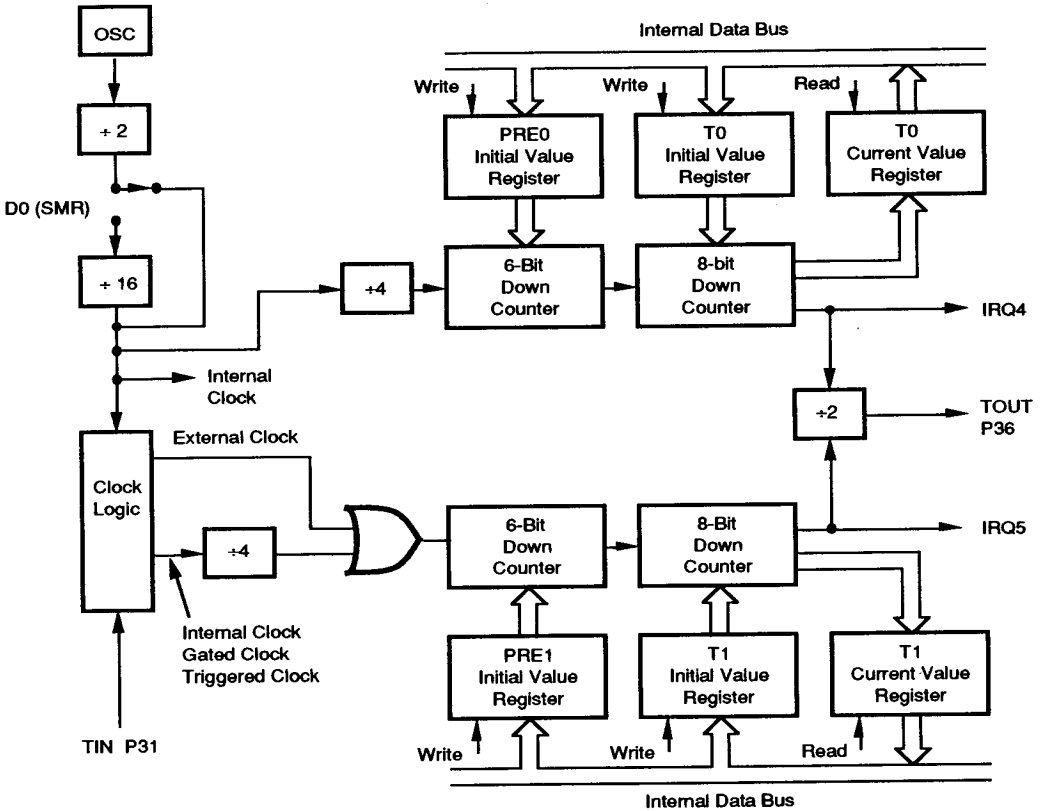


Figure 14. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C90/C89 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 15). The six sources are divided as follows; four sources are claimed by Port 3 lines P30-P33, and two in counter/timers (Table 5). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

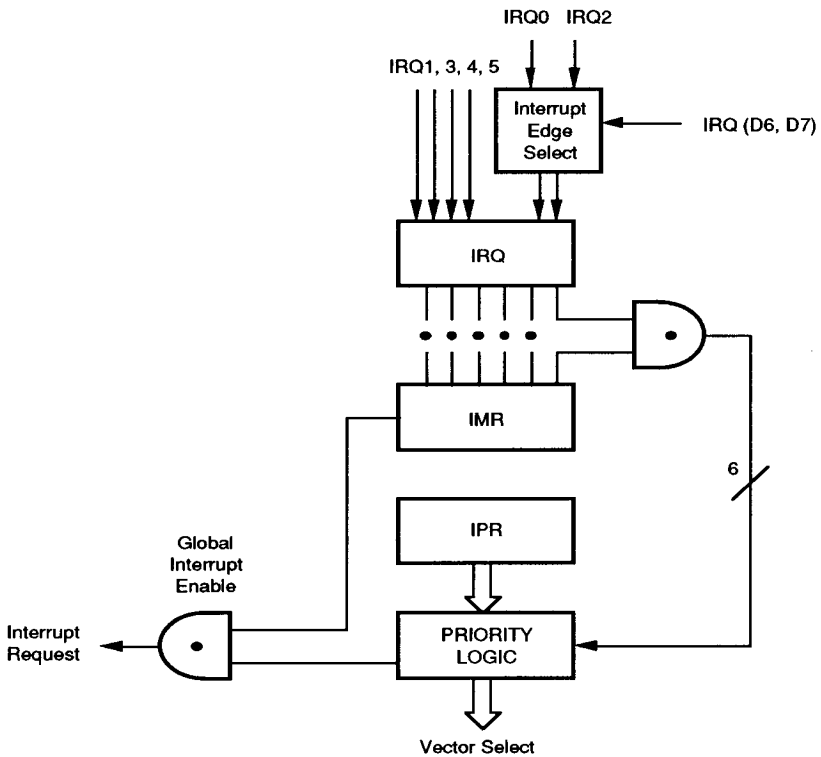


Figure 15. Interrupt Block Diagram

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	/DAV 0, IRQ 0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ 1,	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	/DAV 2, IRQ 2, T_{IN}	4, 5	External (P31), Rising Falling Edge Triggered
IRQ 3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ 4	T0	8, 9	Internal
IRQ 5	TI	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. Thus, this disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86C90/C89 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 6.

Table 6. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F=Falling Edge
R=Rising Edge

Clock. The Z86C90 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 12 MHz max., with a series resistance (RS) less than or equal to 100 Ohms. The Z86C89 on-chip oscillator may be driven with a low cost RC network or other suitable external clock source. (Note: The RC option is not available in the 12 MHz part).

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance is more than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 16). See Figures 52-54 for typical characteristics.

Power-On-Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. STOP mode recovery (if D5 of SMR=1).
3. WDT timeout.

The POR time is a nominal 5 ms. Bit-5 of the Stop Mode Register determines whether the POR timer is bypassed after STOP mode recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3, remain active. The devices are recovered by interrupts, either externally or internally generated.

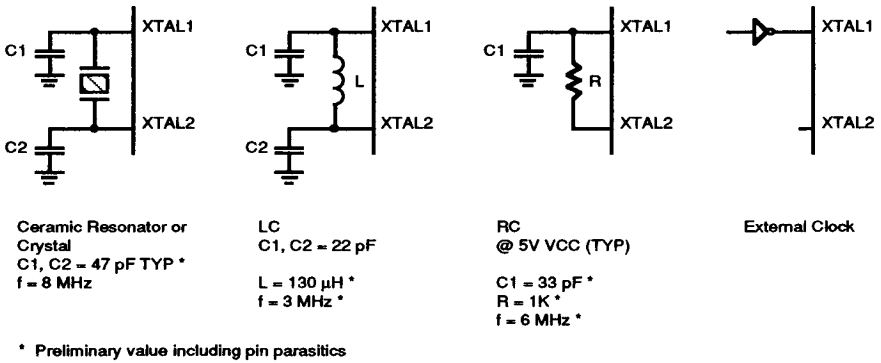


Figure 16. Oscillator Configuration

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. The STOP Mode is terminated by a reset only, either by WDT timeout, POR, SMR recovery or external reset. This causes the processor to restart the application program at address 000C (HEX). In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF    NOP     ; clear the pipeline
6F    STOP    ; enter STOP mode
              or
FF    NOP     ; clear the pipeline
7F    HALT    ; enter HALT mode
```

Stop Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP Mode Recovery (Figure 17). All bits are write only, except Bit 7 which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the STOP Mode Recovery signal. Bits 0 and 1 determine the timeout period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address OBH.

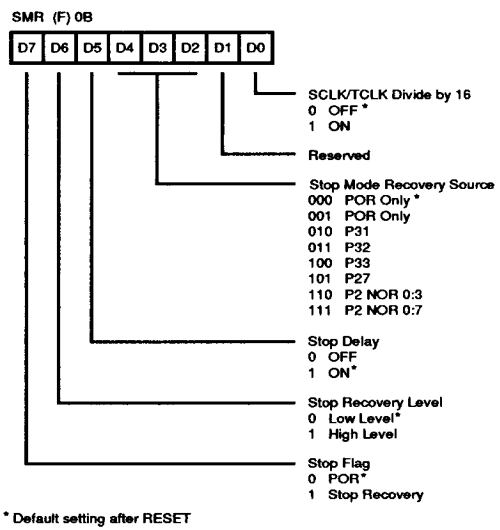


Figure 17. STOP Mode Recovery Register

SCLK/TCLK divide-by-16 Select (D0). D0 of the SMR control a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

STOP Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake up source of the STOP recovery (Figure 18 and Table 7).

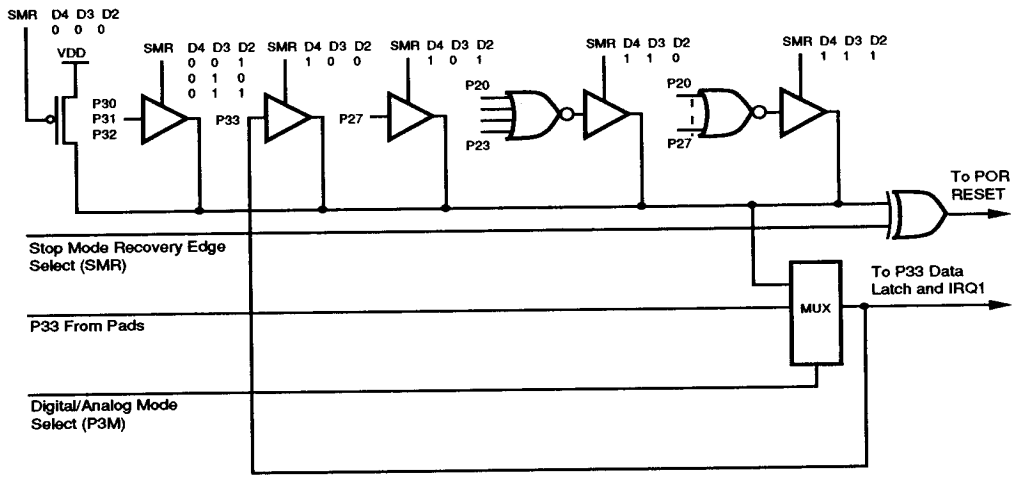


Figure 18. STOP Mode Recovery Source

Table 7. STOP Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

STOP Mode Recovery Delay Select (D5). This bit, if high, disables the 5 ms /RESET delay after STOP Mode Recovery. The default configuration of this bit is one. If the "fast" wake up is selected, the STOP Mode Recovery source needs to be kept active for at least 5 TpC.

STOP Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z86C90/C89 from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 18).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit (cold) indicates that the device will be reset by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

Watch-Dog-Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figures 19 and 20).

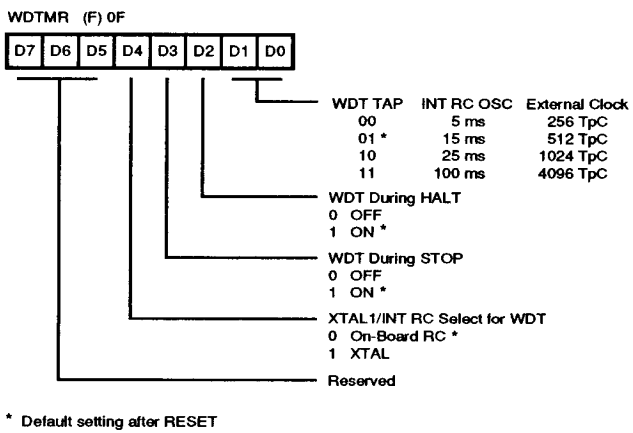


Figure 19. Watch-Dog Timer Mode Register

WDT Time Select (D0,D1). Selects the WDT time period. It is configured as shown in Table 8.

Table 8. WDT Time Select

D1	D0	Timeout of internal RC OSC	Timeout of XTAL clock
0	0	5 ms min	256TpC
0	1	15 ms min	512TpC
1	0	25 ms min	1024TpC
1	1	100 ms min	4096TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms.
See Figures 55 to 58 for details.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Clock source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

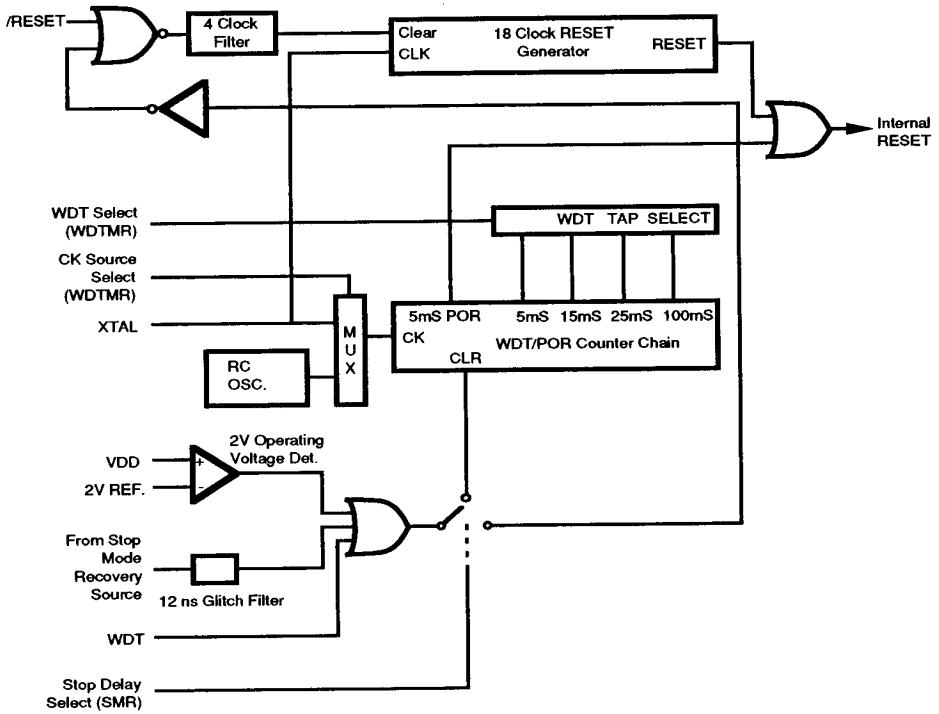


Figure 20. Resets and WDT

Brown-Out Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{BO} (Brown-Out Voltage). The minimum operating voltage varies with the temperature and operating frequency, while V_{BO} varies with temperature only.

The brown-out trip voltage (V_{BO}) is less than 3 volts and above 1.4 volts under the following conditions.

Maximum (V_{BO}) Conditions:

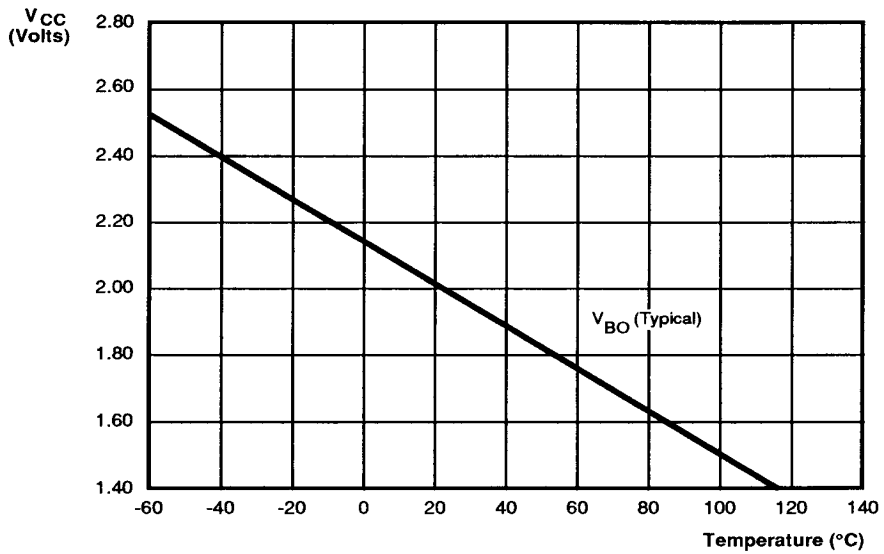
Case 1 T_A = -40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

Case 2 T_A = -40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency is one-half the external clock frequency.

FUNCTIONAL DESCRIPTION (Continued)

The device functions normally at or above 3.0 V under all conditions. Below 3.0 V, the device functions normally until the Brown-Out Protection trip point is reached, below which reset is globally driven. The device is guaranteed to function normally at supply voltages above the brown out trip point for the temperatures and operating frequencies in cases 1 and 2. The actual brown out trip point is a function of temperature and process parameters (Figure 21).



* Power-on Reset threshold for V_{CC} and 4 MHz V_{BO} overlap

Figure 21. Typical Z86C90/C89 Brown-Out Voltage vs Temperature at 4 MHz

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 22).

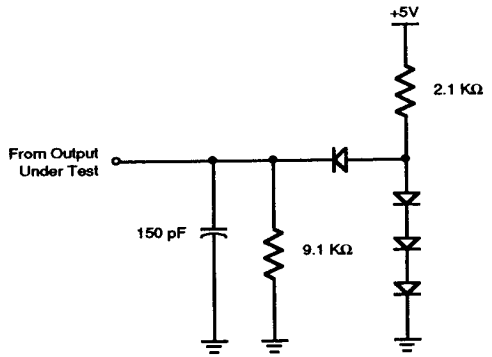


Figure 22. Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	-0.3	+7.0	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins to GND

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0°C to 70°C Min	Max	T_A = -40° C to 105° C Min	Max	Typ @ 25°C	Units	Conditions	Notes
	Max Input Voltage	3.3V		7		7		V	I_{IN} 250µA	
		5.0V		7		7		V	I_{IN} 250µA	
V_{CH}	Clock Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.3V	GND -0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.3V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V		
		5.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltge	3.3V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	
V_{OL1}	Output Low Voltage	3.3V		0.6		0.6	0.2	V	I_{OH} = +4.0 mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.3V		1.2		1.2	0.3	V	I_{OL} = +6 mA, 3 Pin Max	
		5.0V		1.2		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max	
V_{RH}	Reset Input	3.3V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V		
	High Voltage	5.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input	3.3V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1			
	Low Voltage	5.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.7			
V_{OFFSET}	Comparator Input	3.3V		25		25	10	mV		
	Offset Voltage	5.0V		25		25	10	mV		
I_{IL}	Input Leakage	3.3V	-1	1	-1	2	< 1	µA	V_{IN} = 0V, V_{CC}	
		5.0V	-1	1	-1	2	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.3V	-1	1	-1	2	< 1	µA	V_{IN} = 0V, V_{CC}	
		5.0V	-1	1	-1	2	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.3V		-45		-60	-20	µA		
		5.0V		-55		-70	-30	µA		
I_{CC}	Supply Current	3.3V		10		10	4	mA	@ 8 MHz	[4,5]
		5.0V		15		15	10	mA	@ 8 MHz	[4,5]
		3.3V		15		15	5	mA	@ 12 MHz	[4,5]
		5.0V		20		20	15	mA	@ 12 MHz	[4,5]

Sym	Parameter	V_{CC} Note [3]	T_A = 0°C to 70°C Min	Max	T_A = -40° C to 105° C Min	Max	Typ @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	3.3V		3		3	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4,5]
		5.0V		5		5	2.4	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4,5]
		3.3V		4		4	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		5.0V		6		6	3.2	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		3.3V		2		2	0.8	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		5.0V		4		4	1.8	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		3.3V		3		3	1.2	mA	Clock Divide by 16 @ 12 MHz	[4,5]
		5.0V		5		5	2.5	mA	Clock Divide by 16 @ 12 MHz	[4,5]
I_{CC2}	Standby Current	3.3V		8		15	1	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		5.0V		10		20	2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		3.3V		500		600	310	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6]
		5.0V		800		1000	600	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	
I_{ALL}	Auto Latch Low Current	3.3V		8		10	5	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		15		20	11	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.3V		-5		-7	-3	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		-8		-10	-6	µA	$0V < V_{IN} < V_{CC}$	
I_{POR}	Power On Reset	3.3V	7	24	7	25	13	ms		
		5.0V	3	13	3	14	7	ms		
V_{BO}	V_{CC} Brown-Out Voltage		1.5	2.65	1.2	2.95	2.1	V	2 MHz max Ext. CLK Freq.	[7]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Frequency
Crystal/Resonator	3.0 mA	5	mA	8 MHz
External Clock Drive	0.3 mA	5	mA	8 MHz

[2] GND=0V

[3] 5.0V ±0.5V,3.3V ±0.3V.

[4] All outputs unloaded, I/O pins floating, inputs at rail.

[5] CL1=CL2=100 pF

[6] Same as note [4] except inputs at V_{CC}.

[7] The V_{BO} increases as the temperature decreases.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

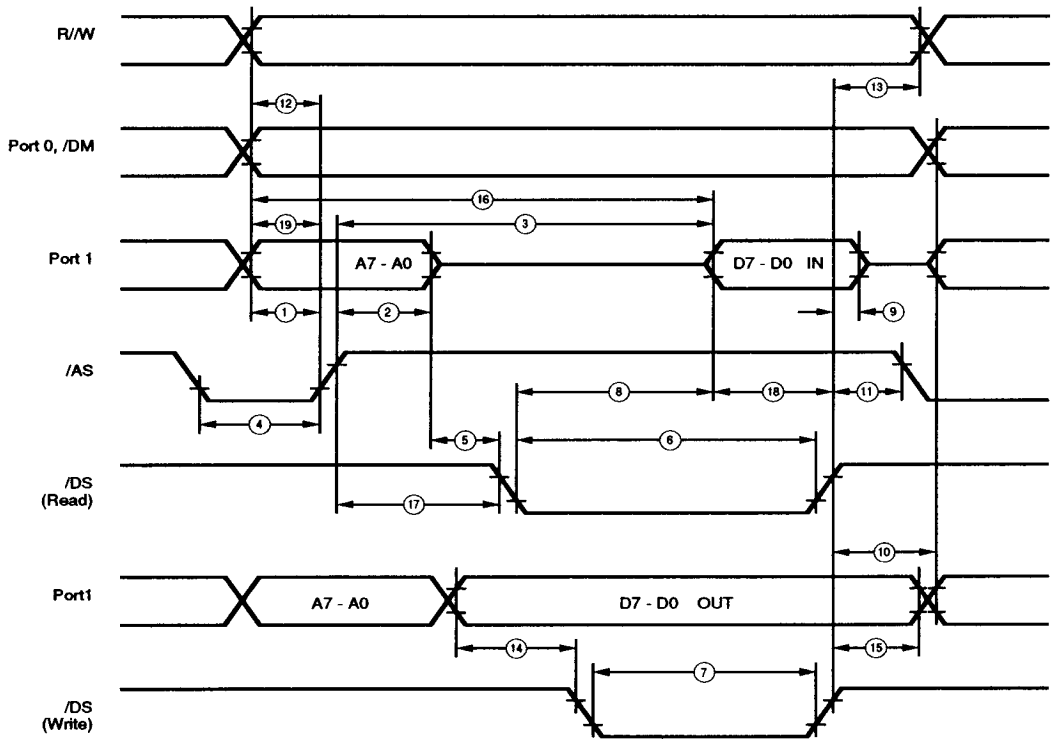


Figure 23. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	V_{cc} Note[3]	T_A = 0°C to 70°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	T_A = -40°C to 105°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TdA(AS)	Address Valid to	3.3	55		35		55		35		ns	[2]
		/AS Rising Delay	5.0	55		35		55		35		ns	
2	TdAS(A)	/AS Rising to Address	3.3	70		45		70		45		ns	[2]
		Float Delay	5.0	70		45		70		45		ns	
3	TdAS(DR)	/AS Rising to Read	3.3		400		250		400		250	ns	[1,2]
		Data Required Valid	5.0		400		250		400		250	ns	
4	TwAS	/AS Low Width	3.3	80		55		80		55		ns	[2]
			5.0	80		55		80		55		ns	
5	Td	Address Float to	3.3	0		0		0		0		ns	
		/DS Falling	5.0	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.3	300		200		300		200		ns	[1,2]
			5.0	300		200		300		200		ns	
7	TwDSW	/DS (Write) Low Width	3.3	165		110		165		110		ns	[1,2]
			5.0	165		110		165		110		ns	
8	TdDSR(DR)	/DS Falling to Read	3.3		260		150		260		150	ns	[1,2]
		Data Required Valid	5.0		260		160		260		160	ns	
9	ThDR(DS)	Read Data to	3.3	0		0		0		0		ns	[2]
		/DS Rising Hold Time	5.0	0		0		0		0		ns	
10	TdDS(A)	/DS Rising to Address	3.3	85		45		85		45		ns	[2]
		Active Delay	5.0	95		55		95		55		ns	
11	TdDS(AS)	/DS Rising to /AS	3.3	60		30		60		30		ns	[2]
		Falling Delay	5.0	70		45		70		45		ns	
12	TdR/W(AS)	R//W Valid to /AS	3.3	70		45		70		45		ns	[2]
		Rising Delay	5.0	70		45		70		45		ns	
13	TdDS(R/W)	/DS Rising to	3.3	70		45		70		45		ns	[2]
		R//W Not Valid	5.0	70		45		70		45		ns	
14	TdDW(DSW)	Write Data Valid to /DS	3.3	80		55		80		55		ns	[2]
		Falling (Write) Delay	5.0	80		55		80		55		ns	
15	TdDS(DW)	/DS Rising to Write	3.3	70		45		70		45		ns	[2]
		Data Not Valid Delay	5.0	80		55		80		55		ns	
16	TdA(DR)	Address Valid to Read	3.3		475		310		475		310	ns	[1,2]
		Data Required Valid	5.0		475		310		475		310	ns	
17	TdAS(DS)	/AS Rising to	3.3	100		65		100		65		ns	[2]
		/DS Falling Delay	5.0	100		65		100		65		ns	
18	TdDI(DS)	Data Input Setup to	0.0	115		115		115		115		ns	[1,2]
		/DS Rising	5.0	75		75		75		75		ns	
19	TdDM(AS)	/DM Valid to /AS	3.3	55		35		55		35		ns	[2]
		Falling Delay	5.0	55		35		55		35		ns	

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] 5.0V ±0.5V, 3.3V ±0.3V.

† Standard Test Load

†† All timing references use 0.9 V_{cc} for a logic 1 and 0.1 V_{cc} for a logic 0.

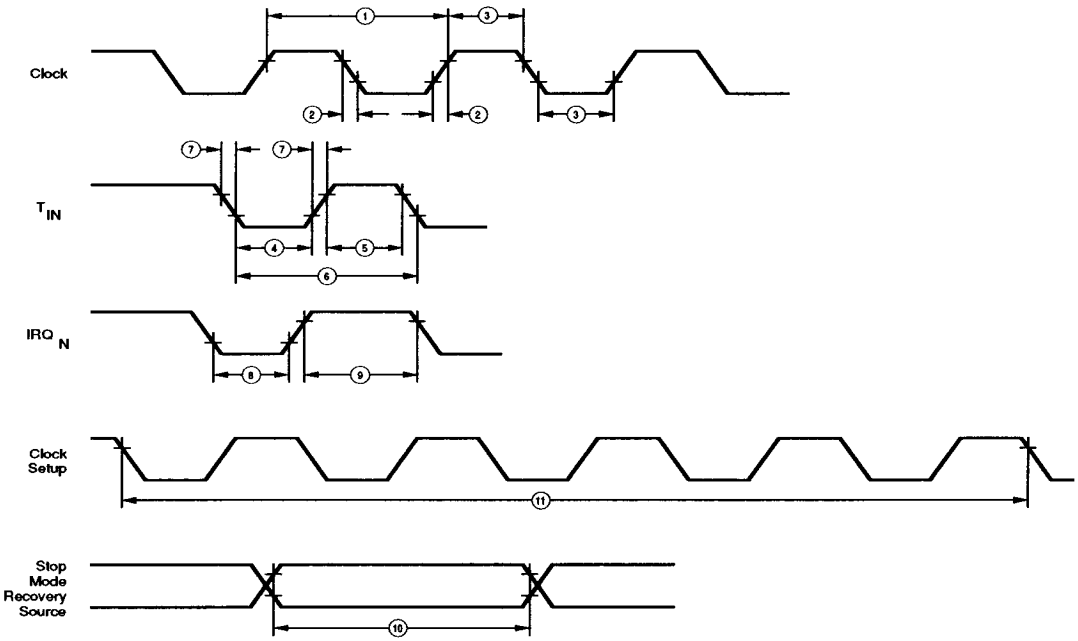


Figure 24. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

No	Symbol	Parameter	V_{cc} Note[6]	T_A = 0°C to 70°C				T_A = -40°C to 105°C				Units	Notes
				8 MHz		12 MHz		8 MHz		12 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	3.3V	125	100000	83	100000	125	100000	83	100000	ns	[1]
			5.0V	125	100000	83	100000	125	100000	83	100000	ns	[1]
2	TrC,TfC	Clock Input Rise	3.3V		25		15		25		15	ns	[1]
		and Fall Times	5.0V		25		15		25		15	ns	[1]
3	TwC	Input Clock Width	3.3V	37		26		37		26		ns	[1]
			5.0V	37		26		37		26		ns	[1]
4	TwTinL	Timer Input	3.3V	100		100		100		100		ns	[1]
		Low Width	5.0V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input	3.3V	3TpC		3TpC		3TpC		3TpC			[1]
		High Width	5.0V	3TpC		3TpC		3TpC		3TpC			[1]
6	TpTin	Timer Input Period	3.3V	8TpC		8TpC		8TpC		8TpC			[1]
			5.0V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin,TfTin	Timer Input Rise	3.3V		100		100		100		100	ns	[1]
		and Fall Timers	5.0V		100		100		100		100	ns	[1]
8A	TwIL	Interrupt Request	3.3V	100		100		100		100		ns	[1,2]
		Low Time	5.0V	70		70		70		70		ns	[1,2]
8B	TwIL	Int. Request	3.3V	3TpC		3TpC		3TpC		3TpC			[1,3]
		Low Time	5.0V	3TpC		3TpC		3TpC		3TpC			[1,3]
9	TwIH	Interrupt Request	3.3V	3TpC		3TpC		3TpC		3TpC			[1,2]
		Input High Time	5.0V	3TpC		3TpC		3TpC		3TpC			[1,2]
10	Twsm	STOP Mode	3.3V	12		12		12		12		ns	
		Recovery Width Spec	5.0V	12		12		12		12		ns	
			3.3V	5TpC									[7]
			5.0V	5TpC									[8]

AC CHARACTERISTICS
Additional Timing Table (Continued)

No	Symbol	Parameter	V_{cc} Note[6]	T_A = 0°C to 70°C				T_A = -40°C to 105°C				Units	Notes
				8 MHz		12 MHz		8 MHz		12 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
11	Tost	Oscillator	3.3V		5TpC		5TpC		5TpC		5TpC		[4]
		Startup Time	5.0V		5TpC		5TpC		5TpC		5TpC		[4]
12	Twdt	Watchdog Timer	3.3V	10		10		10		10		ms	D0 = 0 [5]
		Delay Time	5.0V	5		5		5		5		ms	D1 = 0 [5]
			3.3V	30		30		30		30		ms	D0 = 1 [5]
			5.0V	15		15		15		15		ms	D1 = 0 [5]
			3.3V	50		50		50		50		ms	D0 = 0 [5]
			5.0V	25		25		25		25		ms	D1 = 1 [5]
			3.3V	200		200		200		200		ms	D0 = 1 [5]
			5.0V	100		100		100		100		ms	D1 = 1 [5]

Notes:
[1] Timing Reference uses 0.9 V_{cc} for a logic 1 and 0.1 V_{cc} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 0
[5] Reg. WDTMR
[6] 5.0V ±0.5V, 3.3V ±0.3V
[7] Reg. SMR - D5=0
[8] Reg. SMR - D5=1

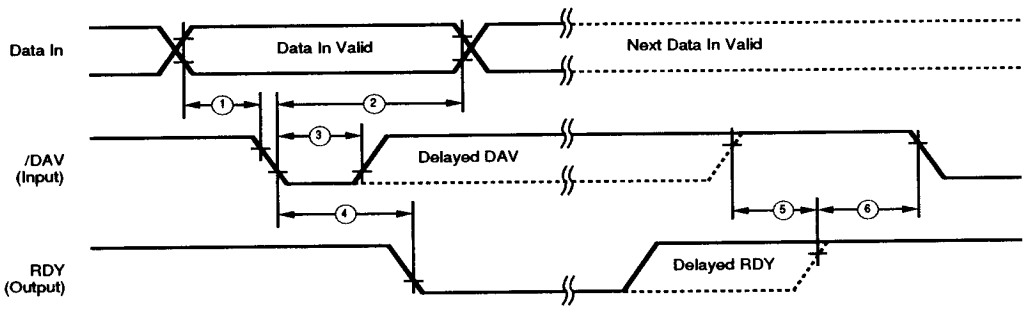


Figure 25. Input Handshake Timing

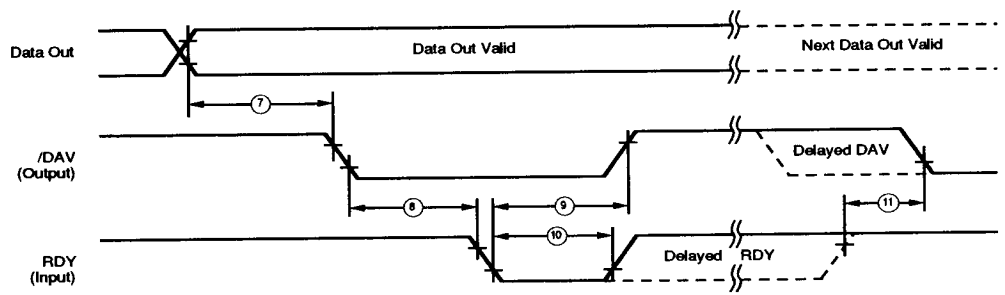


Figure 26. Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

No	Symbol	Parameter	V_{cc} Note[1]	T_A = 0°C To 70° C				T_A = -40° C To 105° C				Data Direction
				8 MHz		12 MHz		8 MHz		12 MHz		
				Min	Max	Min	Max	Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	3.3V	0		0		0		0		IN
			5.0V	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	3.3V	160		160		160		160		IN
			5.0V	115		115		115		115		IN
3	TwDAV	Data Available Width	3.3V	155		155		155		155		IN
			5.0V	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Falling to RDY	3.3V		160		160		160		160	IN
		Falling Delay	5.0V		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rising to RDY	3.3V		120		120		120		120	IN
		Falling Delay	5.0V		80		80		80		80	IN
6	TdDO(DAV)	RDY Rising to DAV	3.3V	0		0		0		0		IN
		Falling Delay	5.0V	0		0		0		0		IN
7	TcLDAV0(RDY)	Data Out to DAV	3.3V	63		42		63		42		OUT
		Falling Delay	5.0V	63		42		63		42		OUT
8	TcLDAV0(RDY)	DAV Falling to RDY	3.3V	0		0		0		0		OUT
		Falling Delay	5.0V	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	3.3V		160		160		160		160	OUT
		Rising Delay	5.0V		115		115		115		115	OUT
10	TwRDY	RDY Width	3.3V	110		110		110		110		OUT
			5.0V	80		80		80		80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV	3.3V		110		110		110		110	OUT
		Falling Delay	5.0V		80		80		80		80	OUT

Note:
[1] 5.0 V ±0.5V, 3.3V ±0.3V

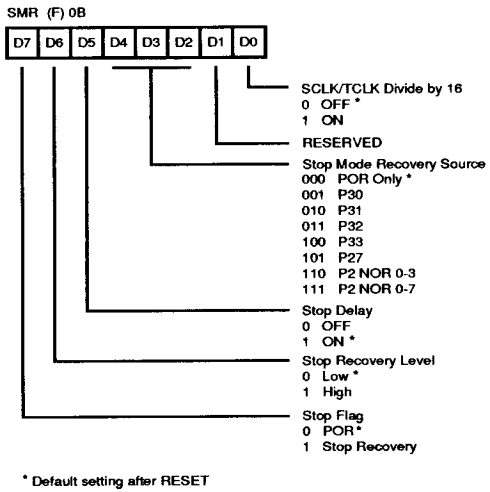


Figure 27. Stop Mode Recovery Register

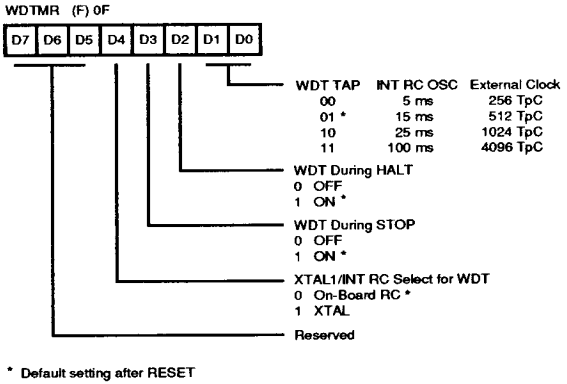


Figure 28. Watchdog Timer Mode Register

R240

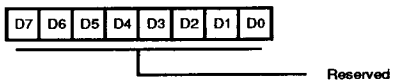


Figure 29. Reserved

R241 TMR

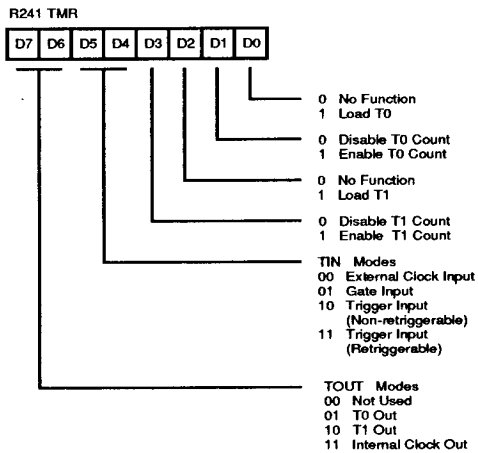


Figure 30. Timer Mode Register ($F1_H$:Read/Write)

R242 T1

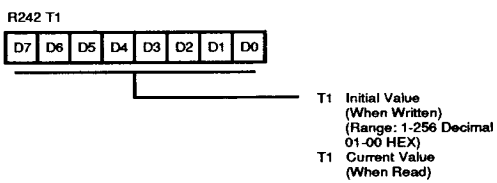


Figure 31. Counter/Timer 1 Register ($F2_H$:Read/Write)

R243 PRE1

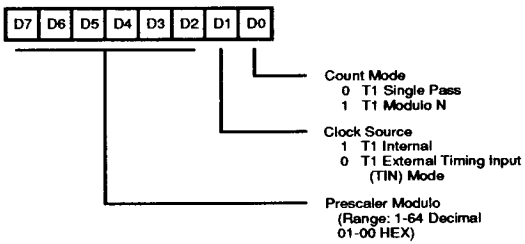


Figure 32. Prescaler 1 Register ($F3_H$:Write Only)

R244 T0

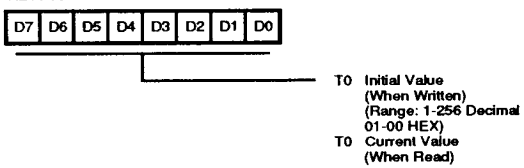


Figure 33. Counter/Timer 0 Register ($F4_H$:Read/Write)

R245 PRE0

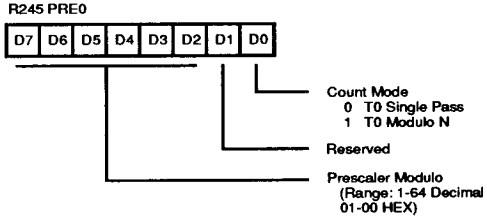


Figure 34. Prescaler 0 Register ($F5_H$:Write Only)

R246 P2M

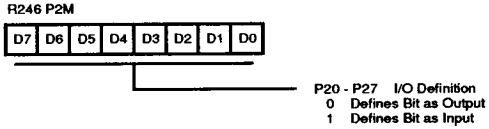


Figure 35. Port 2 Mode Register ($F6_H$: Write Only)

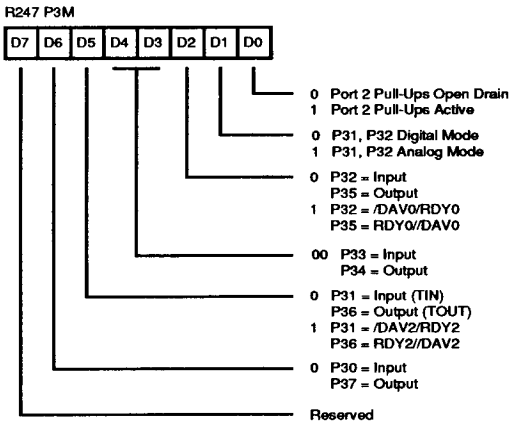


Figure 36. Port 3 Mode Register ($F7_H$:Write Only)

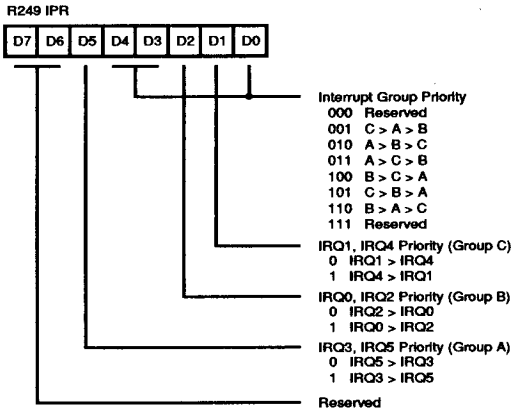


Figure 38. Interrupt Priority Register ($F9_H$:Write Only)

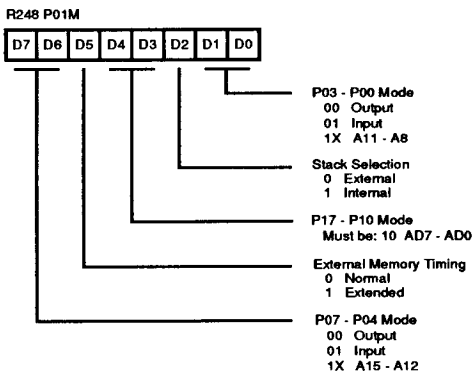


Figure 37. Ports 0 and 1 Mode Registers ($F8_H$:Write Only)

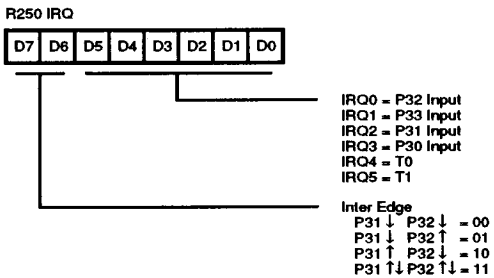


Figure 39. Interrupt Request Register (FA_H:Read/Write)

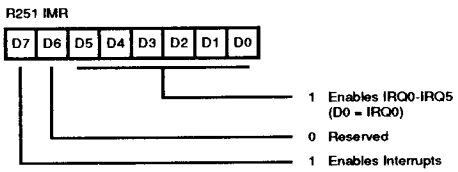


Figure 40. Interrupt Mask Register (FB_H:Read/Write)

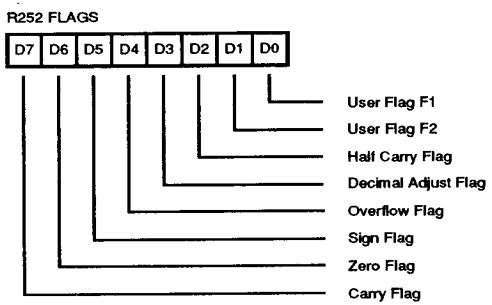


Figure 41. Flag Register (FC_H:Read/Write)

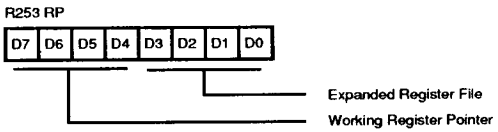


Figure 42. Register Pointer (FD_H:Read/Write)

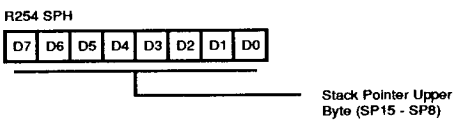


Figure 43. Stack Pointer High (FE_H:Read/Write)

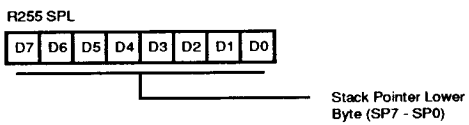


Figure 44. Stack Pointer Low (FF_H:Read/Write)

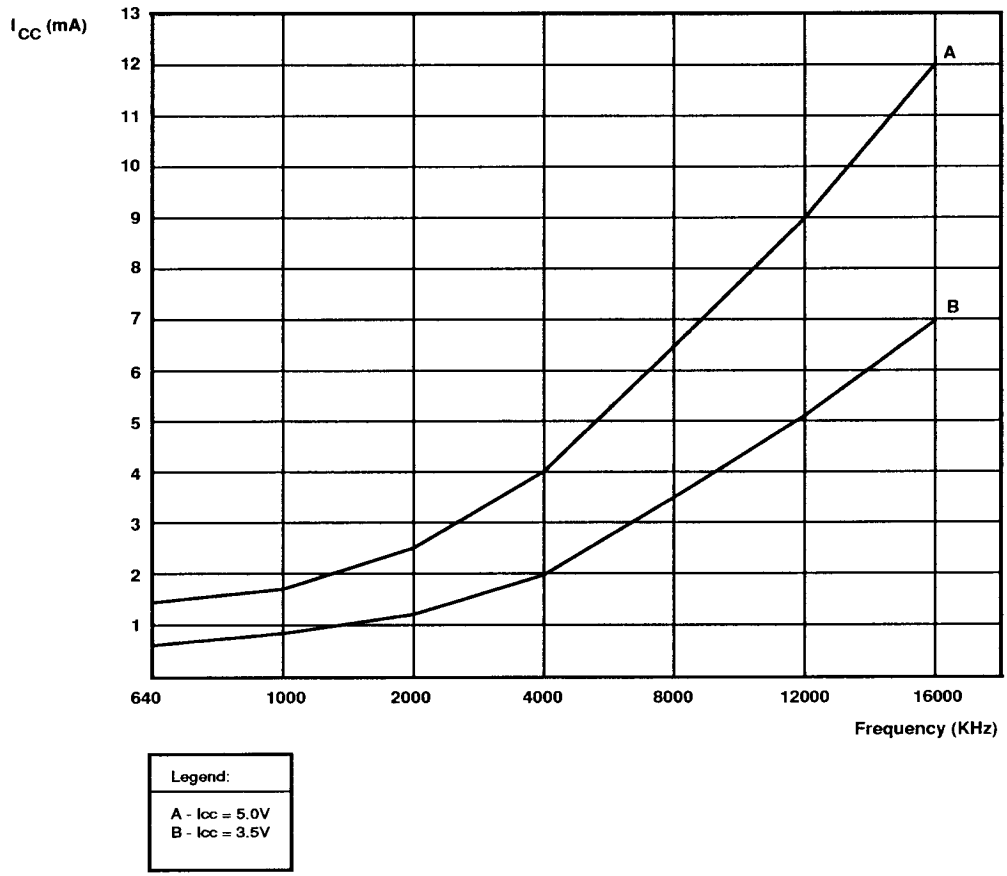


Figure 45. Typical I_{cc} vs Frequency

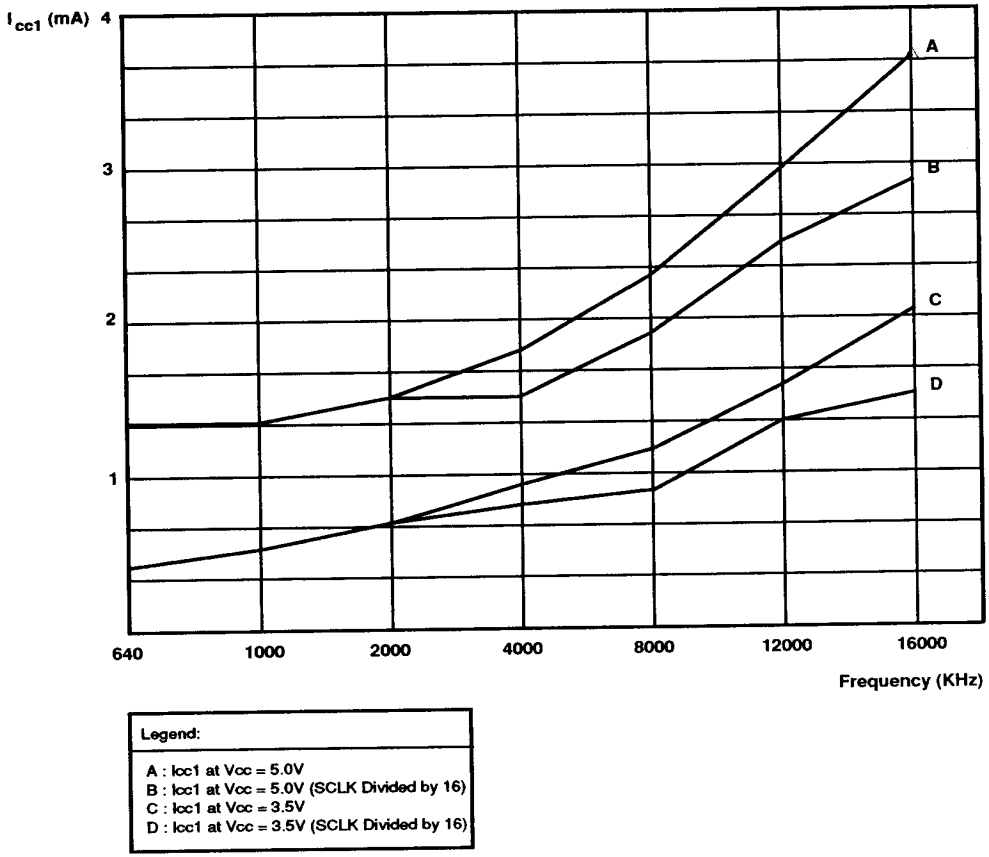


Figure 46. Typical I_{cc1} vs Frequency

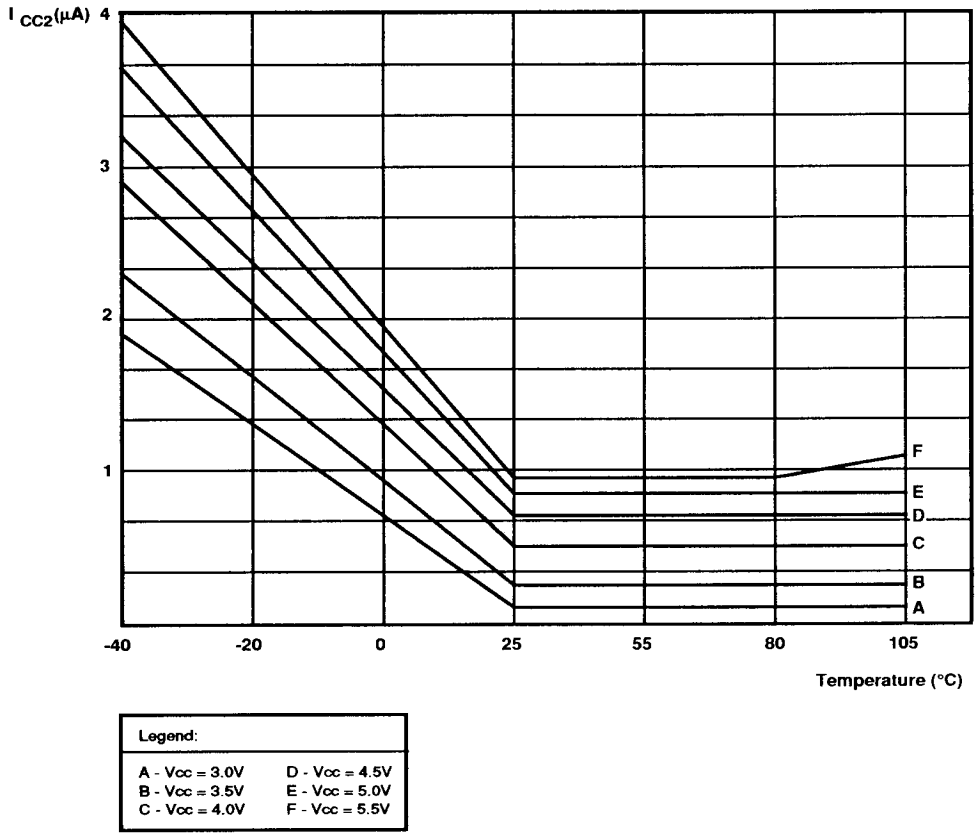
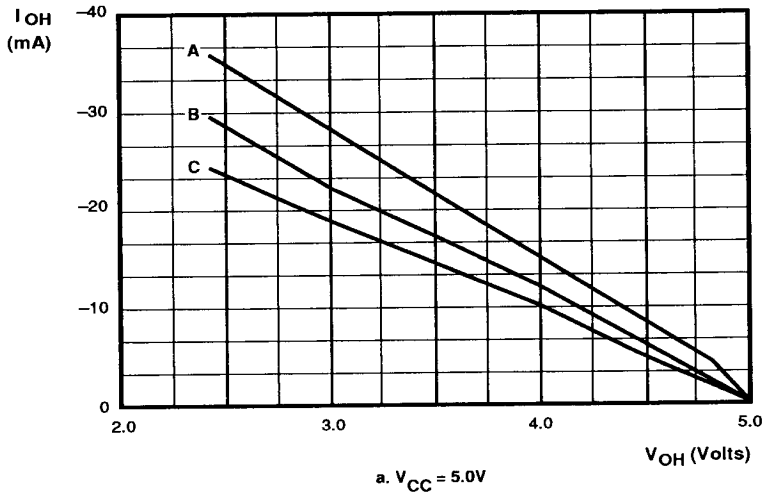
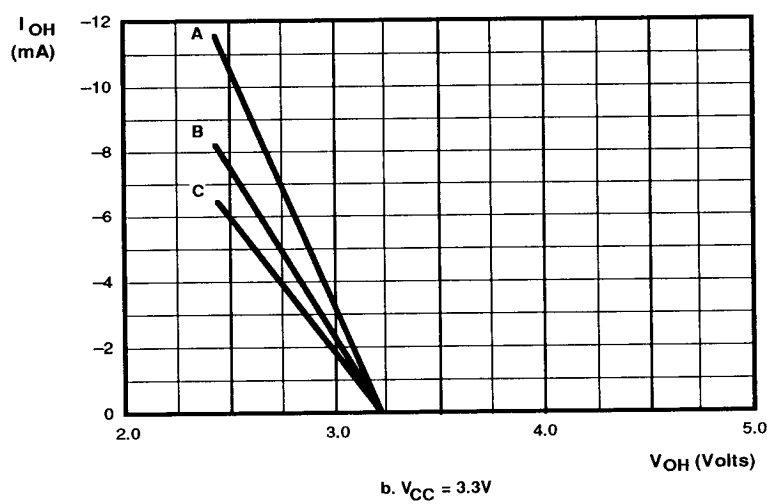


Figure 47. Typical I_{CC2} vs Frequency



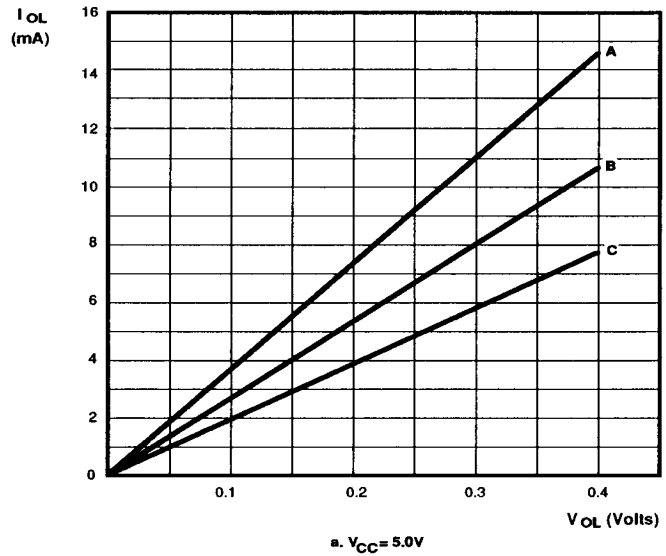
a. V_{CC} = 5.0V



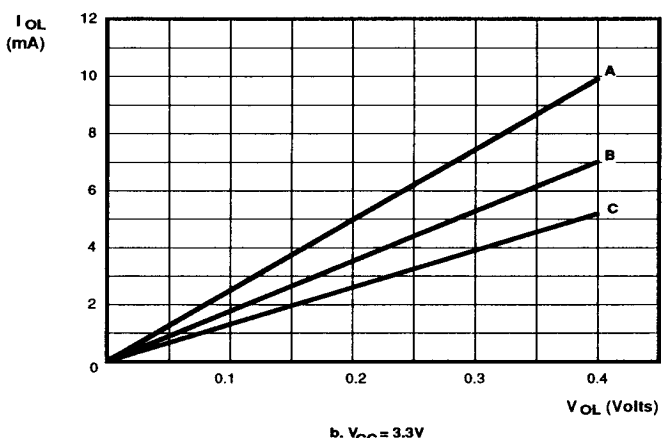
b. V_{CC} = 3.3V

Legend:
A = –55°C
B = 25°C
C = 125°C

Figure 48. Typical I_{OH} vs V_{OH} Over Temperature



a. V_{CC} = 5.0V



b. V_{CC} = 3.3V

Legend:
A = –55°C
B = 25°C
C = 125°C

Figure 49. Typical I_{OL} vs V_{OL} Over Temperature

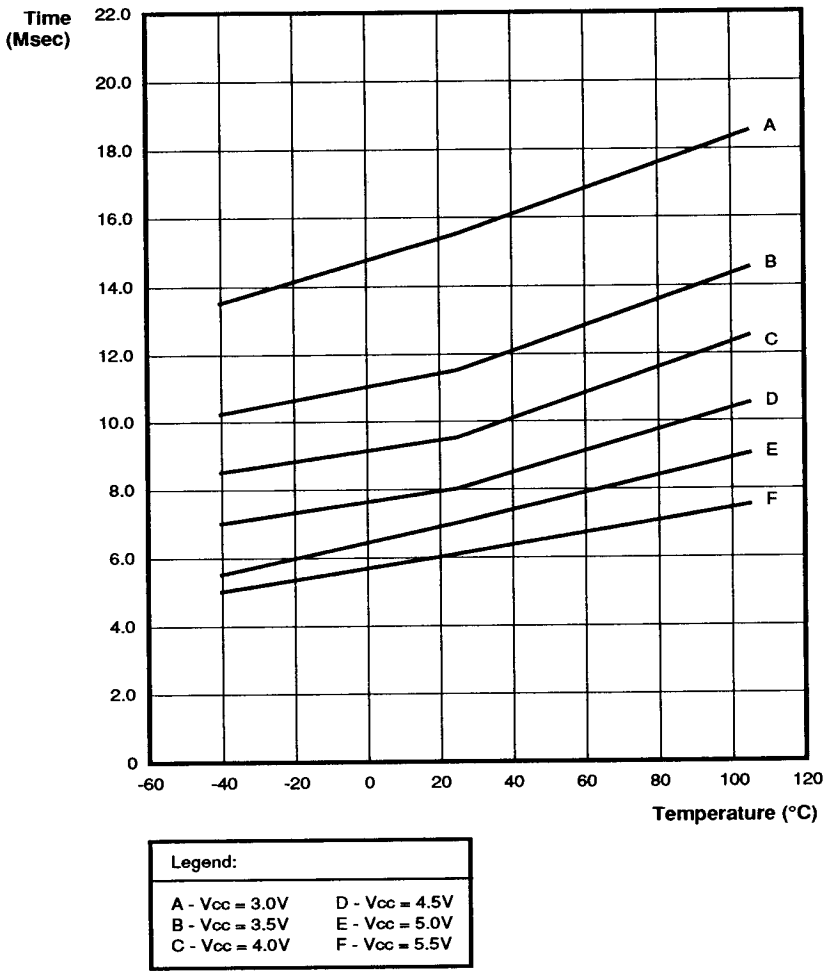
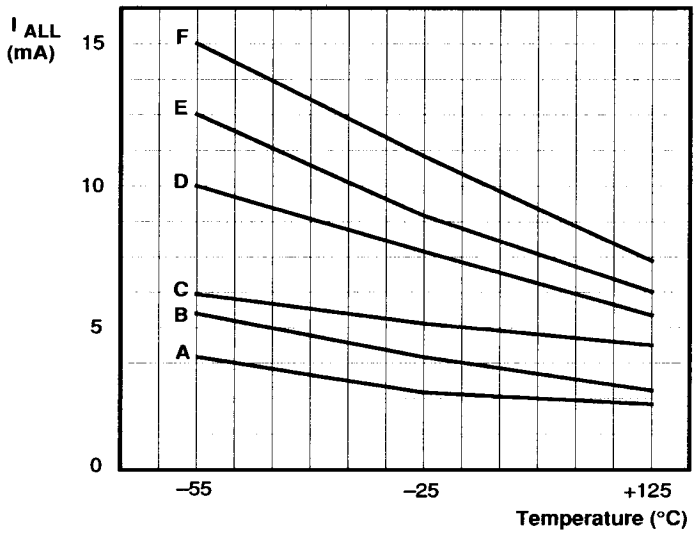
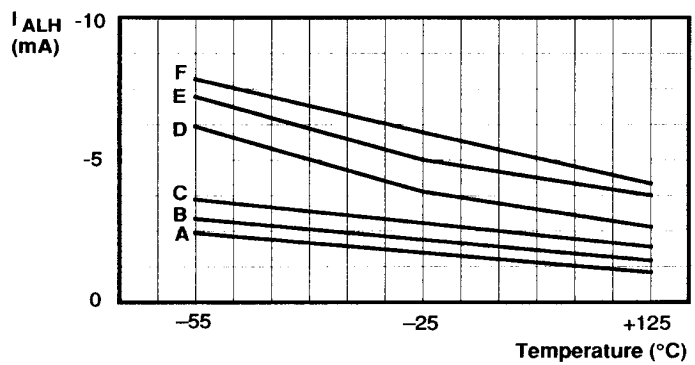


Figure 50. Typical Power-On Reset Time vs Temperature



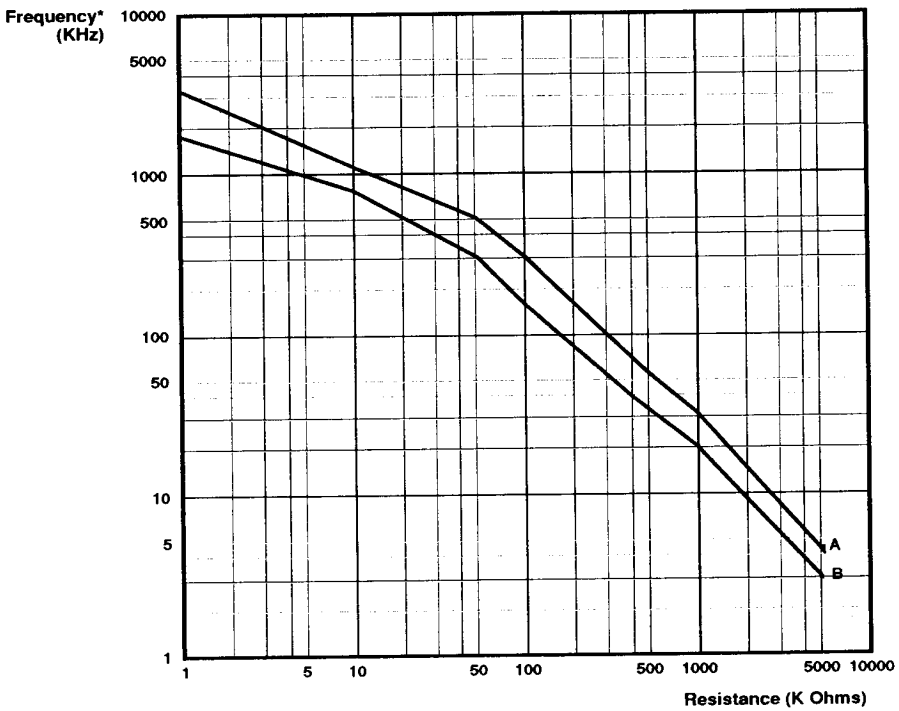
a. Typical Auto Latch Low Current vs Temperature



b. Typical Auto Latch High Current vs Temperature

Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.3V	E - Vcc = 5.0V
C - Vcc = 3.6V	F - Vcc = 5.5V

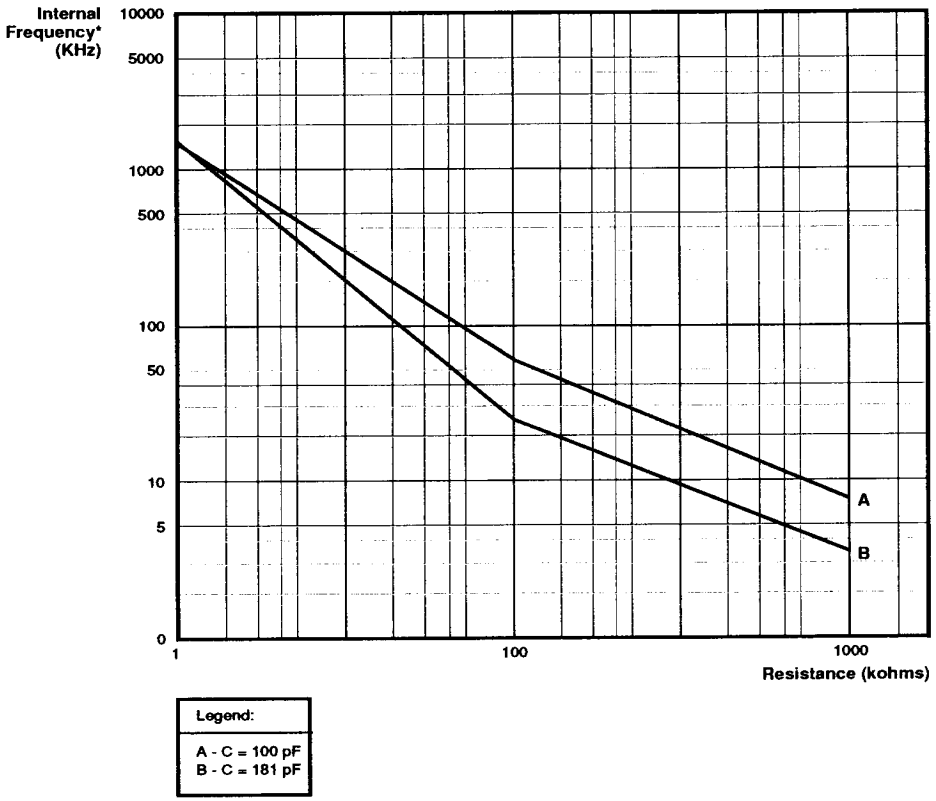
Figure 51. Typical Auto-Latch Current vs Temperature



Legend:
A - Vcc = 5.0V C = 33pF B - Vcc = 3.3V C = 33pF

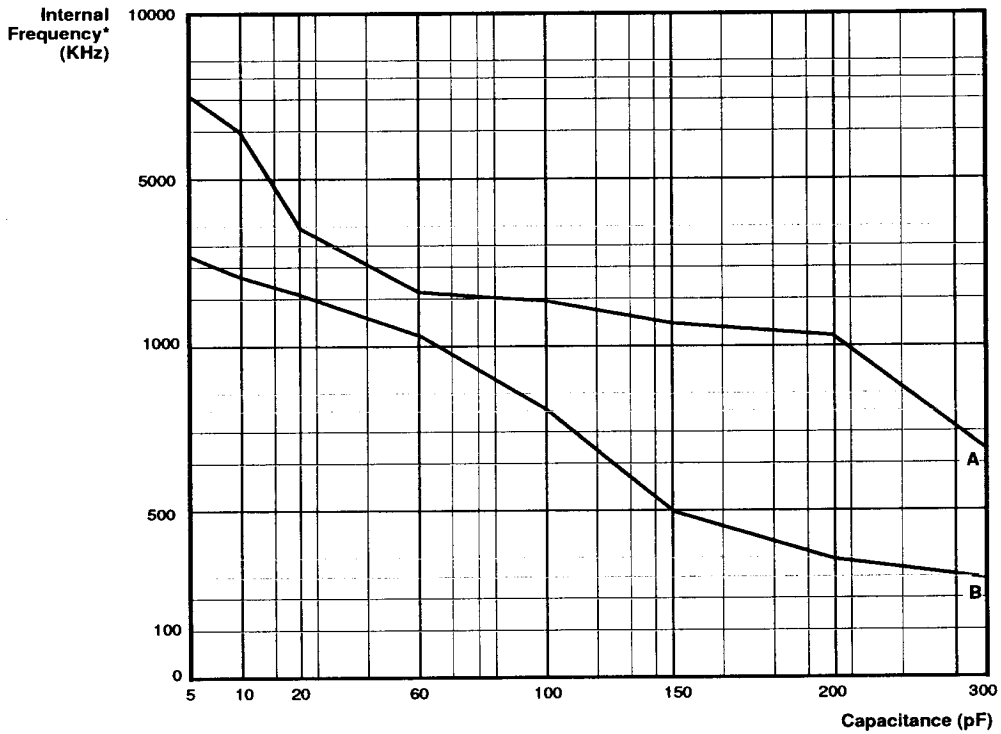
Note: * The internal clock frequency is one half the external clock frequency.
This chart for reference only. Each process will have a different characteristic curve.

Figure 52. Typical Internal Frequency vs RC Resistance



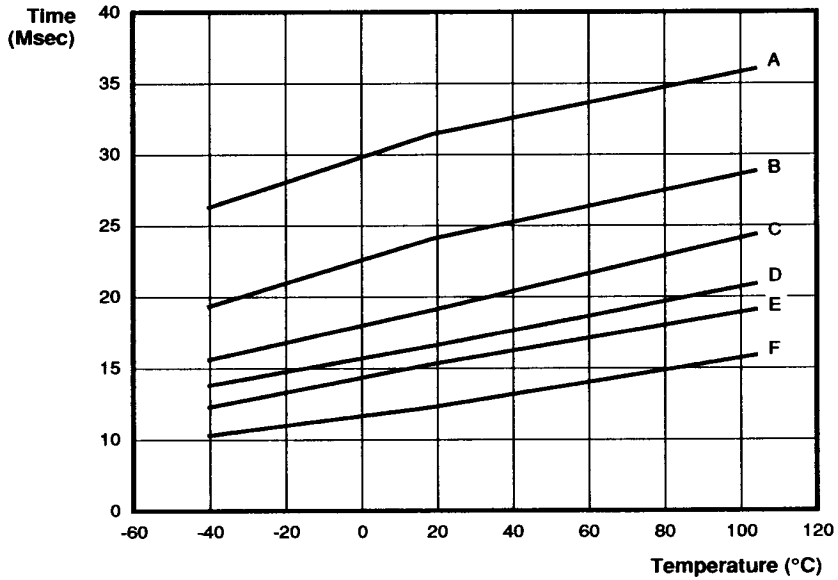
Note: * The internal clock frequency is one half the external clock frequency.
This chart for reference only. Each process will have a different characteristc curve.

Figure 53. Typical Internal Frequency vs Resistance



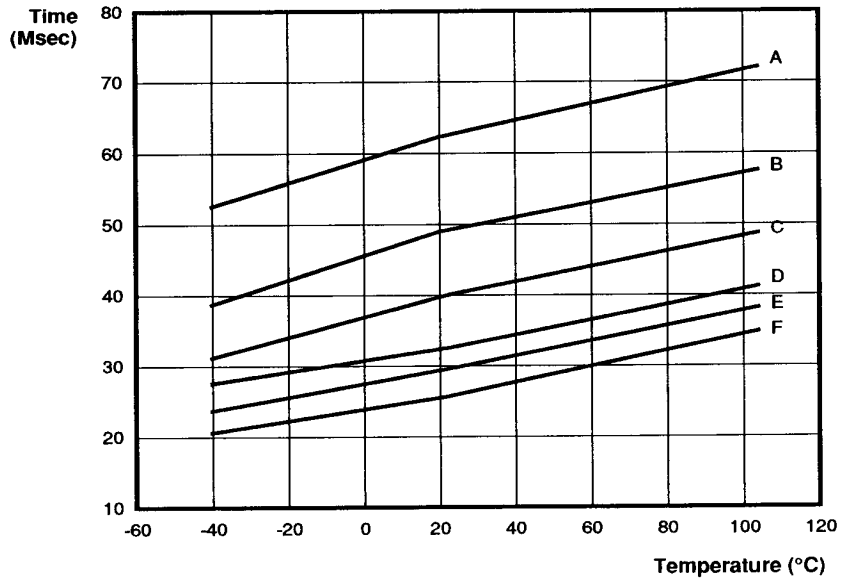
Note: * The internal clock frequency is one half the external clock frequency.
This chart for reference only. Each process will have a different characteristc curve.
R = 1 kohm

Figure 54. Typical Internal Frequency vs RC Capacitance



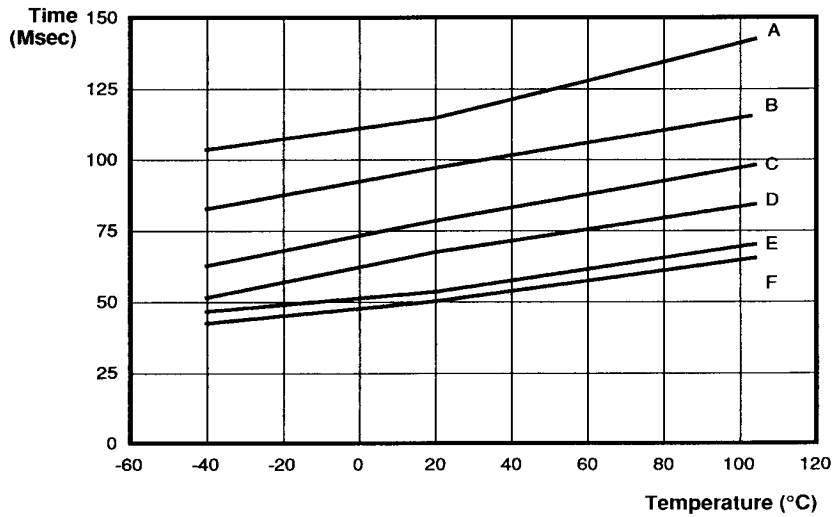
Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 55. Typical 5 ms WDT Setting vs Temperature



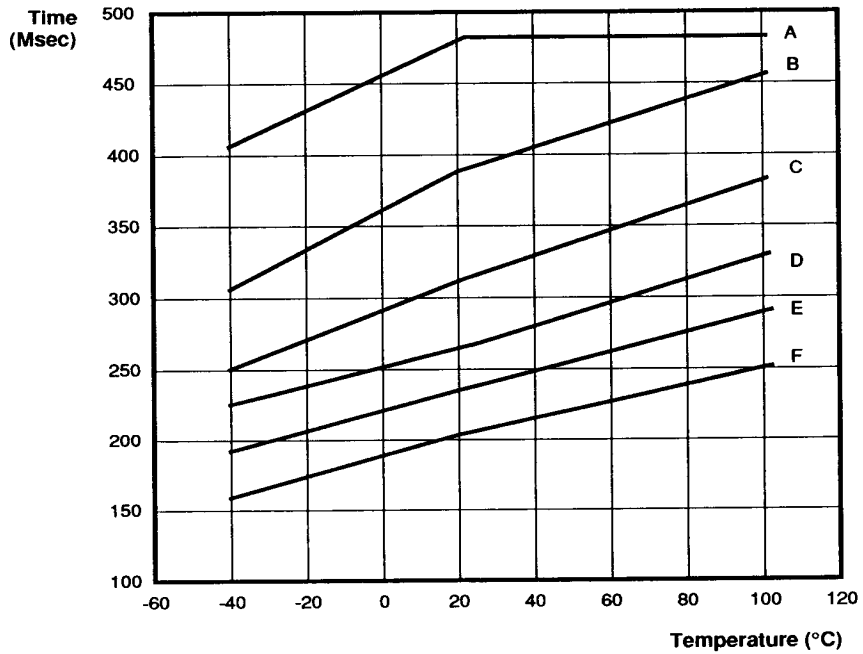
Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 56. Typical 15 ms WDT Setting vs Temperature



Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 57. Typical 25 ms WDT Setting vs Temperature



Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 58. Typical 100 ms WDT Setting vs Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

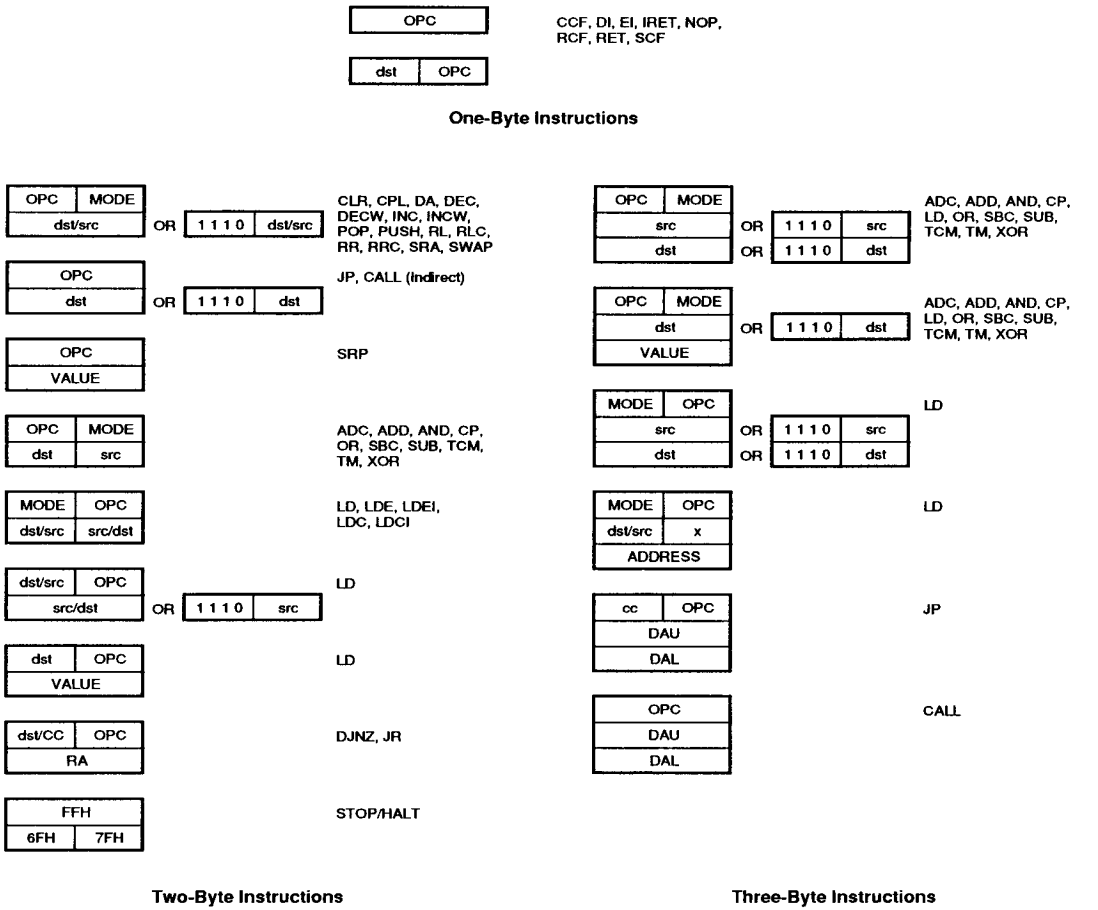
Affected flages are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

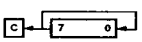
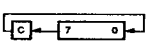
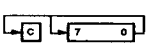
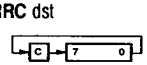
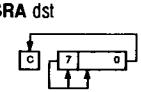
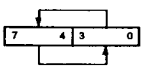
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r Irr	Irr r	C2 D2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir Irr	Irr Ir	C3 D3	-	-	-	-	-	-
LDE dst, src dst←src	r Irr	Irr Ir	82 92	-	-	-	-	-	-
LDEI dst, src dst←src r←r + 1;rr←rr + 1	Ir Irr	Irr Ir	83 93	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src	R IR		70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP dst RP←src		Im	31	-	-	-	-	-	-
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

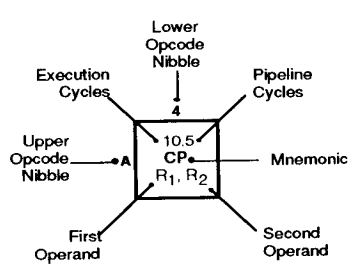
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								5.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



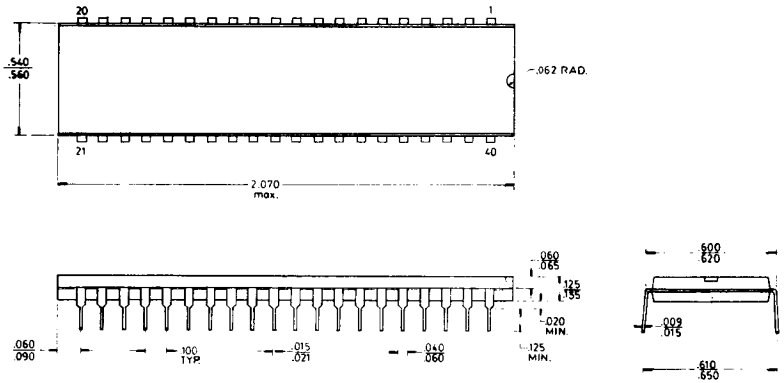
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

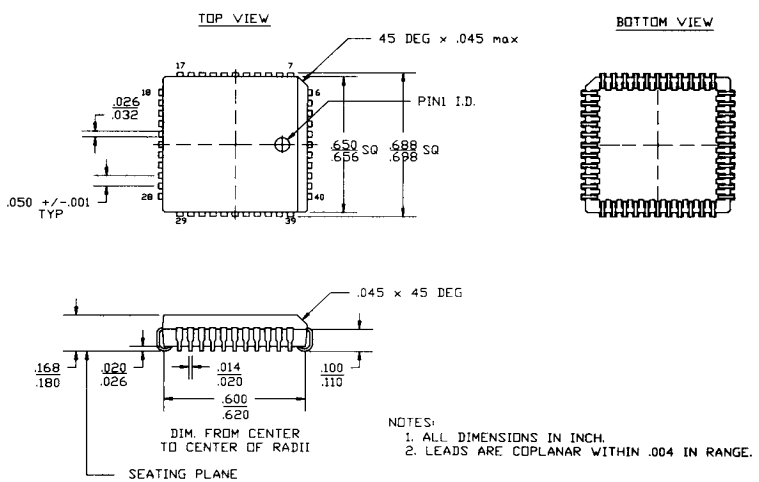
Note: Blank areas not defined.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION

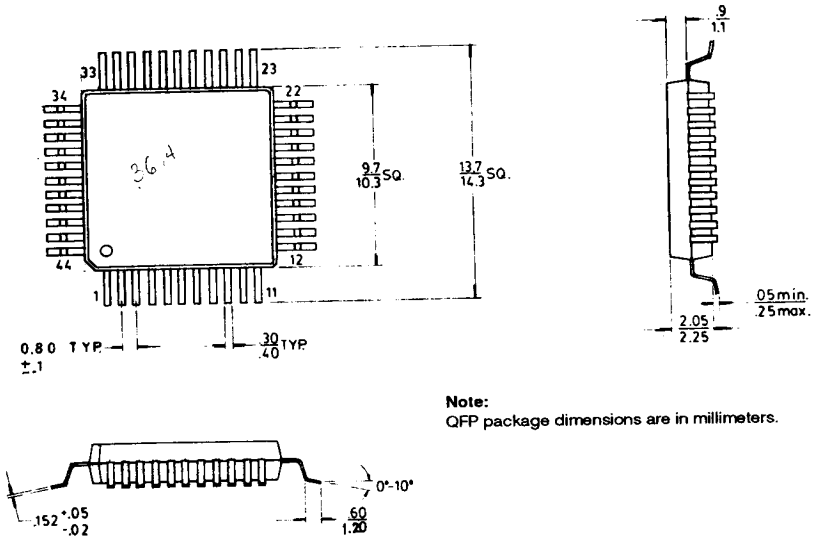


40-Pin Dual-In-Line (DIP) Plastic Package



44-Pin Plastic Chip Carrier (PLCC)

PACKAGE INFORMATION (Continued)



Note:
QFP package dimensions are in millimeters.

44-Pin Quad Flat Pack (QFP)

ORDERING INFORMATION

Z86C90

8 MHZ

40-Pin DIP	40-Pin PLCC	44-Pin QFP
Z86C9008PSC	Z86C9008VSC	Z86C9008FSC
Z86C9008PEC	Z86C9008VEC	Z86C9008FEC

12 MHz

40-Pin DIP	40-Pin PLCC	44-Pin QFP
Z86C9012PSC	Z86C9012VSC	Z86C9012FSC
Z86C9012PEC	Z86C9012VEC	Z86C9012FEC

Z86C89

8 MHz

40-Pin DIP	40-Pin PLCC	44-Pin QFP
Z86C8908PSC	Z86C8908VSC	Z86C8908FSC
Z86C8908PEC	Z86C8908VEC	Z86C8908FEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Codes

Package
P = Plastic DIP
V = Plastic Chip Carrier
C = Ceramic DIP
L = Ceramic LCC

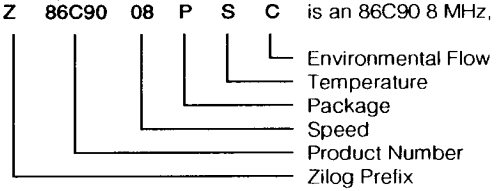
Longer Lead Time
F = Plastic Quad Flat Pack

Speed
8 = 8 MHz
12 = 12 MHz

Temperature
E = -40°C to +105°C
S = 0°C to + 70°C

Example:

Z 86C90 08 P S C is an 86C90 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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